



NX7002AKS

60 V, dual N-channel Trench MOSFET

Rev. 1 — 1 March 2012

Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- ESD protection

1.3 Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

1.4 Quick reference data

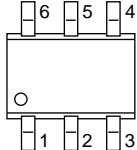
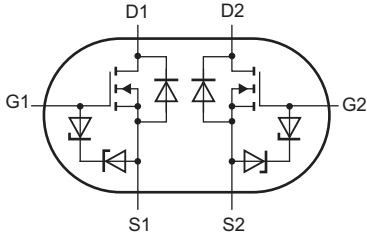
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	170	mA
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 100\text{ mA}; T_j = 25\text{ °C}$	-	3	4.5	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>SOT363 (TSSOP6)</p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX7002AKS	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
NX7002AKS	TD%

[1] % = placeholder for manufacturing site code

5. Limiting values

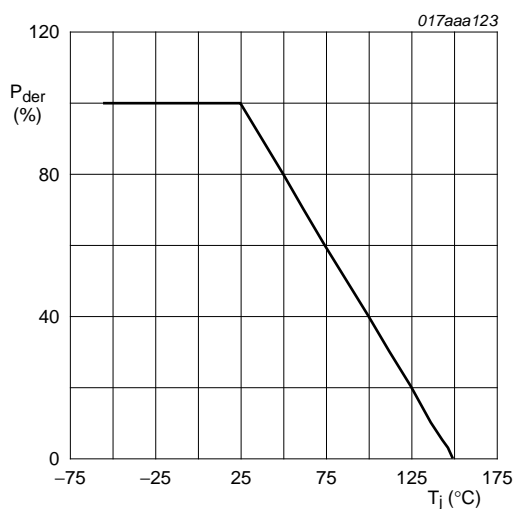
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	60	V	
V_{GS}	gate-source voltage		-20	20	V	
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	170	mA
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	100	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	680	mA	
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	220	mW
			[1]	-	255	mW
		$T_{sp} = 25\text{ °C}$	-	1060	mW	
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	170	mA
Per device						
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	330	mW
T_j	junction temperature		-55	150	°C	
T_{amb}	ambient temperature		-55	150	°C	
T_{stg}	storage temperature		-65	150	°C	

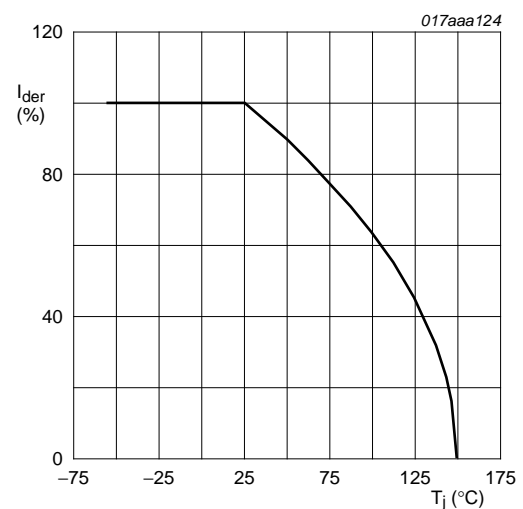
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



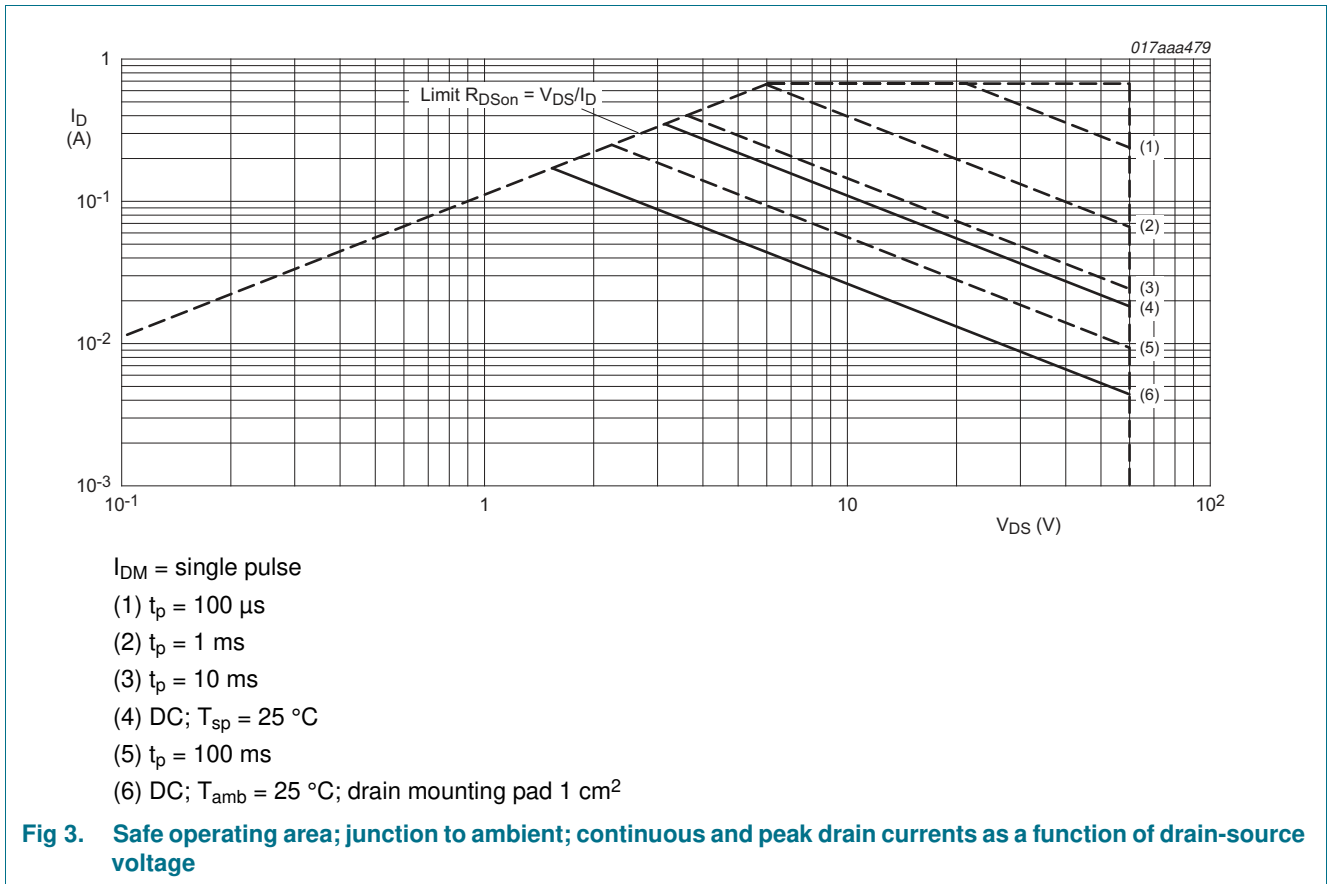
$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ °C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25\text{ °C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



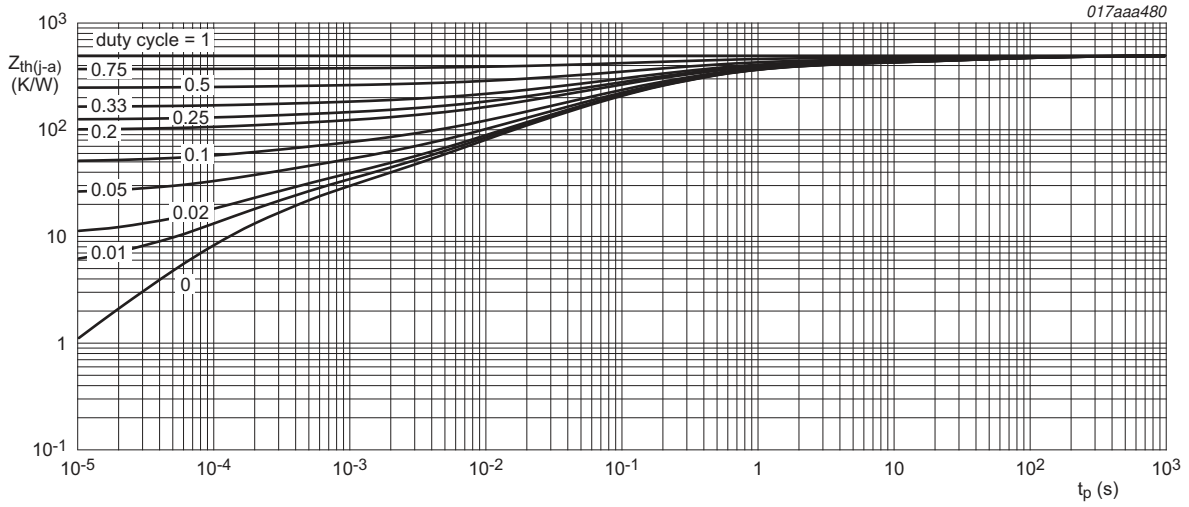
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	500	560	K/W
			[2]	-	450	480	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	115	K/W	

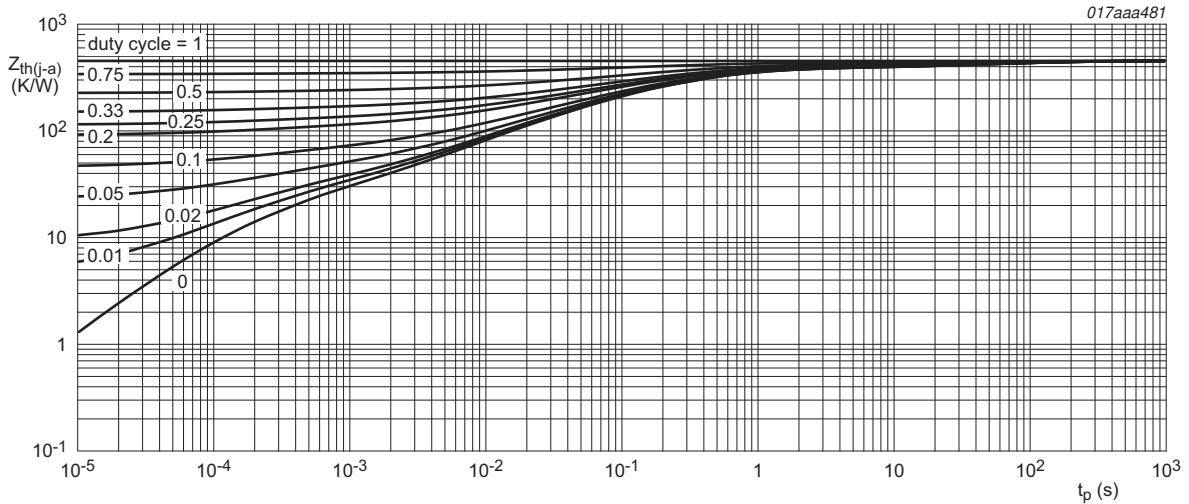
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



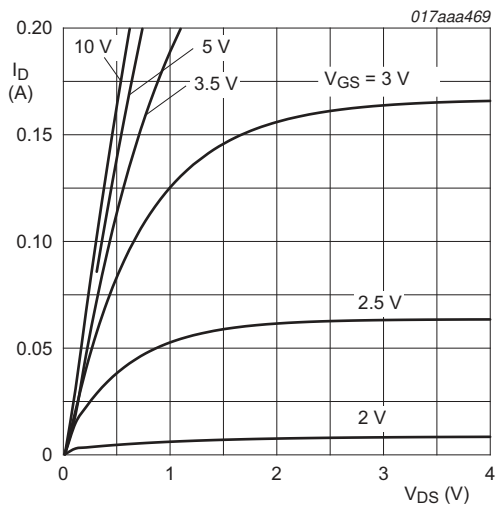
FR4 PCB, mounting pad for drain 1 cm²

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

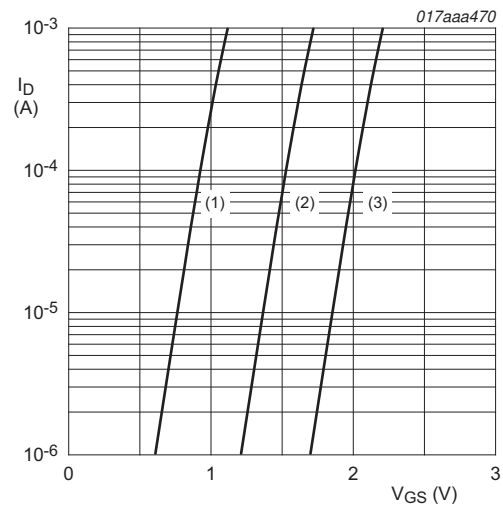
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	1.1	1.6	2.1	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 60 V$; $V_{GS} = 0 V$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	2	μA
		$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	2	μA
		$V_{GS} = 10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	0.5	μA
		$V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	0.5	μA
		$V_{GS} = 5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 100 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	3	4.5	Ω
		$V_{GS} = 10 V$; $I_D = 100 \text{ mA}$; $T_j = 150 \text{ }^\circ\text{C}$	-	6.2	9.2	Ω
		$V_{GS} = 5 V$; $I_D = 100 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	3.7	5.2	Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V$; $I_D = 200 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	230	-	mS
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V$; $I_D = 200 \text{ mA}$; $V_{GS} = 4.5 V$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.33	0.43	nC
Q_{GS}	gate-source charge		-	0.12	-	nC
Q_{GD}	gate-drain charge		-	0.09	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	-	11	17	pF
C_{oss}	output capacitance		-	3.4	-	pF
C_{rss}	reverse transfer capacitance		-	1.4	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 V$; $R_L = 250 \Omega$; $V_{GS} = 10 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	6	12	ns
t_r	rise time		-	7	-	ns
$t_{d(off)}$	turn-off delay time		-	20	40	ns
t_f	fall time		-	14	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 115 \text{ mA}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ\text{C}$	0.47	0.7	1.2	V



$T_j = 25\text{ }^\circ\text{C}$

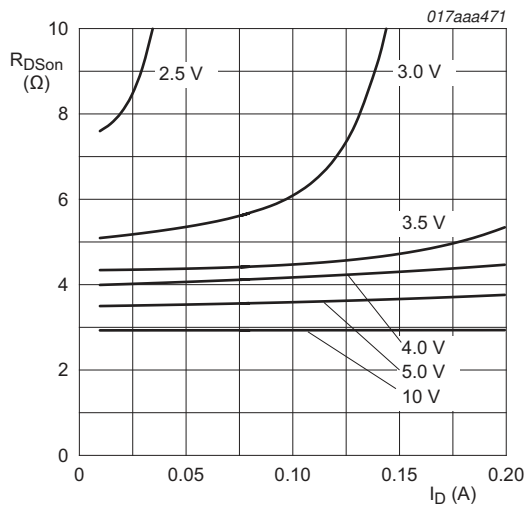
Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

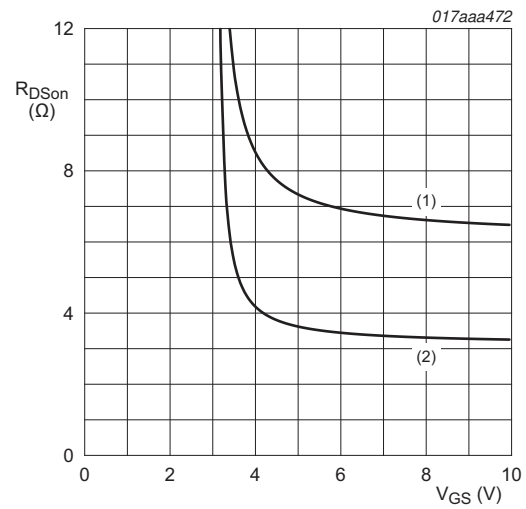
- (1) minimum values
- (2) typical values
- (3) maximum values

Fig 7. Subthreshold drain current as a function of gate-source voltage



$T_j = 25\text{ }^\circ\text{C}$

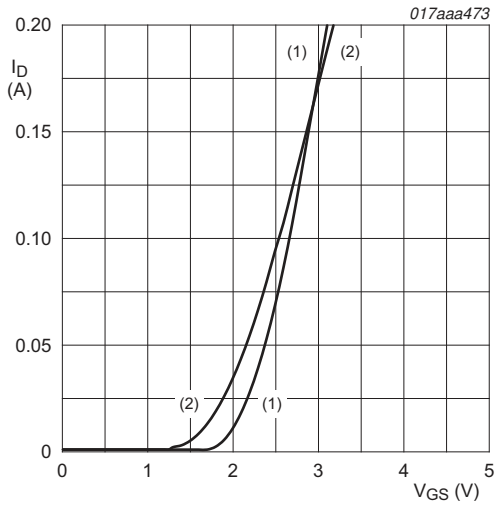
Fig 8. Drain-source on-state resistance as a function of drain current; typical values



$I_D = 0.2\text{ A}$

- (1) $T_j = 150\text{ }^\circ\text{C}$
- (2) $T_j = 25\text{ }^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DS(on)}$
 (1) $T_j = 25\text{ °C}$
 (2) $T_j = 150\text{ °C}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

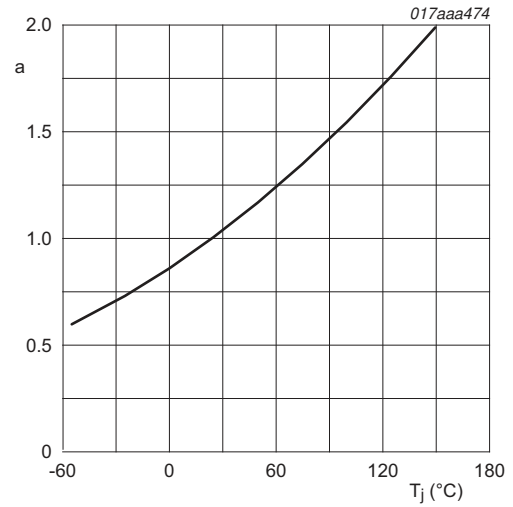
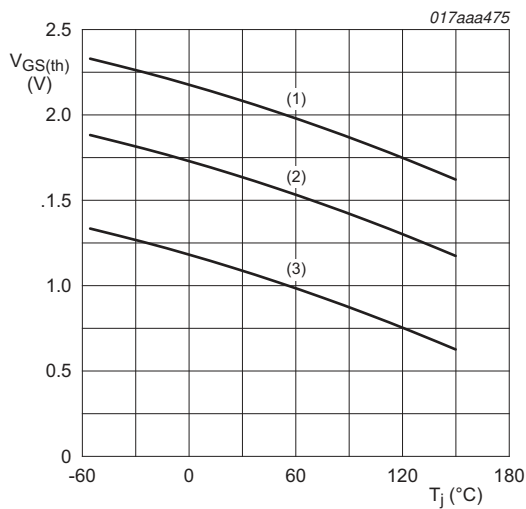
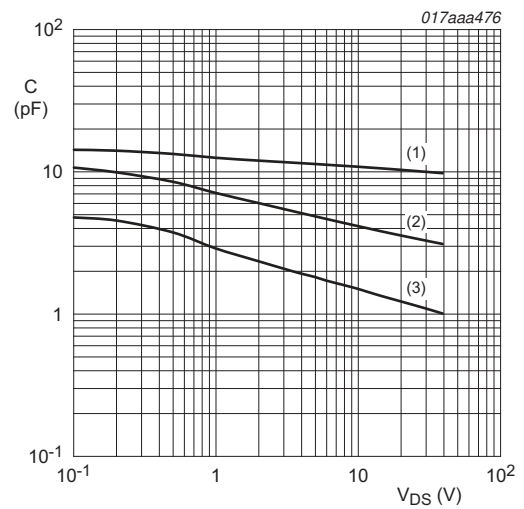


Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



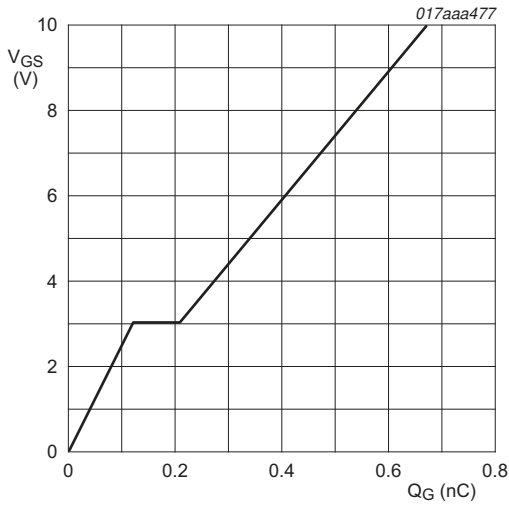
$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$
 (1) maximum values
 (2) typical values
 (3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$
 (1) C_{iss}
 (2) C_{oss}
 (3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 0.2 \text{ A}$; $V_{DS} = 30 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 14. Gate-source voltage as a function of gate charge; typical values

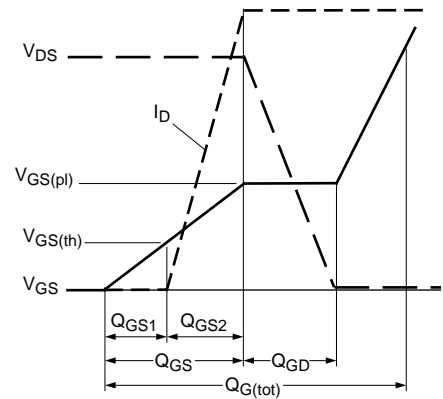
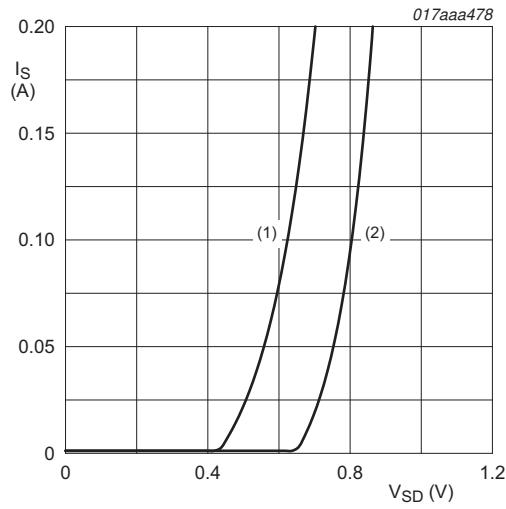


Fig 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$
 (1) $T_j = 150 \text{ }^\circ\text{C}$
 (2) $T_j = 25 \text{ }^\circ\text{C}$

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

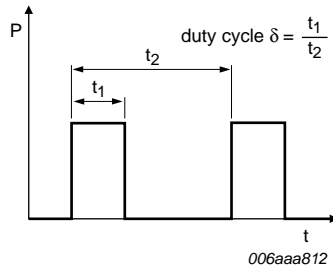


Fig 17. Duty cycle definition

9. Package outline

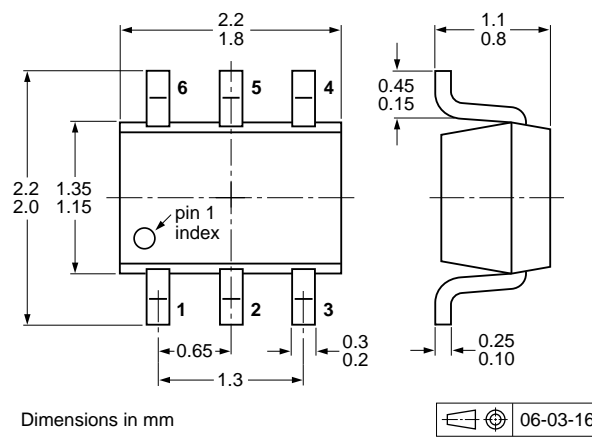


Fig 18. Package outline SOT363 (TSSOP6)

10. Soldering

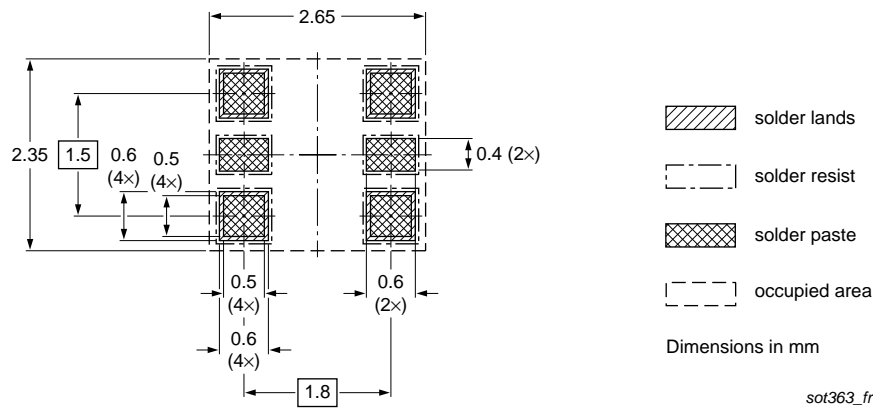


Fig 19. Reflow soldering footprint for SOT363 (TSSOP6)

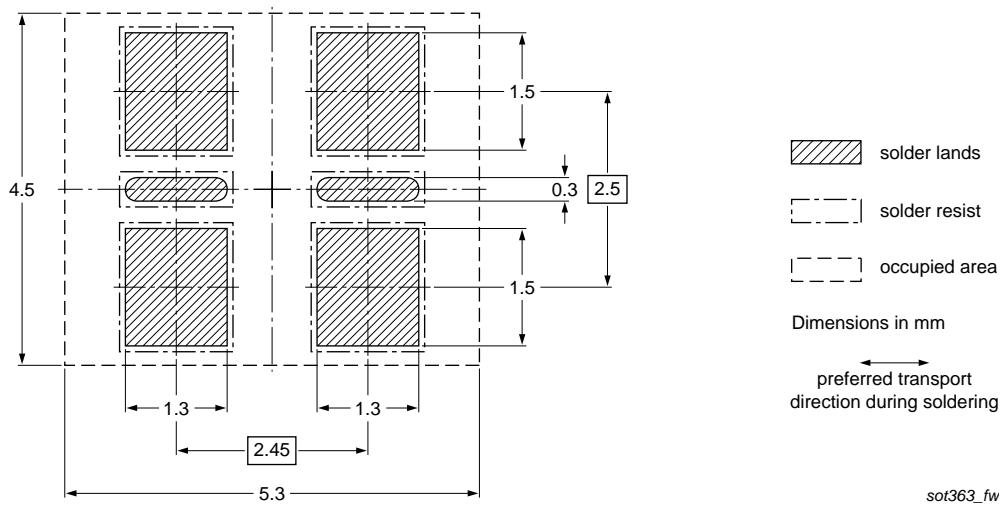


Fig 20. Wave soldering footprint for SOT363 (TSSOP6)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX7002AKS v.1	20120301	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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