AS5165

AUTOMOTIVE Angle Position Sensor with SENT J2716

1 General Description

The AS5165 is a contactless magnetic angle position sensor for accurate angular measurement over a full turn of 360°. A sub range can be programmed to achieve the best resolution for the application. It is a system-on-chip, combining integrated Hall elements, analog front end, digital signal processing and best in class automotive protection features in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip, is required. The magnet may be placed above or below the IC.

The absolute angle measurement provides instant indication of the magnet's angular position with a programmable resolution of 0.022° = 16384 positions per revolution. According to this resolution the adjustment of the application specific mechanical positions are possible. The angular output data is available over the SENT J2716 interface.

The AS5165 operates at a supply voltage of 5V and the supply and output pins are protected against overvoltage up to +27V. In addition the supply pins are protected against reverse polarity up to -18V.

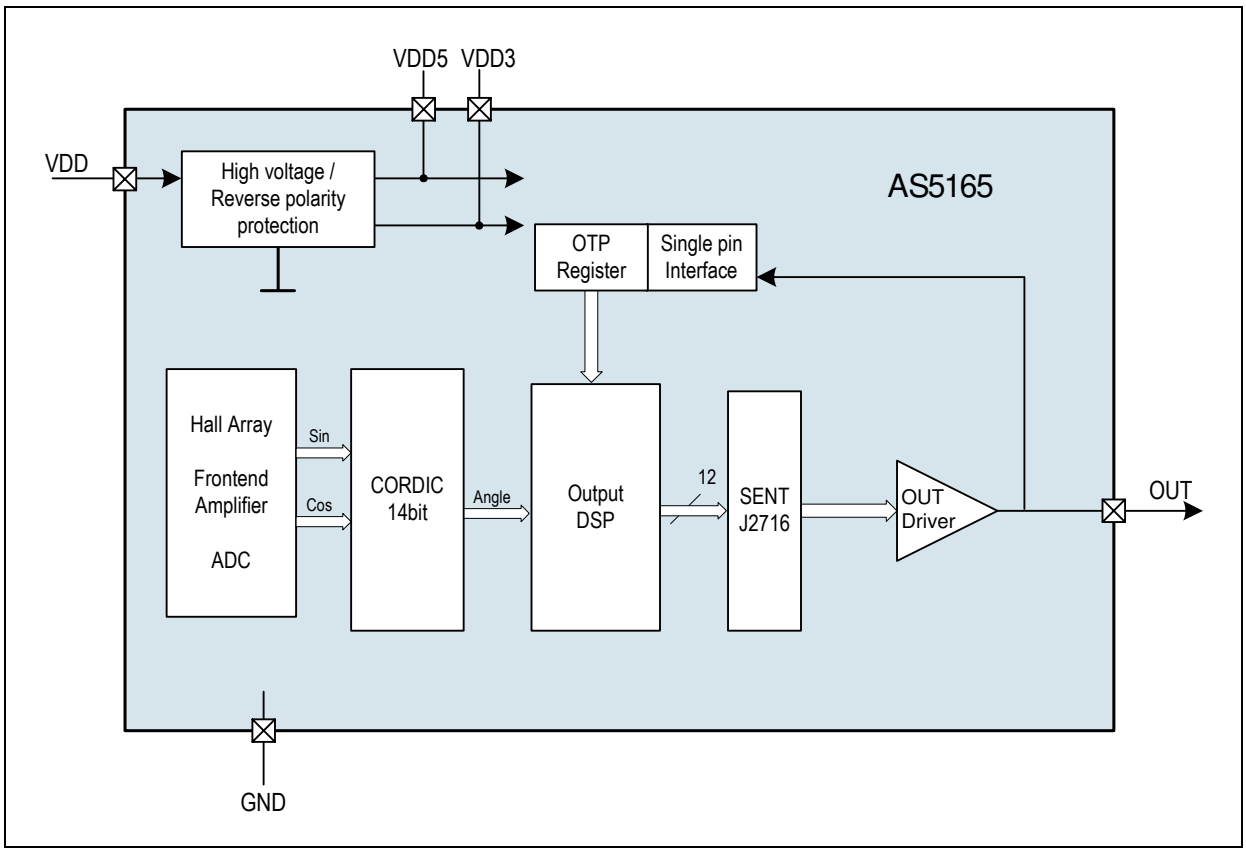
2 Key Features

- 360° contactless high resolution angular position encoding
- User programmable start and end point of the application region
- User programmable clamping levels and programming of the transition point
- Wide temperature range: - 40°C to + 150°C
- Small Pb-free package: TSSOP 14

3 Applications

The AS5165 is suitable for Automotive applications like throttle and valve position sensing and several power train applications.

Figure 1. AS5165 Block Diagram



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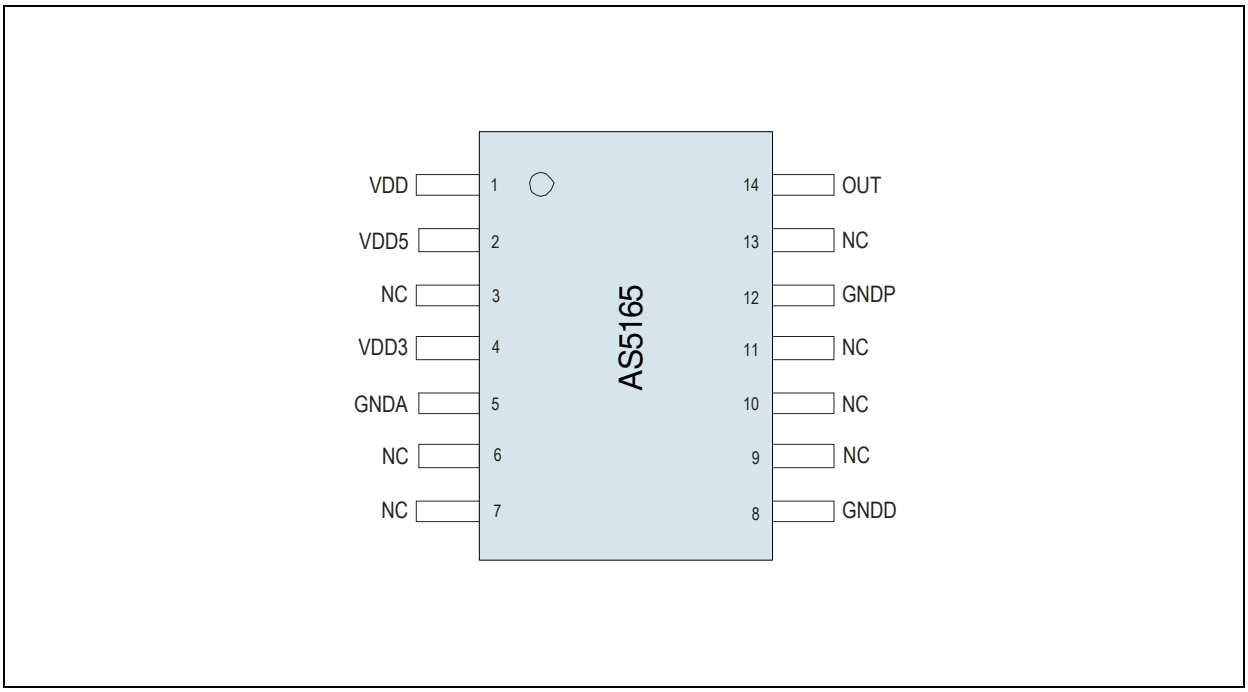
4 Pin Assignments

Figure 2. TSSOP-14 Pin Configuration



4.1 Pin Descriptions

Table 1. TSSOP-14 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
VDD	1	Supply pin	Positive supply pin. This pin is overvoltage protected.
VDD5	2	Supply pin	4.5V- Regulator output, internally regulated from VDD. This pin needs an external ceramic capacitor of 2.2 µF
NC	3	Multi purpose pin	Test pins for fabrication. Connected to ground in the application.
VDD3	4	Supply pin	3.45V- Regulator output, internally regulated from VDD5. This pin needs an external ceramic capacitor of 2.2 µF
GNDA	5	Supply pin	Analog ground pin. Connected to ground in the application.
NC	6	Multi purpose pin	Test pins for fabrication. Connected to ground in the application.
NC	7	Multi purpose pin	Test pins for fabrication. Open in the application.
GNDD	8	Supply pin	Digital ground pin. Connected to ground in the application.
NC	9	Multi purpose pin	Test pins for fabrication. Connected to ground in the application.
NC	10	Multi purpose pin	Test pins for fabrication. Connected to ground in the application.
NC	11	NC	Unconnected (not bonded)
GNDP	12	Supply pin	Analog ground pin. Connected to ground in the application.
NC	13	Multi purpose pin	Test pins for fabrication. Connected to ground in the application.
OUT	14	Multi purpose pin	SENT output pin.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
VDD	DC supply voltage at pin VDD Overvoltage	-18	27	V	No operation
VOUT	Output voltage OUT	-0.3	27	V	permanent
VDD3	DC supply voltage at pin VDD3	-0.3	5.5	V	
VDD5	DC supply voltage at pin VDD5	-0.3	7	V	
I_{SCR}	Input current (latchup immunity)	-100	100	mA	Norm: JEDEC 78
ESD	Electrostatic discharge		±4	kV	Norm: MIL 883 E method 3015 VDD, GND, OUT and KDOWN Pin. All other pins ±2 kV
T_{Strg}	Storage temperature	-55	150	ºC	Min -67ºF; Max +257ºF
T_{BODY}	Body temperature (Lead-free package)		260	ºC	t=20 to 40s, The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
H	Humidity non-condensing	5	85	%	

6 Electrical Characteristics

6.1 Operating Conditions

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TAMB	Ambient temperature	-40ºF…+302ºF	-40		+150	ºC
I_{SUPP}	Supply current				15	mA
VDD	Supply voltage at pin VDD	5V Operation	4.5	5.0	5.5	V
VDD3	Voltage regulator output voltage at pin VDD3		3.3	3.45	3.6	
VDD5	Voltage regulator output voltage at pin VDD5			4.5		

6.2 Magnetic Input Specification

TAMB = -40 to +150ºC, VDD5 = 4.5-5.5V (5V operation) unless otherwise noted.

Two-pole cylindrical diametrically magnetized source:

Table 4. Magnetic Input Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
d_{mag}	Diameter	Recommended magnet: Ø 6mm x 2.5mm for cylindrical magnets		6		mm
t_{mag}	Thickness		2.5			mm
B_{pk}	Magnetic input field amplitude	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm	30		70	mT
B_{off}	Magnetic offset	Constant magnetic stray field			±10	mT
	Field non-linearity	Including offset gradient			5	%
Disp	Displacement radius	Offset between defined device center and magnet axis (see Figure 25). Dependant on the selected magnet.		0.25	1	mm
Ecc	Eccentricity	Eccentricity of magnet center to rotational axis		100		µm
	Recommended magnet material and temperature drift	NdFeB (Neodymium Iron Boron)		-0.12		%/K
		SmCo (Samarium Cobalt)		-0.035		

6.3 Electrical System Specifications

T_{AMB} = -40 to +150ºC, VDD = 4.5-5.5V (5V operation) unless otherwise noted.

Table 5. Electrical System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution SENT Output				12	bit
INL_{opt}	Integral non-linearity (optimum) 360 degree full turn	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB} =25ºC. This is specified over 360 degrees. A sub range may improve the non-linearity.			±0.5	deg
INL_{temp}	Integral non-linearity (optimum) 360 degree full turn	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB} = -40 to +150ºC. This is specified over 360 degrees. A sub range may improve the non-linearity.			±0.9	deg
INL	Integral non-linearity 360 degree full turn	Best line fit = $(Err_{max} – Err_{min}) / 2$ Over displacement tolerance with 6mm diameter magnet, without calibration, T_{AMB} = -40 to +150ºC. This is specified over 360 degrees. A sub range may improve the non-linearity			±1.4	deg
TN	Transition noise	1 sigma		0.06		Deg RMS
V_{ON}	Power-on reset thresholds On voltage; 300mV typical hysteresis	DC supply voltage 3.3V (VDD3)	1.37	2.2	2.9	V
V_{OFF}	Power-on reset thresholds Off voltage; 300mV typical hysteresis		1.08	1.9	2.6	
t_{PwrUp}	Power-up time				10	ms
t_{delay}	System propagation delay absolute output: delay of ADC, DSP and absolute interface	Fast mode, times 2 in slow mode			100	µs

Note: The INL performance is specified over the full turn of 360 degrees. An operation in an angle segment increases the accuracy. A two point linearization is recommended to achieve the best INL performance for the chosen angle segment.

6.4 Timing Characteristics

Table 6. Timing Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FRCOT	Internal Master Clock	±10%	4.05	4.5	4.95	MHz
TCLK	Interface Clock Time	TCLK = 1 / FRCOT		222.2		ns
T1	Bit first level			128		TCLK
T2	Bit second level			384		TCLK
TBIT	Bit Time			512		TCLK
START	Packet start			1		TBIT
PACKET	Packet			20		TBIT
IDLE	Idle Time			1		TBIT
TSW	Switch Time			10		TBIT
TDETWD	WatchDog error detection time				12	ms

7 Detailed Description

The AS5165 is manufactured in a CMOS process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip.

The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5165 provides accurate high-resolution absolute angular position information. For this purpose, a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs that indicate movements of the used magnet towards or away from the device's surface.

A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information (see Figure 24).

The AS5165 senses the orientation of the magnetic field and calculates a 14-bit binary code. This code is mapped to a programmable output characteristic. A 12-bit output data and diagnostic bits are transmitted by the SENT J2716 output. This signal is available at the pin 14 (OUT).

The SENT output can be configured in many ways. The application angular region can be programmed in a user friendly way. The start angle position T1 and the end point T2 can be set and programmed according the mechanical range of the application with a resolution of 14 bits. In addition, the T1Y and T2Y parameter can be set and programmed according to the application. The transition point 0 to 360 degree can be shifted using the break point parameter BP. This point is programmable with a high resolution of 14 bits of 360 degrees. The voltage for clamping level low CLL and clamping level high CLH can be programmed with a resolution of 8 bits. Both levels are individually adjustable.

The AS5165 is configured by default in the single secure sensor format described in Appendix (Section A.3) of SAE-J2716 definition. It is possible to program the device to implement the Single Sensor format described in Appendix (Section A.4) of the SAE-J2716. This selection is programmed by the RollCnt user bit.

The output parameters can be programmed in an OTP register. No additional voltage is required to program the AS5165. The setting may be overwritten at any time and will be reset to default when power is cycled. To make the setting permanent, the OTP register must be programmed by using a lock bit and the content could be frozen for ever.

The AS5165 is tolerant to magnet misalignment and unwanted external magnetic fields due to differential measurement technique and Hall sensor conditioning circuitry.

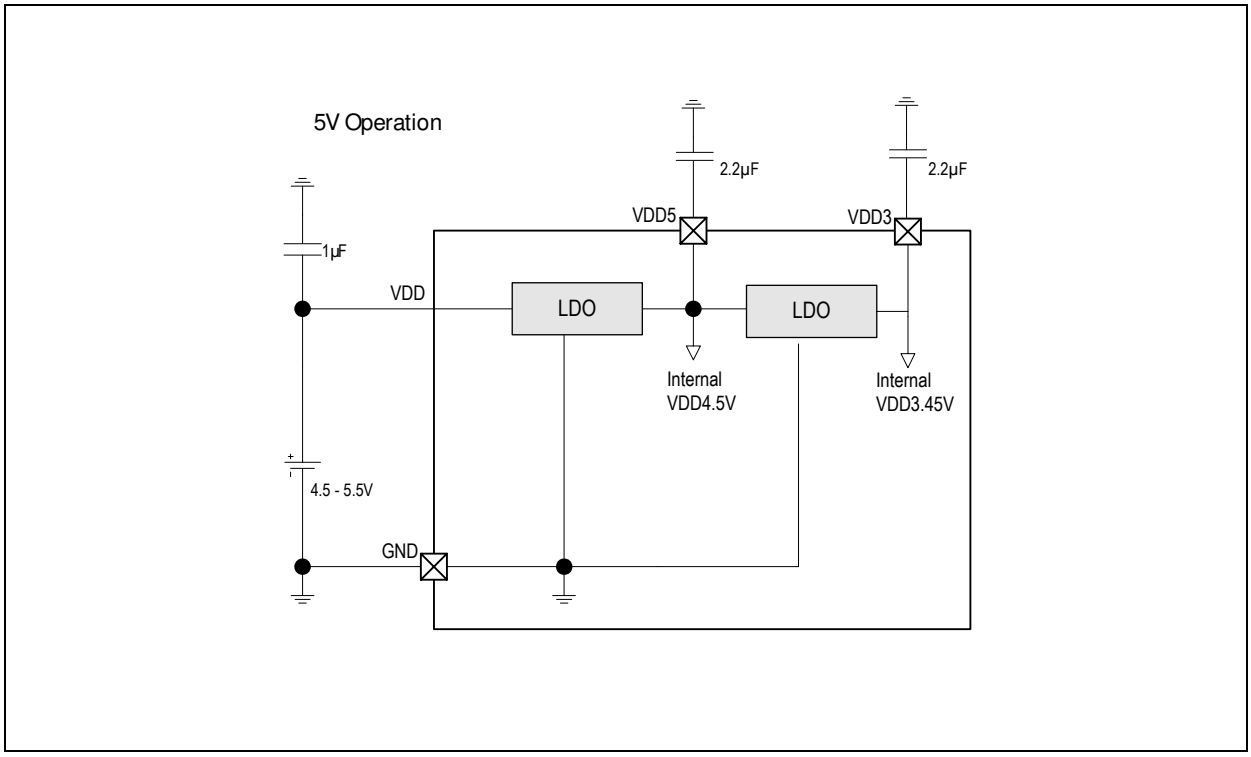
Figure 3. Typical Arrangement of AS5165 and Magnet

7.1 Operation

The AS5165 operates at 5V ±10%, using two internal Low-Dropout (LDO) voltage regulators. For operation, the 5V supply is connected to pin VDD. While VDD3 and VDD5 (LDO outputs) must be buffered by 2.2µF capacitors, the VDD requires a 1µF capacitor. All capacitors (low ESR ceramic) are supposed to be placed close to the supply pins (see Figure 4).

The VDD3 and VDD5 outputs are intended for internal use only. It must not be loaded with an external load.

Figure 4. Connections for 5V Supply Voltages



Note: The pins VDD3 and VDD5 must always be buffered by a capacitor. It must not be left floating, as this may cause instable internal supply voltages which may lead to larger output jitter of the measured angle.

The supply pins are overvoltage protected up to 27V. In addition, the device has a reverse polarity protection.

7.1.1 VDD Voltage Monitor

VDD Overvoltage Management. If the voltage applied to the VDD pin exceeds the overvoltage upper threshold for longer than the detection time, then the device enters a low power mode reducing the power consumption. When the overvoltage event has passed and the voltage applied to the VDD pin falls below the overvoltage lower threshold for longer than the recovery time, then the device enters the normal mode.

VDD5 Undervoltage Management. When the voltage applied to the VDD5 pin falls below the undervoltage lower threshold for longer than the VDD5_detection time, then the device stops the clock of the digital part and the output drivers are turned off to reduce the power consumption. When the voltage applied to the VDD5 pin exceeds the VDD5 undervoltage upper threshold for longer than the VDD5_recovery time, then the clock is restarted and the output drivers are turned on.

7.2 Output Characteristic

The pin OUT provides the SENT output format with a push/pull output driver.

The DSP maps the application range to the output characteristic. An inversion of the slope is also programmable to allow inversion of the rotation direction.

7.2.1 Programming Parameters

The analog output voltage modes are programmable by OTP. Depending on the application, the analog output can be adjusted. The user can program the following application specific parameters:

T1	Mechanical angle start point
T2	Mechanical angle end point
T1C	Output code at the T1 position
T2C	Output code at the T2 position
CLL	Clamping Level Low
CLH	Clamping Level High
BP	Break point (transition point 0 to 360 degree)

These parameters are input parameters. The parameters are converted over the provided programming software and programmer and finally written into the AS5165 128 bit OTP memory.

7.2.2 Application Specific Angular Range Programming

The application range can be selected by programming T1 with a related T1C and T2 with a related T2C into the AS5165. The internal gain factor is calculated automatically. The clamping levels CLL and CLH can be programmed independent from the T1 and T2 position and both levels can be separately adjusted.

Figure 5. Programming of an Individual Application Range

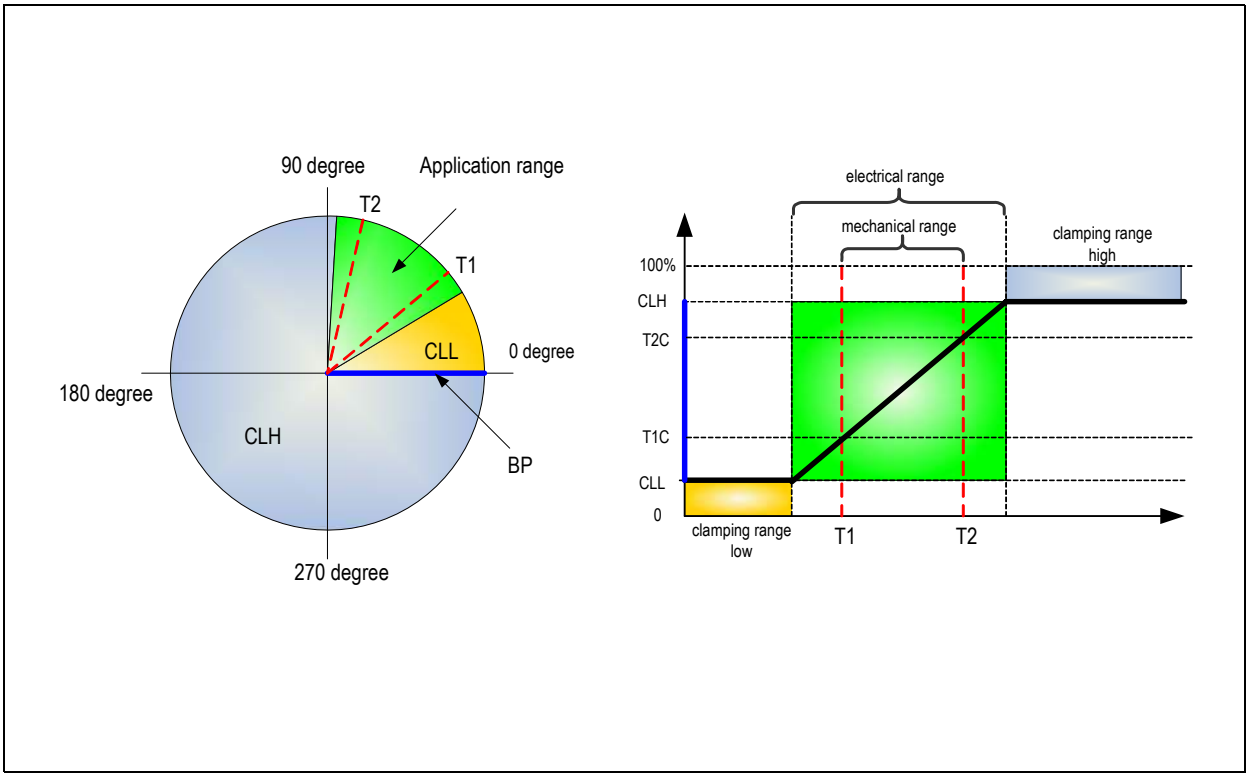
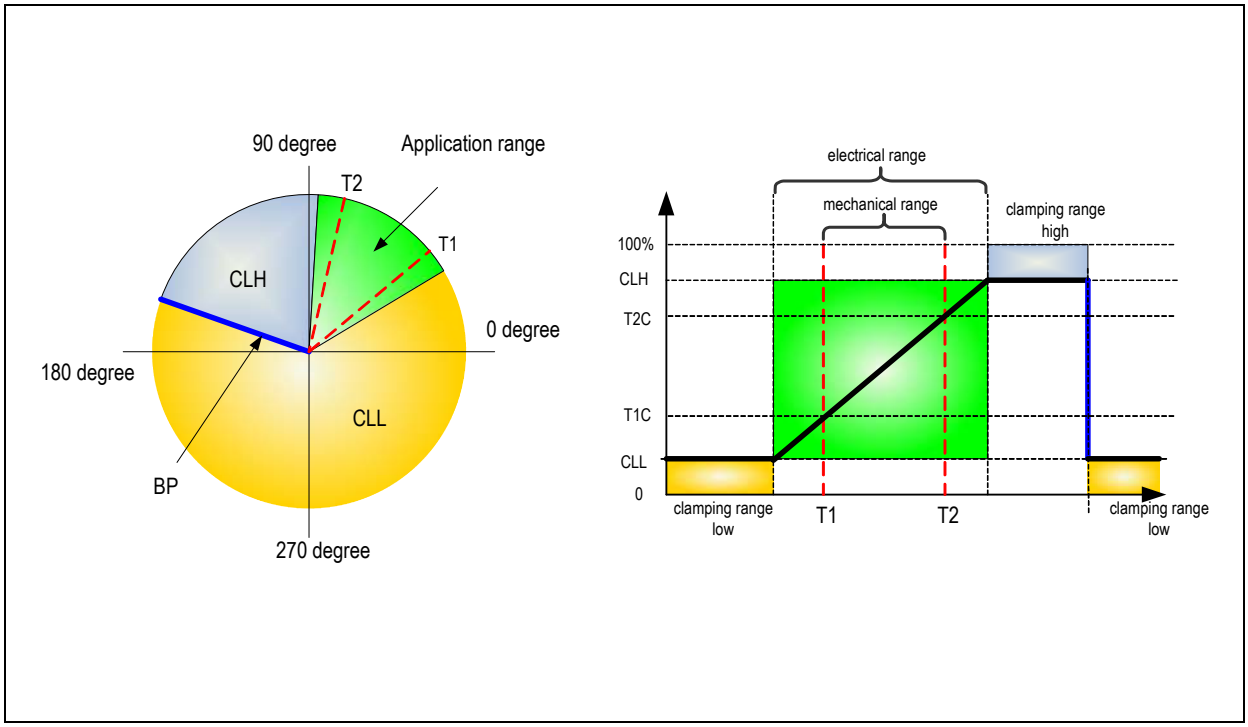


Figure 5 shows a simple example of the selection of the range. The mechanical starting point T1 and the mechanical end point T2 are defining the mechanical range. A sub range of the internal Cordic output range is used and mapped to the needed output characteristic. The output signal has 12-bit, hence the level T1C and T2C can be adjusted with this resolution. As a result of this level and the calculated slope, the clamping region low is defined. The break point BP defines the transition between CLL and CLH. In this example, the BP is set to 0 degree. The BP is also the end point of the clamping level high CLH. This range is defined by the level CLH and the calculated slope. Both clamping levels can be set independently form each other. The minimum application range is 10 degrees. In addition, the BP parameter specifies the used sector. The BP parameter must be set outside of the application range.

7.2.3 Application Specific Programming of the Break Point

The break point BP can be programmed as well with a resolution of 14 bits. This is important when the default transition point is inside the application range. In such a case, the default transition point must be shifted out of the application range. The parameter BP defines the new position. The function can be used also for an on-off indication.

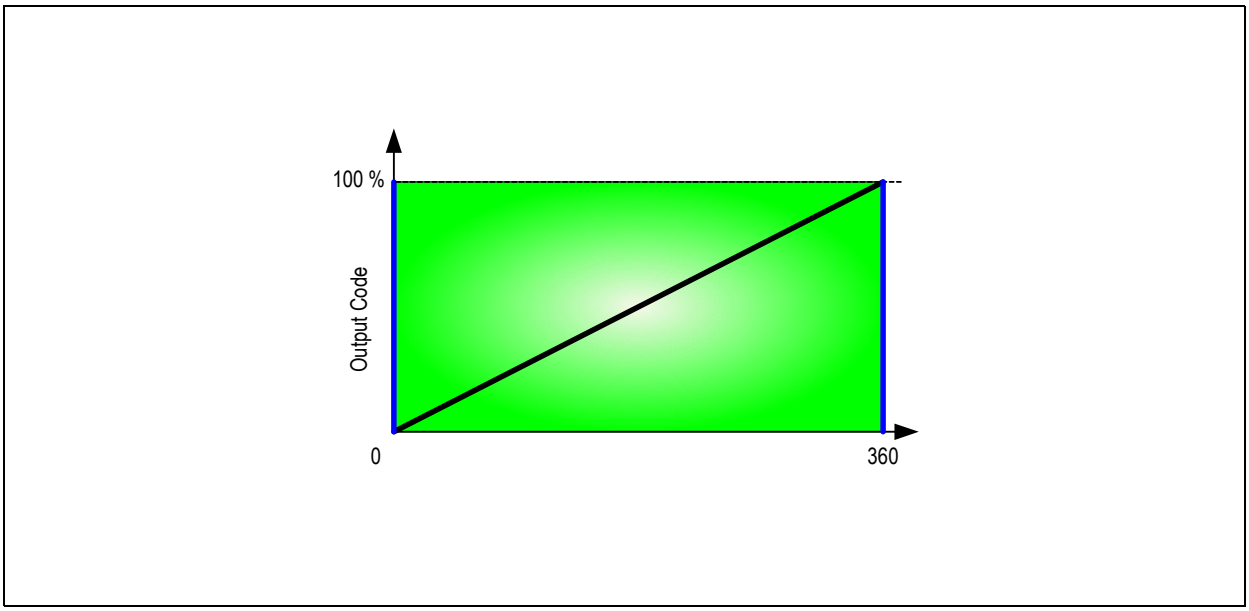
Figure 6. Individual Programming of the Break Point BP



7.2.4 Full Scale Mode

Without programming the parameters T1 and T2, the AS5165 is in the full scale mode.

Figure 7. Full Scale Mode



For simplification, Figure 7 describes a linear output format. Due to the digital output, a rail to rail operation is possible. (as indicated Figure 7).

7.2.5 Resolution of the Parameters

The programming parameters have a wide resolution up to 14 bits.

Table 7. Resolution of the Programming Parameters

Symbol	Parameter	Resolution	Note
T1	Mechanical angle start point	14 bits	000h – FFFh
T2	Mechanical angle stop point	14 bits	000h – FFFh
T1C	Output Code at mechanical start point	12 bits	000h – 3FFh
T2C	Output Code at mechanical end point	12 bits	000h – 3FFh
CLL	Clamping level low	8 bits	4080 LSBs is the maximum level
CLH	Clamping level high	8 bits	15 LSBs is the minimum level
BP	Break point	14 bits	000h – FFFh

Figure 8. Overview of the Angular Output Voltage

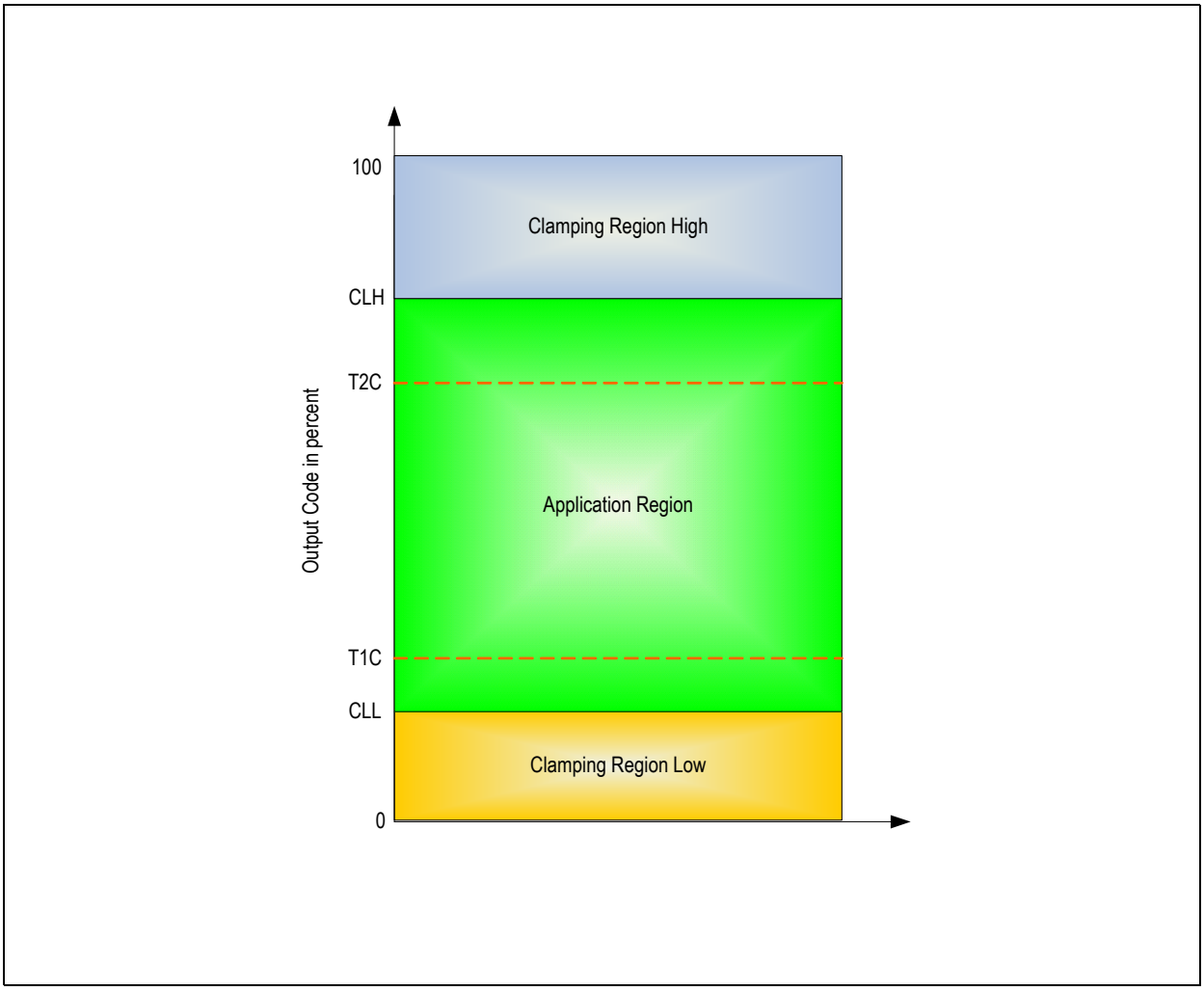


Figure 8 gives an overview of the different ranges.

7.2.6 SENT Output Driver Parameters

The output stage is configured in a push-pull output. Therefore it is possible to sink and source currents.

8 Application Information

The benefits of AS5165 are as follows:

- Unique fully differential patented solution
- Insensitive to external magnetic stray fields
- Best protections for automotive applications
- Easy to program
- Ideal for applications in harsh environments due to contactless position sensing
- Robust system, tolerant to magnet misalignment, air gap variations, temperature variations
- No calibration required because of inherent accuracy

8.1 Programming the AS5165

The AS5165 programming is a one-time-programming (OTP) method, based on polysilicon fuses. The advantage of this method is that no additional programming voltage is needed. The internal LDO provides the current for programming.

The OTP consists of 128 bits; several bits are available for user programming. In addition, the factory settings are stored in the OTP memory. Both regions are independently lockable by built-in lock bits.

A single OTP cell can be programmed only once. By default, the cell is “0”; a programmed cell will contain a “1”. While it is not possible to reset a programmed bit from “1” to “0”, multiple OTP writes are possible, as long as only unprogrammed “0”-bits are programmed to “1”.

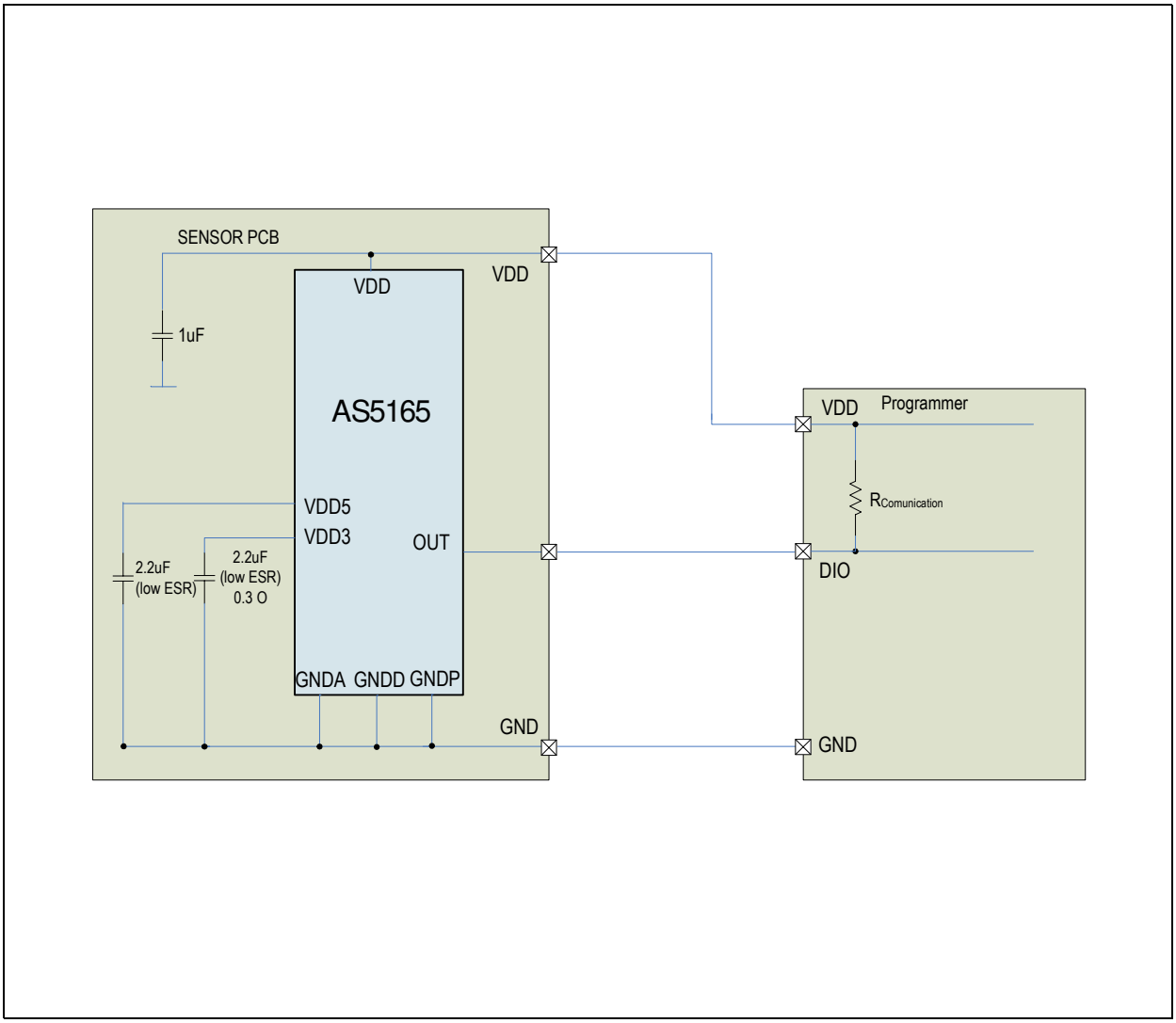
Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command. This is possible only if the user lock bit is not programmed.

Due to the programming over the output pin, the device will initially start in the communication mode. In this mode the digital angle value can be read with a specific protocol format. It is a bidirectional communication possible. Parameters can be written into the device. A programming of the device is triggered by a specific command. With another command (pass2func) the device can be switched into operation mode. In case of a programmed user lock bit, the AS5165 automatically starts up in the functional operation mode. No communication of the specific protocol is possible after this.

8.1.1 Hardware Setup

For OTP memory access, the pin OUT and the supply connection is required. Without the programmed Mem_Lock_USER OTP bit, the device will start up in the communication mode and will remain into an IDLE operation mode. The pull up resistor $R_{Communication}$ is required during startup.

Figure 9. Programming Schematic of the AS5165



8.1.2 Protocol Timing and Commands of Single Pin Interface

During the communication mode, the output level is defined by the external pull up resistor $R_{Communication}$. The output driver of the device is in tri-state. The bit coding (shown in Figure 10) has been chosen in order to allow the continuous synchronization during the communication, which can be required due to the tolerance of the internal clock frequency. Figure 10 shows how the different logic states '0' and '1' are defined. The period of the clock T_{CLK} is defined with 222.2 ns.

The voltage levels V_H and V_L are CMOS typical.

Each frame is composed by 20 bits. The 4 MSB (CMD) of the frame specifies the type of command that is passed to the AS5165. 16 data bits contain the communication data. There will be no operation in case of the usage of a not specified CMD. The sequence is oriented in a way that the LSB of the data is coming first followed by the command. Depending on the command the number of frames is different. The single pin programming interface block of the AS5165 can operate in slave communication or master communication mode. In the slave communication mode, the AS5165 receives the data organized in frames. The programming tool is the driver of the single communication line and can pull down the level. In case of the master communication mode, the AS5165 transmits data in the frame format. The single communication line can be pulled down by the AS5165.

Figure 10. Bit Coding of the Single Pin Programming Interface

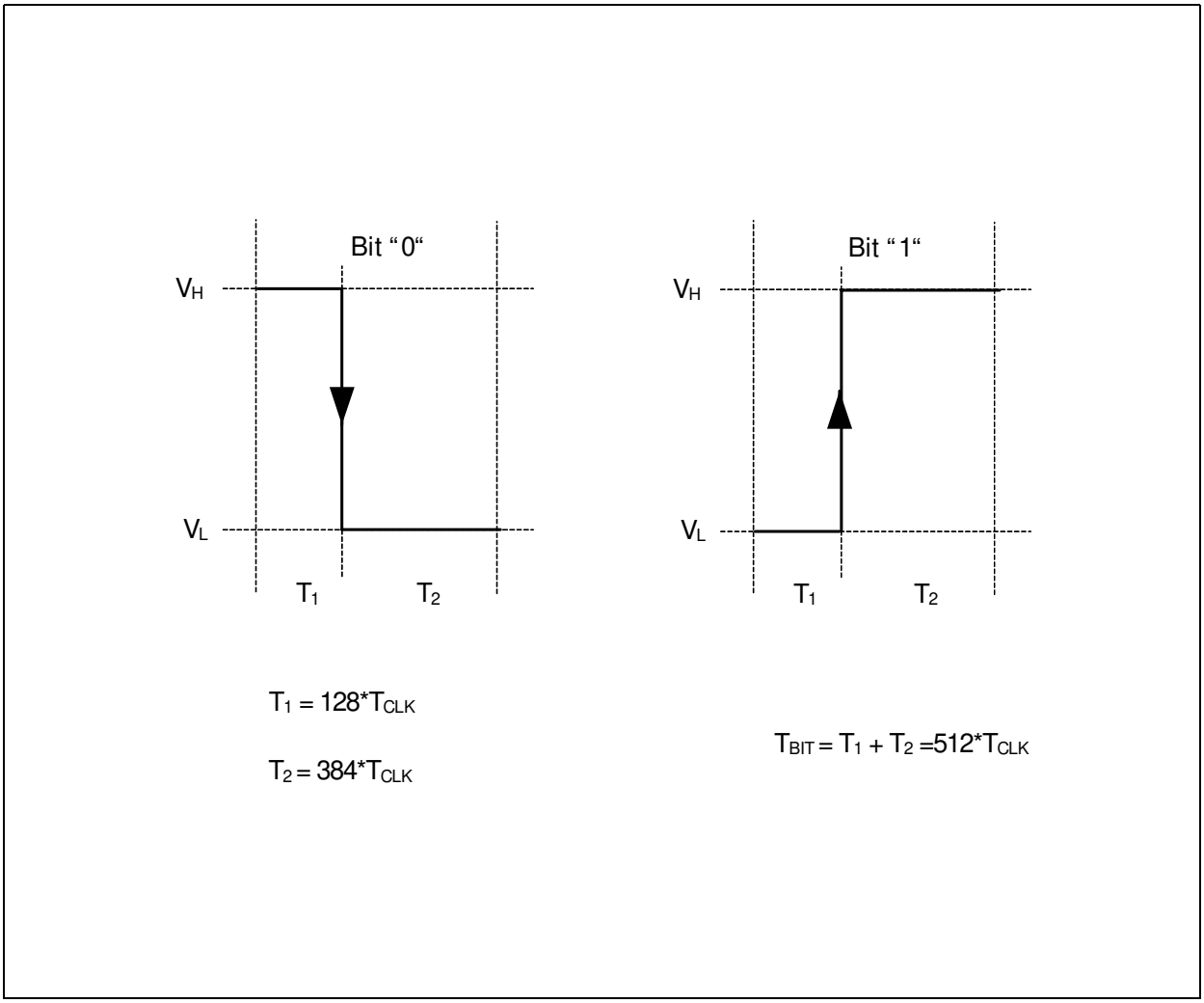


Figure 11. Protocol Definition

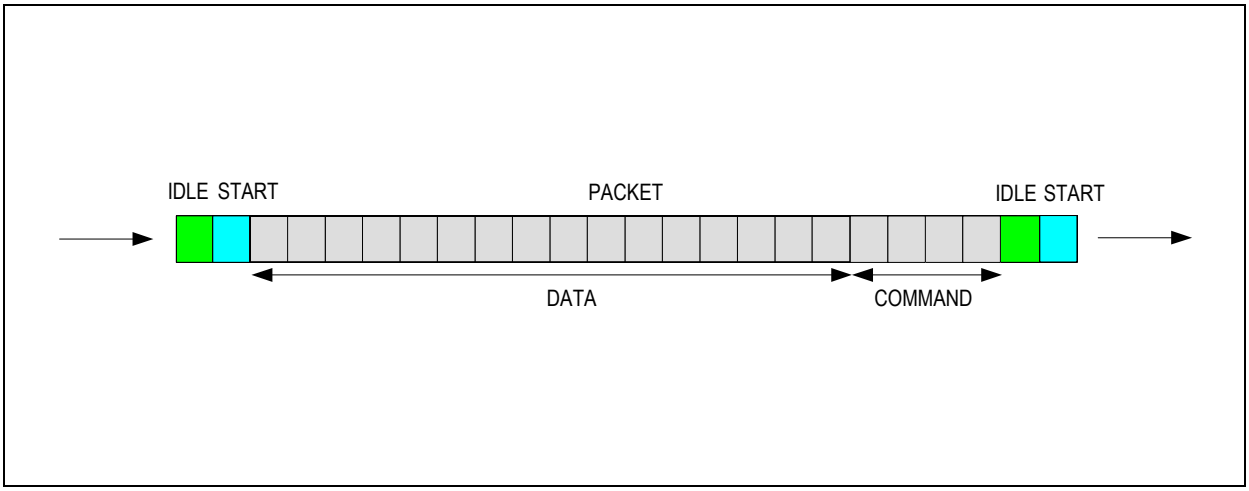


Table 8. OTP Commands and Communication Interface Modes

Possible Interface Commands	Description	AS5165 Communication Mode	Command CMD	Number of Frames
UNBLOCK	Resets the interface	SLAVE	0x0	1
WRITE128	Writes 128 bits (user+ factory settings) into the device	SLAVE	0x9 (0x1)	8
READ128	Read 128 bits (user+ factory settings) from the device	SLAVE and MASTER	0xA	9
UPLOAD	Transfers the register content into the OTP memory	SLAVE	0x6	1
DOWNLOAD	Transfers the OTP content to the register content	SLAVE	0x5	1
FUSE	Command for permanent programming	SLAVE	0x4	1
PASS2FUNC	Change operation mode from communication to operation	SLAVE	0x7	1
READ	Read related to address the user data	SLAVE and MASTER	0xB	2
WRITE	Write related to address the user data	SLAVE	0xC	1

Note: The command CMD 0x2 is reserved for AMS test purpose.

When single pin programming interface bus is in high impedance state, the logical level of the bus is held by the pull up resistor $R_{Communication}$. Each communication begins by a condition of the bus level which is called START. This is done by forcing the bus in logical low level (done by the programmer or AS5165 depending on the communication mode). Afterwards the bit information of the command is transmitted as shown in Figure 12.

Figure 12. Bus Timing for the WRITE128 Command

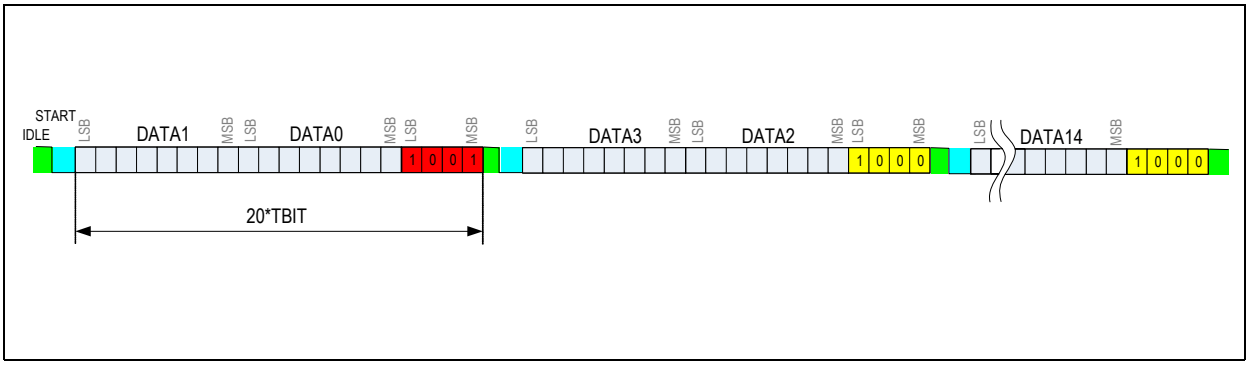
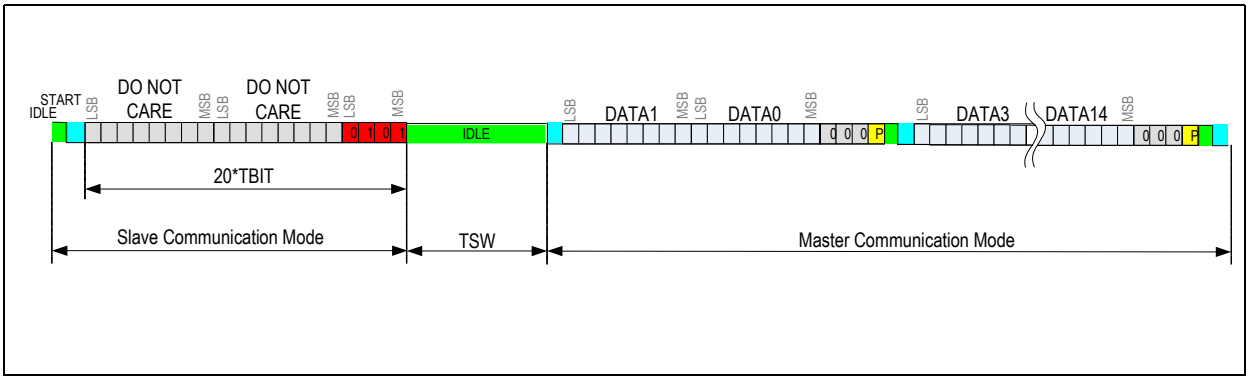
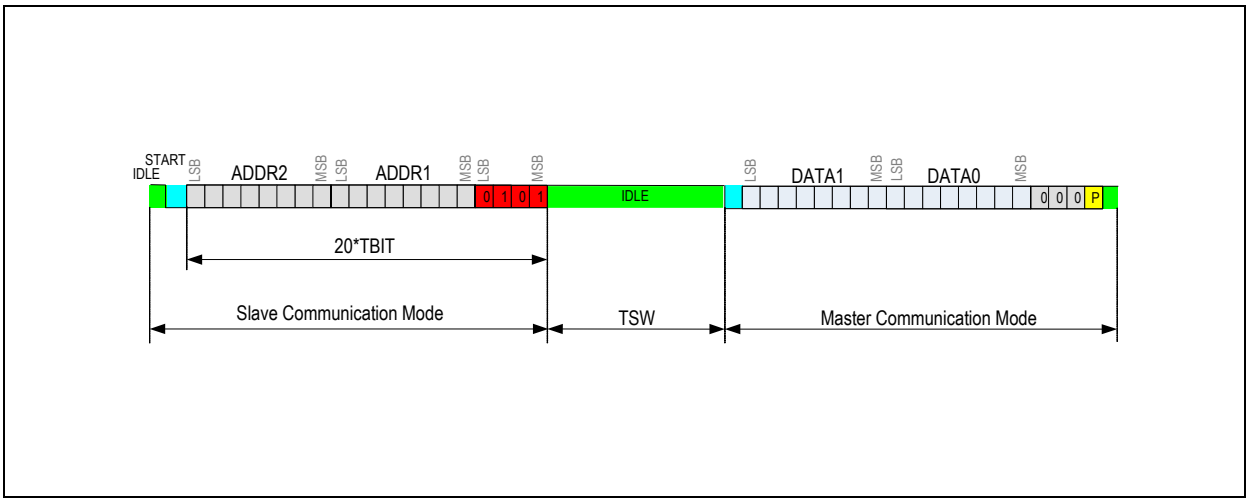


Figure 13. Bus Timing for the READ128 Command



In case of READ or READ128 command (Figure 13) the idle phase between the command and the answer is 10 TBIT (TSW).

Figure 14. Bus Timing for the READ Commands



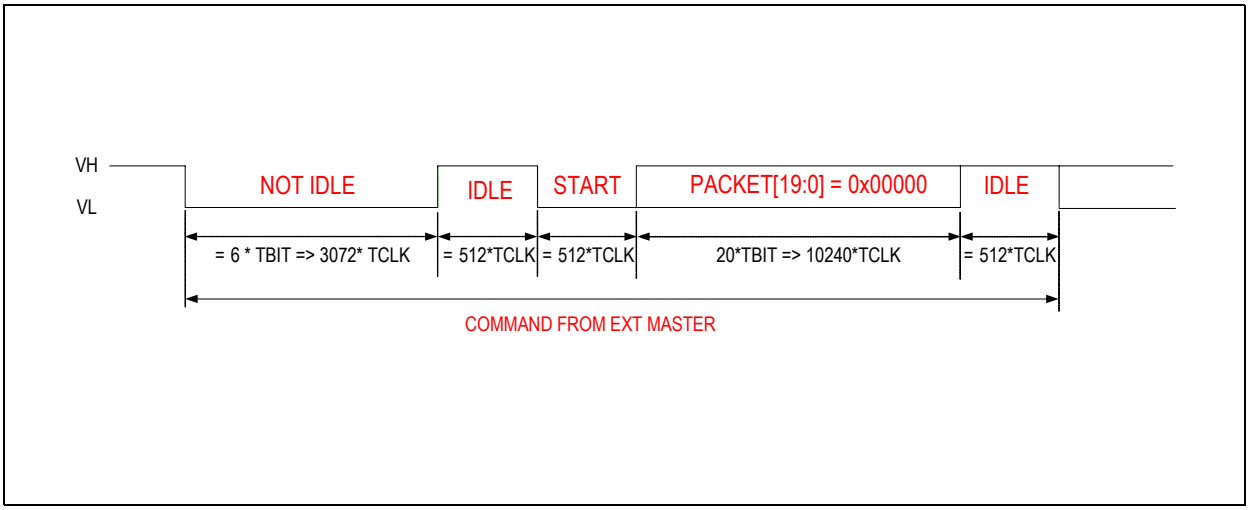
In case of a WRITE command, the device stays in slave communication mode and will not switch to master communication mode.

When using other commands like DOWNLOAD, UPLOAD, etc. instead of READ or WRITE, it does not matter what is written in the address fields (ADDR1, ADDR2).

Unblock. The Unblock command can be used to reset only the one-wire interface of the AS5165 in order to recover the possibility to communicate again without the need of a POR after a stacking event due to noise on the bus line or misalignment with the AS5165 protocol.

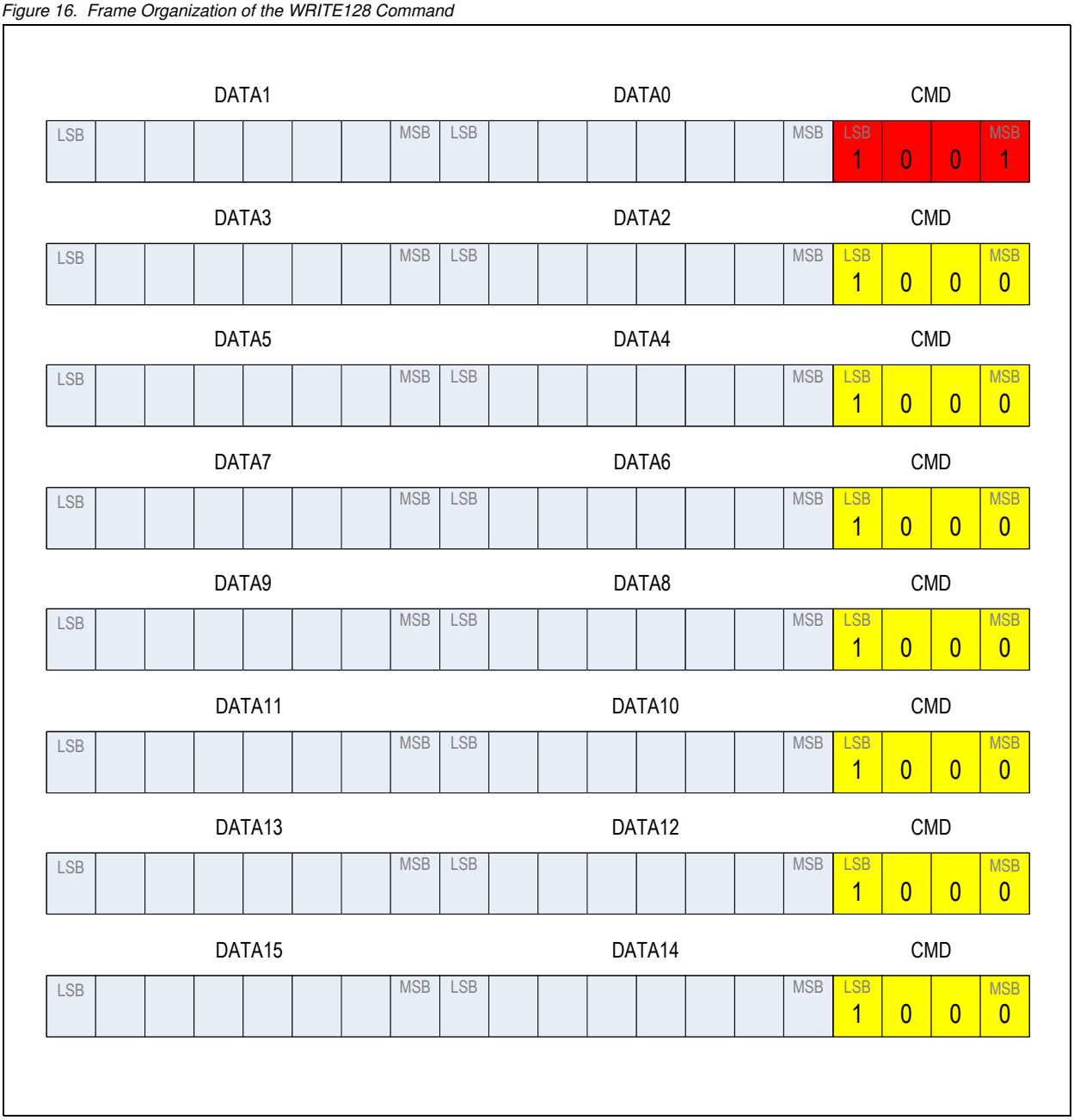
The command is composed by a not idle phase of at least 6 TBIT followed by a packet with all 20 bits at zero (see Figure 15).

Figure 15. Unblock Sequence



WRITE128. Figure 16 shows the format of the frame and the command.

Figure 16. Frame Organization of the WRITE128 Command



The command contains 8 frames. With this command the AS5165 is only receiving frames. This command will transfer the data in the special function registers (SFRs) of the device. The data is not permanent programmed using this command.

Table 9 describes the organization of the OTP data bits.

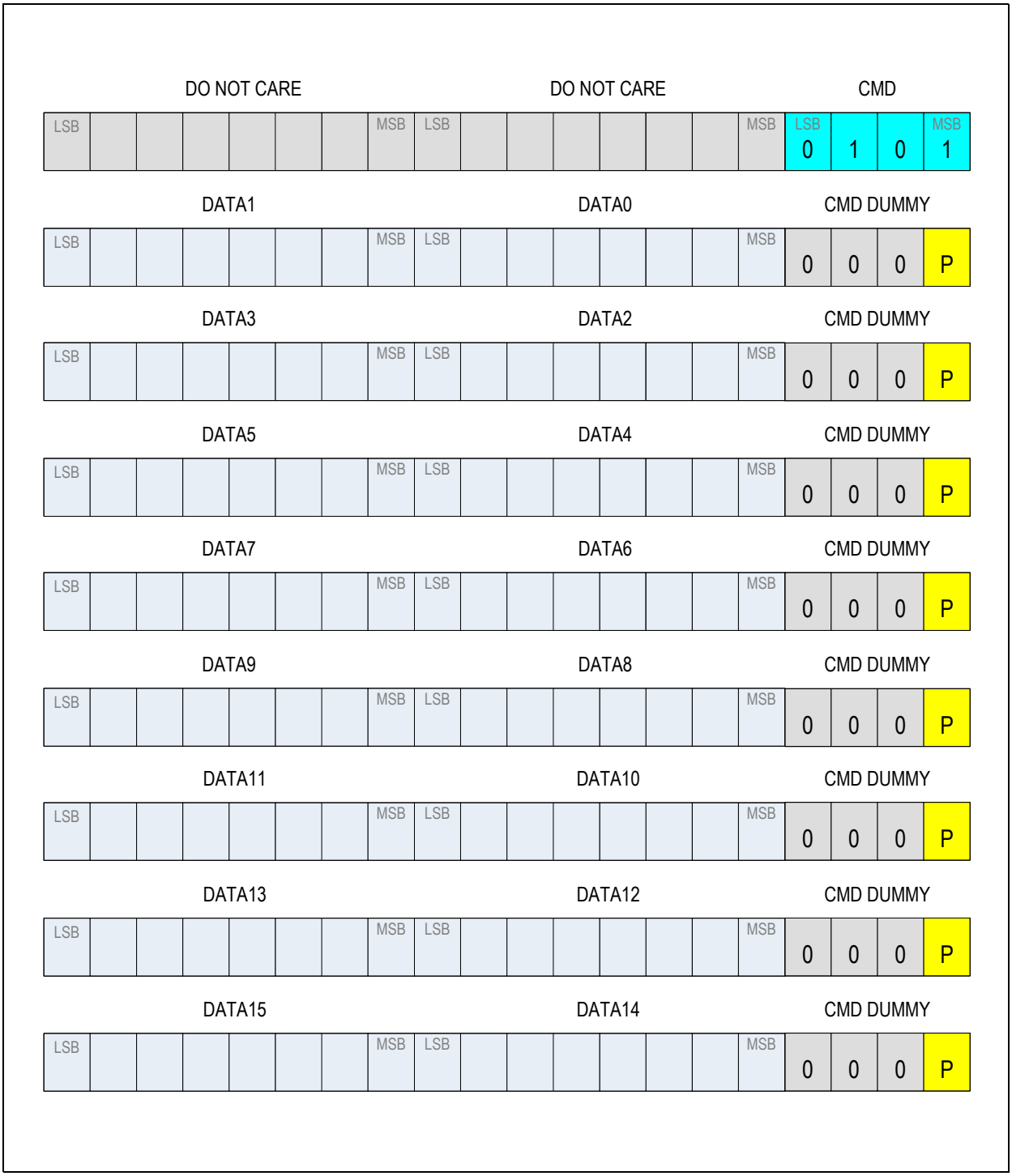
The access is performed with CMD field set to 0x9. The next 7 frames with CMD field set to 0x1. The 2 bytes of the first command will be written at address 0 and 1 of the SFRs, the 2 bytes of the second at address 2 and 3 and so on in order to cover all the 16 bytes of the 128 SFRs.

Note: It is important to always complete the command. All 8 frames are needed. In case of a wrong command or a communication error a power on reset must be performed.

The device will be delivered with the programmed Mem_Lock_AMS OTP bit. This bit locks the content of the factory settings. It is impossible to overwrite this particular region. The written information will be ignored.

READ128. Figure 17 shows the format of the frame and the command.

Figure 17. Frame Organization of the READ128 Command

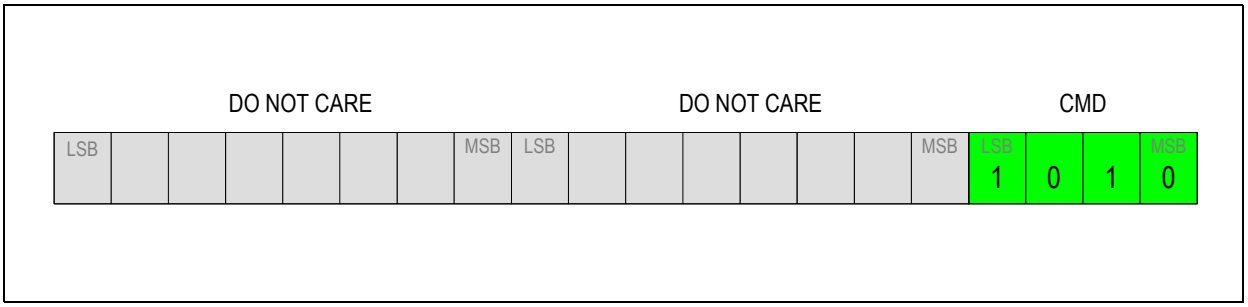


The command is composed by a first frame transmitted to the AS5165. The device is in slave communication mode. The device remains for the time TSW_{ITCH} in IDLE mode before changing into the master communication mode. The AS5165 starts to send 8 frames. This command will read the SFRs. The numbering of the data bytes correlates with the address of the related SFR.

An even parity bit is used to guarantee a correct data transmission. Each parity (P) is related to the frame data content of the 16 bit word. The MSB of the CMD dummy (P) is reserved for the parity information.

DOWNLOAD. Figure 18 shows the format of the frame.

Figure 18. Frame Organization of the DOWNLOAD Command

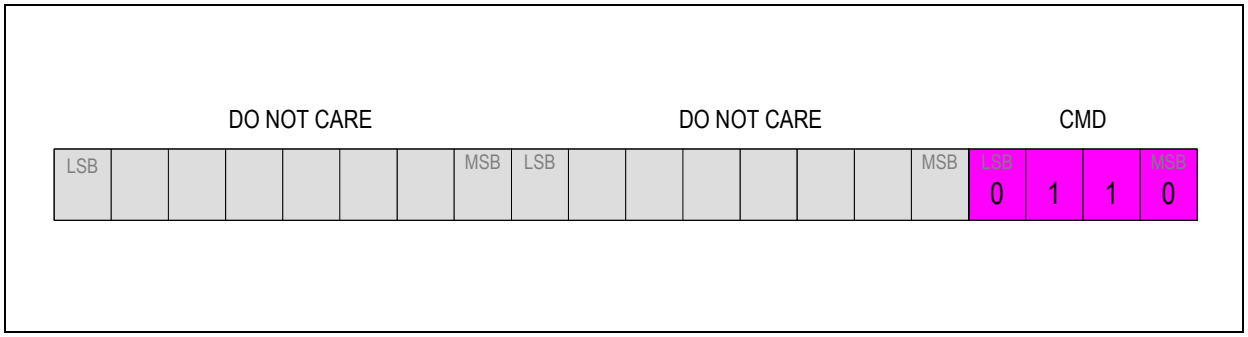


The command consists of one frame received by the AS5165 (slave communication mode). The OTP cell fuse content will be downloaded into the SFRs.

The access is performed with CMD field set to 0x5.

UPLOAD. Figure 19 shows the format of the frame.

Figure 19. Frame Organization of the UPLOAD Command

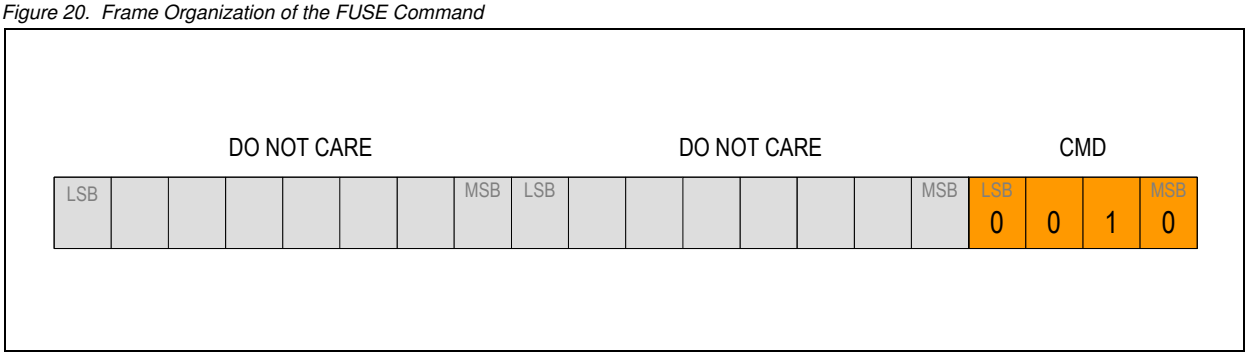


The command consists of one frame received by the AS5165 (slave communication mode) and transfers the data from the SFRs into the OTP fuse cells. The OTP fuses are not permanent programmed using this command.

The access is performed with CMD field set to 0x6.

FUSE. Figure 20 shows the format of the frame.

Figure 20. Frame Organization of the FUSE Command



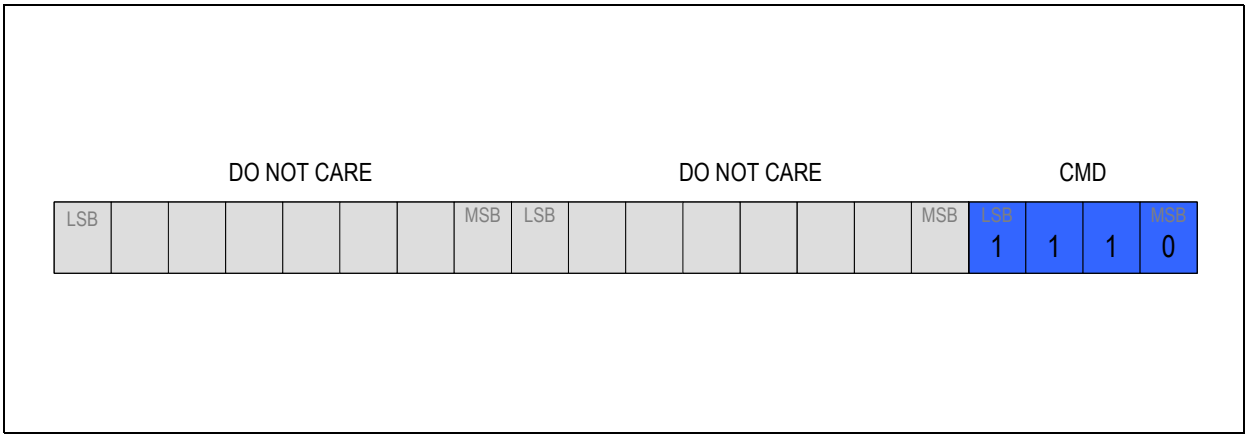
The command consists of one frame received by the AS5165 (slave communication mode) and it is giving the trigger to permanent program the non volatile fuse elements.

The access is performed with CMD field set to 0x4.

Note: After this command, the device automatically starts to program the built-in programming procedure. It is not allowed to send other commands during this programming time. This time is specified to 4ms after the last CMD bit.

PASS2FUNC. Figure 21 shows the format of the frame.

Figure 21. Frame Organization of the PASS2FUNC Command

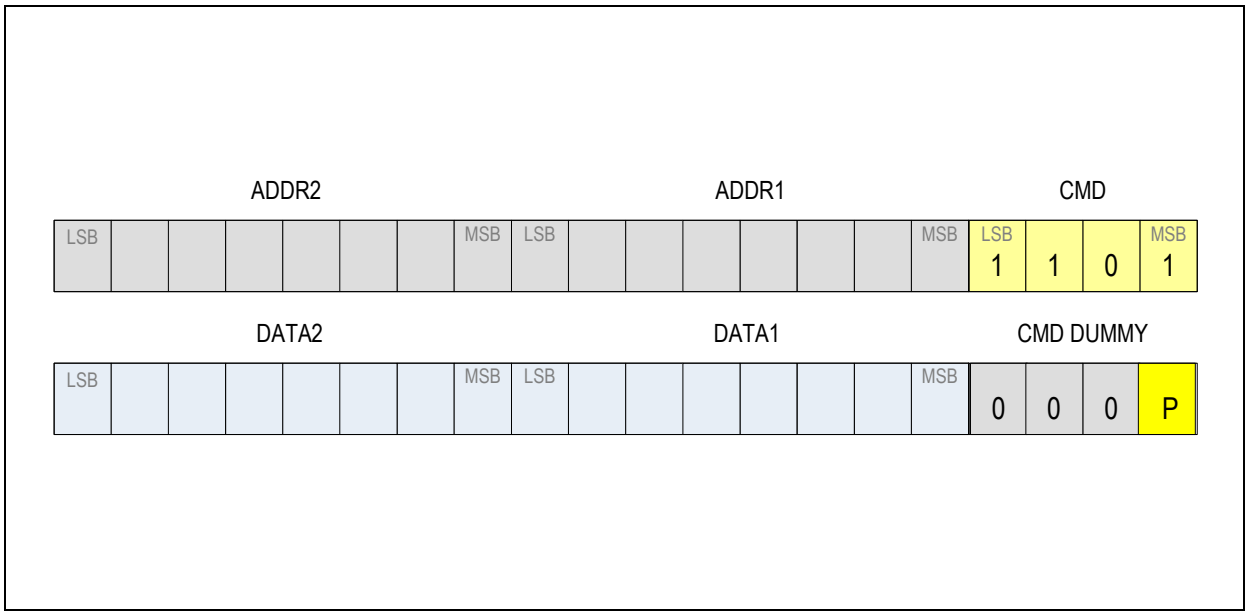


The command consists of one frame received by the AS5165 (slave communication mode). This command stops the communication receiving mode, releases the reset of the DSP of the AS5165 device and starts to work in functional mode with the values of the SFR currently written.

The access is performed with CMD field set to 0x7.

READ. Figure 22 shows the format of the frame.

Figure 22. Frame Organization of the READ Command



The command is composed by a first frame sent to the AS5165. The device is in slave communication mode. The device remains for the time T_{SWITCH} in IDLE mode before changing into the master communication mode. The AS5165 starts to send the second frame transmitted by the AS5165.

The access is performed with CMD field set to 0xB.

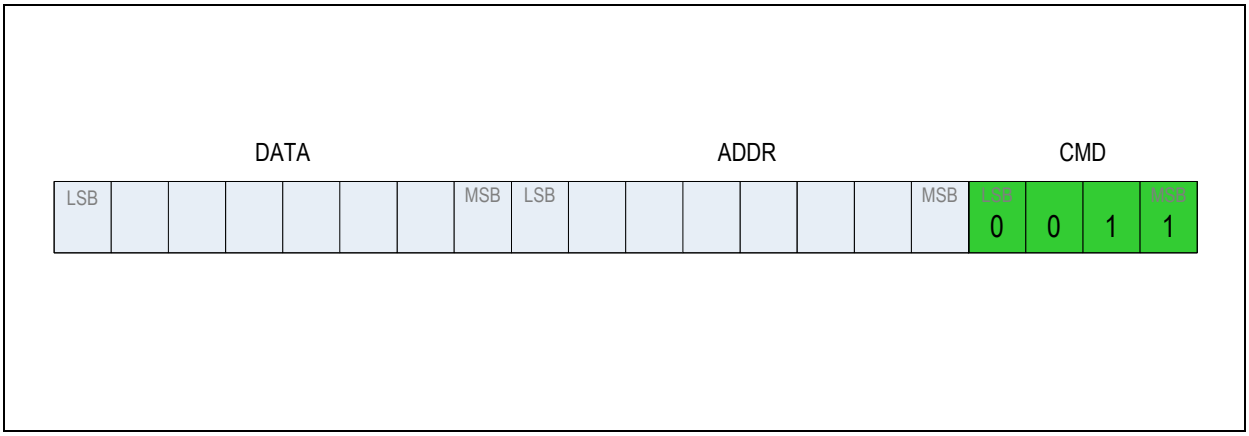
When the AS5165 has received the first frame, it sends a frame with data value of the address specified in the field of the first frame.

Table 10 shows the possible readable data information for the AS5165 device.

An even parity bit is used to guarantee a correct data transmission. The parity bit (P) is generated by the 16 data bits. The MSB of the CMD dummy (P) is reserved for the parity information.

WRITE. Figure 23 shows the format of the frame.

Figure 23. Frame Organization of the WRITE Command



The command consists of one frame received by the AS5165 (slave communication mode). The data byte will be written to the address. The access is performed with CMD field set to 0xC.

Table 10 shows the possible write data information for the AS5165 device.

Note: It is not recommended to access OTP memory addresses using this command.

8.2 OTP Programming Data

Table 9. OTP Data Organization

Data Byte	Bit Number	Symbol	Default	Description	
DATA15 (0x0F)	0	AMS_Test	FS	AMS Test area	Factory Settings
	1	AMS_Test	FS		
	2	AMS_Test	FS		
	3	AMS_Test	FS		
	4	AMS_Test	FS		
	5	AMS_Test	FS		
	6	AMS_Test	FS		
	7	AMS_Test	FS		
DATA14 (0x0E)	0	AMS_Test	FS		
	1	AMS_Test	FS		
	2	AMS_Test	FS		
	3	AMS_Test	FS		
	4	ChipID<0>	FS	Chip ID	Customer Settings
	5	ChipID<1>	FS		
	6	ChipID<2>	FS		
	7	ChipID<3>	FS		
DATA13 (0x0D)	0	ChipID<4>	FS		
	1	ChipID<5>	FS		
	2	ChipID<6>	FS		
	3	ChipID<7>	FS		
	4	ChipID<8>	FS		
	5	ChipID<9>	FS		
	6	ChipID<10>	FS		
	7	ChipID<11>	FS		
DATA12 (0x0C)	0	ChipID<12>	FS		
	1	ChipID<13>	FS		
	2	ChipID<14>	FS		
	3	ChipID<15>	FS		
	4	ChipID<16>	FS		
	5	ChipID<17>	FS		
	6	ChipID<18>	FS		
	7	ChipID<19>	FS		
DATA11 (0x0B)	0	ChipID<20>	FS		
	1	MemLock_AMS	1	Lock of the Factory Setting Area	

Table 9. OTP Data Organization

Data Byte	Bit Number	Symbol	Default	Description	
	2	KD<0>	0	Kick Down Threshold	Customer Settings
	3	KD<1>	0		
	4	KD<2>	0		
	5	KD<3>	0		
	6	KD<4>	0		
	7	KD<5>	0		
DATA10 (0x0A)	0	ClampLow<0>	0	Clamping Level Low	
	1	ClampLow<1>	0		
	2	ClampLow<2>	0		
	3	ClampLow<3>	0		
	4	ClampLow<4>	0		
	5	ClampLow<5>	0		
	6	ClampLow<6>	0		
	7	DITH_DISABLE	0	DAC12/DAC10 Mode	
DATA9 (0x09)	0	ClampHi<0>	0	Clamping Level High	
	1	ClampHi<1>	0		
	2	ClampHi<2>	0		
	3	ClampHi<3>	0		
	4	ClampHi<4>	0		
	5	ClampHi<5>	0		
	6	ClampHi<6>	0		
	7	DIAG_HIGH	0	Diagnostic Mode, default =0 for Failure Band Low	
DATA8 (0x08)	0	OffsetIn<0>	0	Offset	
	1	OffsetIn<1>	0		
	2	OffsetIn<2>	0		
	3	OffsetIn<3>	0		
	4	OffsetIn<4>	0		
	5	OffsetIn<5>	0		
	6	OffsetIn<6>	0		
	7	OffsetIn<7>	0		
DATA7 (0x07)	0	OffsetIn<8>	0		
	1	OffsetIn<9>	0		
	2	OffsetIn<10>	0		
	3	OffsetIn<11>	0		
	4	OffsetIn<12>	0		
	5	OffsetIn<13>	0		
	6	OP_Mode<0>	0	Selection of Analog, PWM or Digital Mode	
	7	OP_Mode<1>	0		

Table 9. OTP Data Organization

Data Byte	Bit Number	Symbol	Default	Description	
DATA6 (0x06)	0	OffsetOut<0>	0	Output Offset	Customer Settings
	1	OffsetOut<1>	0		
	2	OffsetOut<2>	0		
	3	OffsetOut<3>	0		
	4	OffsetOut<4>	0		
	5	OffsetOut<5>	0		
	6	OffsetOut<6>	0		
	7	OffsetOut<7>	0		
DATA5 (0x05)	0	OffsetOut<8>	0		
	1	OffsetOut<9>	0		
	2	OffsetOut<10>	0		
	3	OffsetOut<11>	0		
	4	KDHYS<0>	0	Kick Down Hysteresis	
	5	KDHYS<1>	0		
	6	PWM Frequency<0>	0	select the PWM frequency (4 frequencies)	
	7	PWM Frequency<1>	0		
DATA4 (0x04)	0	BP<0>	0	Break Point	
	1	BP<1>	0		
	2	BP<2>	0		
	3	BP<3>	0		
	4	BP<4>	0		
	5	BP<5>	0		
	6	BP<6>	0		
	7	BP<7>	0		
DATA3 (0x003)	0	BP<8>	0		
	1	BP<9>	0		
	2	BP<10>	0		
	3	BP<11>	0		
	4	BP<12>	0		
	5	BP<13>	0		
	6	FAST_SLOW	0	Output Data Rate	
	7	ALARM_DISABLE	0	Alarm Disable	
DATA2 (0x02)	0	Gain<0>	0	Gain	
	1	Gain<1>	0		
	2	Gain<2>	0		
	3	Gain<3>	0		
	4	Gain<4>	0		
	5	Gain<5>	0		

Table 9. OTP Data Organization

Data Byte	Bit Number	Symbol	Default	Description	
	6	Gain<6>	0	Gain	Customer Settings
	7	Gain<7>	0		
DATA1 (0x01)	0	Gain<8>	0		
	1	Gain<9>	0		
	2	Gain<10>	0		
	3	Gain<11>	0		
	4	Gain<12>	0		
	5	Gain<13>	0		
	6	Invert_slope	0	Clockwise/counterclockwise rotation	
	7	Lock_OTPCUST	0	Customer Memory Lock	
DATA0 (0x00)	0	redundancy<0>	0	Redundancy Bits	
	1	redundancy<1>	0		
	2	redundancy<2>	0		
	3	redundancy<3>	0		
	4	redundancy<4>	0		
	5	redundancy<5>	0		
	6	redundancy<6>	0		
	7	redundancy<7>	0		

Note: Factory settings (FS) are used for testing and programming at AMS. These settings are locked (only read access possible).

Data Content:

- Redundancy (7:0): For a better programming reliability, a redundancy is implemented. In case the programming of one bit fails, then this function can be used. With an address (7:0) one bit can be selected and programmed.
- Lock_OTPCUST = 1, locks the customer area in the OTP and the device is starting up from now on in operating mode.
- Invert_Slope = 1, inverts the output characteristic in analog output mode.
- Gain (7:0): With this value one can adjust the steepness of the output slope.
- EXT_RANGE = 1, provides a wider z-Range of the magnet by turning off the alarm function.
- FAST_SLOW = 1, improves the noise performance due to internal filtering.
- BP (13:0): The breakpoint can be set with resolution of 14-bit.
- OffsetOut (11:0): Output characteristic parameter
- OffsetIn (13:0): Output characteristic parameter
- DIAG_HIGH = 1: In case of an error, the signal goes into high failure-band.
- ClampHI (6:0) sets the clamping level high with respect to VDD.
- DITH_DISABLE disables filter at DAC.
- ClampLow (6:0) sets the clamping level low with respect to VDD.

8.2.1 Read / Write User Data

Table 10. Read / Write Data

Area Region	Address	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W User Data	0x10	16	CORDIC_OUT[7:0]							
	0x11	17	0	0	CORDIC_OUT[13:8]					
	0x12	18	OCF	COF	0	0	0	0	DSP_RES	R1K_10K
	0x17	23	AGC_VALUE[7:0]							

Read only
Read and Write

Data Content:

Data only for read:

- CORDIC_OUT(13:0): 14 bit absolute angular position data.
- OCF (Offset Compensation Finished): logic high indicates the finished Offset Compensation Algorithm. As soon as this bit is set, the AS5165 has completed the startup and the data is valid.
- COF (Cordic Overflow): Logic high indicates an out of range error in the CORDIC part. When this bit is set, the CORDIC_OUT(13:0) data is invalid. The absolute output maintains the last valid angular value. This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.
- AGC_VALUE (7:0): magnetic field indication

Data for write and read:

- DSP_RES resets the DSP part of the AS5165 the default value is 0. This is active low. The interface is not affected by this reset.
- R1K_10K defines the threshold level for the OTP fuses. This bit can be changed for verification purpose. A verification of the programming of the fuses is possible. The verification is mandatory after programming.

8.2.2 Programming Procedure

- Pull-up on out pin
- VDD=5V
- Wait startup time, device enters communication mode
- Write128 command: The trimming bits are written in the SFR memory.
- Read128 command: The trimming bits are read back.
- Upload command: The SFR memory is transferred into the OTP RAM.
- Fuse command: The OTP RAM is written in the Poly Fuse cells.
- Wait fuse time (6 ms)
- Write command (R1K_10K=1): Poly Fuse cells are transferred into the RAM cells compared with 10KΩ resistor.
- Download command: The OTP RAM is transferred into the SFR memory.
- Read128 command: The fused bits are read back.
- Write command (R1K_10K=0): Poly Fuse cells are transferred into the RAM cells compared with 1KΩ resistor.
- Download command: The OTP RAM is transferred into the SFR memory.
- Read128 command: The fused bits are read back.
- Pass2Func command: Go back in normal mode

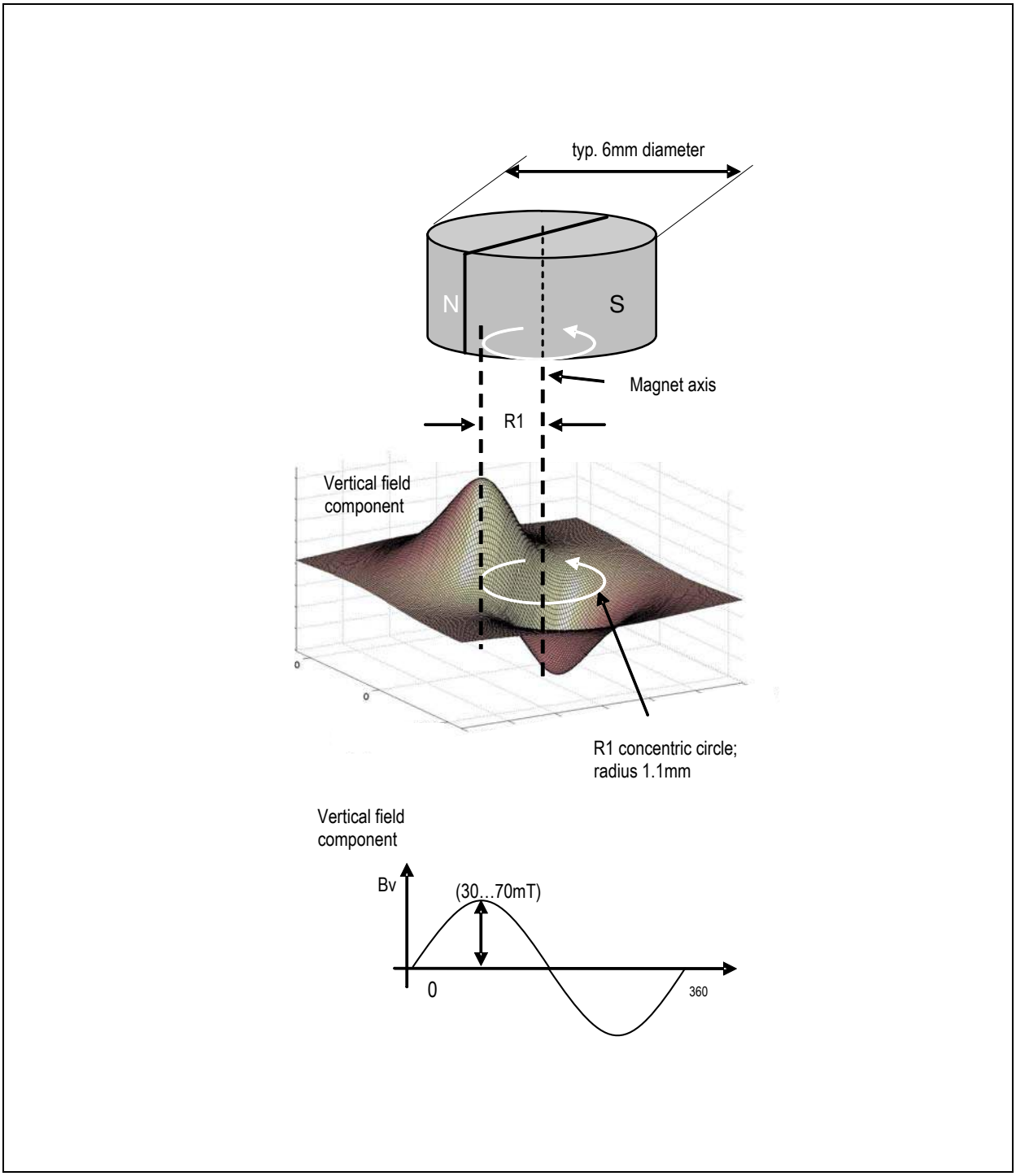
For further information, please refer to Application Note AN_AS5165-10.

8.3 Choosing the Proper Magnet

The AS5165 works with a variety of different magnets in size and shape. A typical magnet could be 6mm in diameter and ≥2.5mm in height. Magnetic materials such as rare earth AlNiCo/SmCo5 or NdFeB are recommended. The magnetic field strength perpendicular to the die surface has to be in the range of ±30mT…±70mT (peak).

The magnet's field strength should be verified using a gauss-meter. The magnetic field B_v at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±30mT…±70mT (see Figure 24).

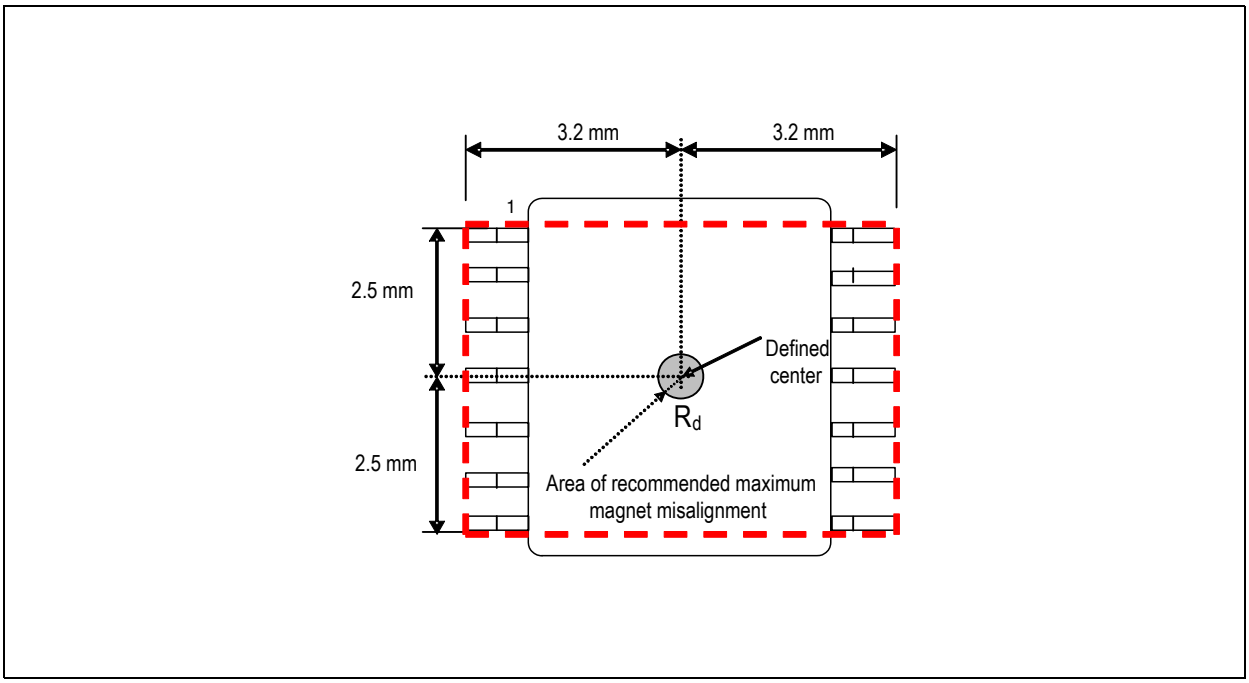
Figure 24. Typical Magnet (6x3mm) and Magnetic Field Distribution



8.3.1 Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in Figure 25.

Figure 25. Defined Chip Center and Magnet Displacement Radius



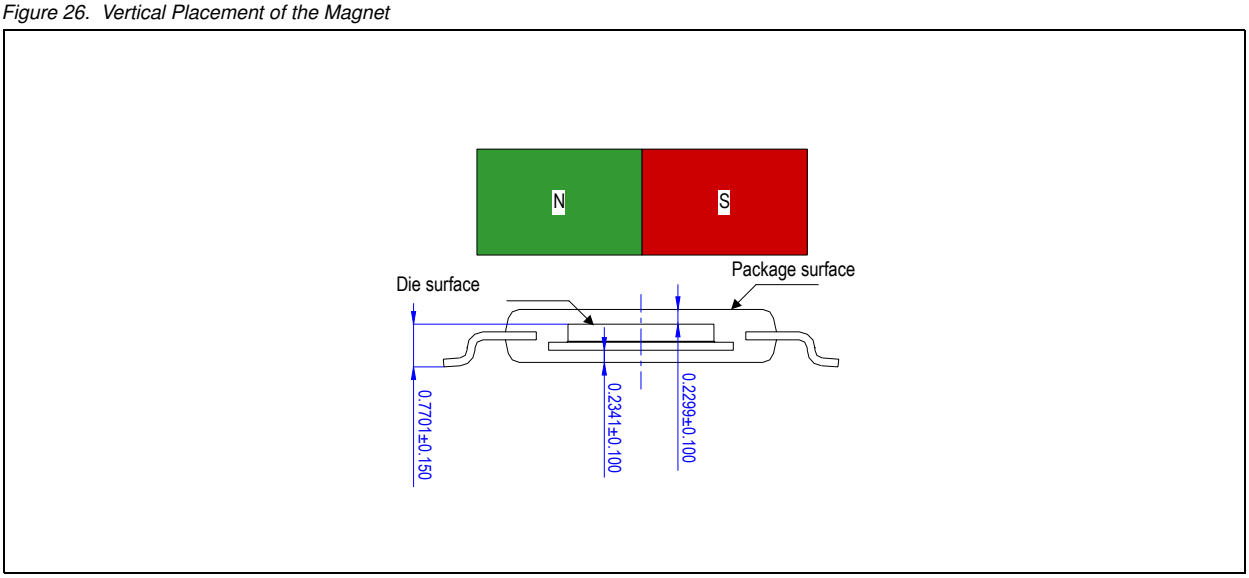
8.3.2 Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm (larger magnets allow more displacement) from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 25). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.5mm, provided the use of the recommended magnet material and dimensions (6mm x 3mm). Larger distances are possible, as long as the required magnetic field strength stays within the defined limits.

However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by an alarm forcing the output into the failure band.

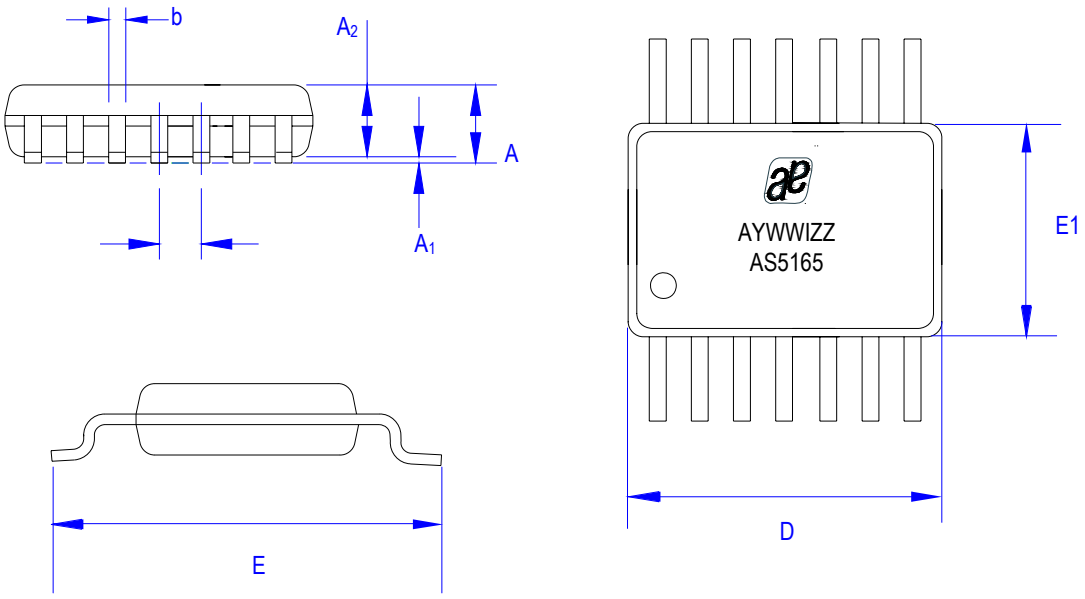
Figure 26. Vertical Placement of the Magnet



9 Package Drawings and Markings

The device is available in a 14-Lead Thin Shrink Small Outline Package.

Figure 27. 14-pin TSSOP Drawings and Dimensions



Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1	0.05	0.10	0.15	.002	.004	.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65			.0256	

Marking: AYWWIZZ.

A	Y	WW	I	ZZ
Pb-Free Identifier	Last Digit of Manufacturing Year	Manufacturing Week	Plant Identifier	Traceability Code

JEDEC Package Outline Standard: MO - 153

Thermal Resistance $R_{th(j-a)}$: 89 K/W in still air, soldered on PCB

Revision History

Revision	Date	Owner	Description
0.1	May 10, 2010	apg	Initial revision

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 11.

Table 11. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS5165HTSU	14-Bit Programmable Magnetic Rotary Encoder	Tubes	TSSOP-14

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

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austriamicrosystems

Contact Information

Headquarters

austriamicrosystems AG
Tobelbaderstrasse 30
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact