User's Guide

Generic ESD Evaluation Module User's Guide

Cameron Phillips

ABSTRACT

The characteristics, operation, and use of the Generic ESDEVM evaluation module (EVM) are described in this user's guide. This EVM includes footprints for almost all of TI's ESD portfolio to be able to test either the signal integrity or DC characteristics. Since this board is for generic evaluation of the ESD parts, it does not come with any devices soldered down. Devices can be sampled by going to ti.com/esd, clicking on the product folder of the device and ordering samples.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Texas Instrument's ESDEVM evaluation module allows the evaluation of most of TI's ESD portfolio. The board comes with all traditional ESD footprints in order to be able to test any number of devices. Devices that need to be tested can be soldered onto their respect footprint and then tested. For the typical high speed ESD devices, an impedance controlled layout is implemented to be able to take the S-parameter and de-embed the board trace. For the non-high speed ESD diodes, footprints with traces going to test points are provided to easily run DC tests such as breakdown voltage, holding voltage, leakage, and so forth. The board layout also makes it easy to connect any of the device's pins to either power (V_{CC}) or ground by shorting the signal pin to which every the signal is. This board allows the testing of all of these typical ESD diode footprints:

- DPY (0402)
- DPL (0201)
- DQA
- DBV
- DCK
- DPK
- DRY
- DRB
- DYA (SOD-523)
- DQD
- RVZ
- DPW

More information about TI's packages

2 Definitions

Contact Discharge a method of testing in which the electrode of the ESD simulator is held in contact with the device-under-test (DUT).

Air Discharge a method of testing in which the charged electrode of the ESD simulator approaches the DUT, and a spark to the DUT actuates the discharge.

ESD simulator a device that generates IEC61000-4-2 compliance ESD waveforms shown in Figure 2-1 with adjustable ranges shown in Table 2-1 and Table 2-2.

IEC61000-4-2 has 4 classes of protection levels. Classes 1 – 4 are shown in Table 2-1. Stress tests should be incrementally tested to level 4 as shown in Table 2-2 until the point of failure. If the DUT does not fail at 8 kV, testing can continue in 2 kV increments until failure.

Table 2-1. IEC61000-4-2 Test Levels

Contact Discharge		Air Discharge	
Class	**Test Voltage [± kV]**	**Class**	**Test Voltage [± kV]**
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15

Table 2-2. Waveform Parameters in Contact Discharge Mode

Stress Level Step	Simulator Voltage [kV]	Ipeak ±15% [A]	Rise Time ±25% [nS]	Current at 30ns ±30% [A]	Current at 60ns ±30% [A]
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	16	8

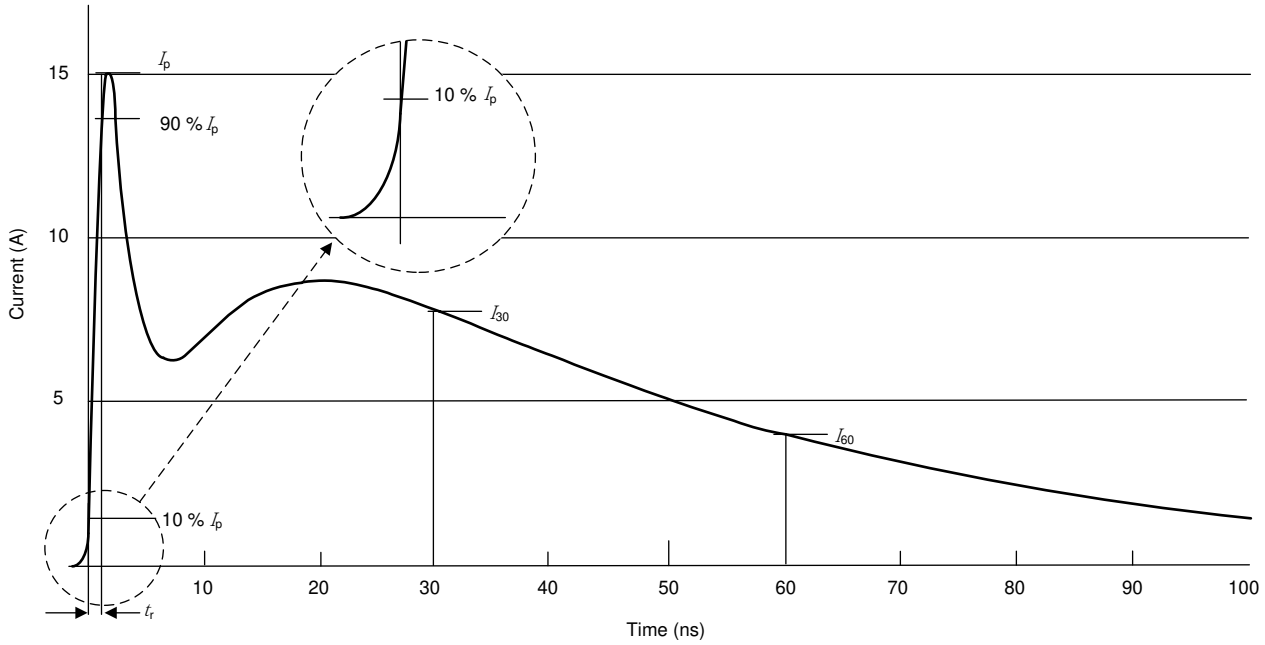

Figure 2-1. Ideal Contact Discharge Waveform of the Output Current of the ESD Simulator at 4 kV

3 S-Parameter Analysis

The top half of the ESDEVM allows signal analysis of ESD diodes. SMA connectors J9 and J10, allow the S-parameter to be taken by vector network analyzer for the DPY (0402), DPL (0201) packages. Also, J16 and J17 can be used to calibrate out the board parasitics to get a more accurate frequency response for the device connected. In order to get results for a particular device only one footprint should be populated at a time. Also for the 4 channel DQA package SMA connectors are provided.

3.1 DQA 4-Port Analysis

ESDEVM is configured with SMA connectors (J1-J4) to allow 4-port analysis with a vector network analyzer. Connect Port 1 to J1 Prot 2 to J2, Port 3 to J3, and Port 4 to J4. This confiuration allows for the following terminology in 4 port analysis:

- S_{11}: Return Loss
- S_{31}: Insertion Loss
- S_{21}: Near End Cross Talk
- S_{41}: Far End Cross Talk

4 Lower Speed Device Testing

The lower portion of the board contains footprints for ESD devices that typically are not placed on high speed signal lines. Therefore the best way to test these devices is to access their pins directly to do DC characteristics on them or to strike the individual pins to see what the device can survive. Each pin of each device goes out to the middle of a three test point row. In the row of test points, the outside most hole is connected to the ground plane of the board. The inside most test point is connected to the VCC plane of the board. This provides ease to be able to connect any setup of an ESD diode to its correct functionality. Most ESD diodes will have one or two pins that are ground for the device which with this layout can easily be shorted to ground by shorting the two test points together. In the same vain the ESD diodes with V_{CC} pins can be connected to the correct pin as well.

If it is desired to do ESD testing on the ESD diodes, make sure that the power pins are connected correctly and use the method below to strike the device. After striking if there is a significant change in the leakage, it is safe to assume the device is broken.

4.1 ESD Tests

TI's ESD portfolio of devices provide robust protection during an ESD event. In order to see the passing level of the device the set up below should be used. It is important to note that due to the parasitics of the EVM, the IEC waveform is slightly different than during validation of the device potentially lending to different results.

4.1.1 Test Method and Set-Up

An example test setup is shown in Figure 4-1. Details of the testing table and ground planes can be found in the IEC 61000-4-2 test procedure. Contact and air-gap discharge are tested using the same simulator with the same discharge waveform. While the simulator is in direct contact with the test point during contact, it is not during air-gap.

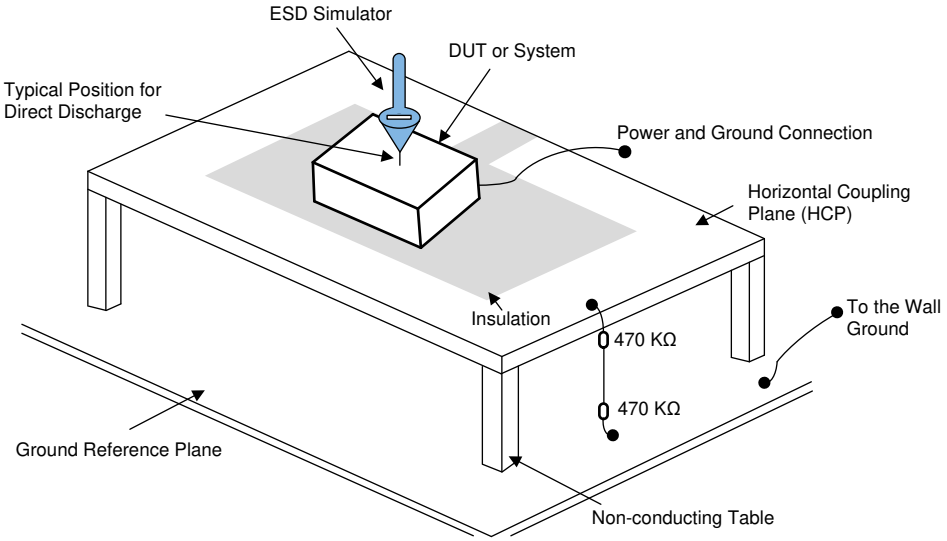

Figure 4-1. System Level ESD Test Setup

4.1.2 Evaluation of Test Results

After ESD testing, perform IV curve testing to see if device has broken or not.

5 Board Layout

This section provides the ESDEVM board layout. ESD224EVM is a 4-layer board of 370HR at 0.062” thickness. Layers 2 and 3 are simple ground planes and not shown here.

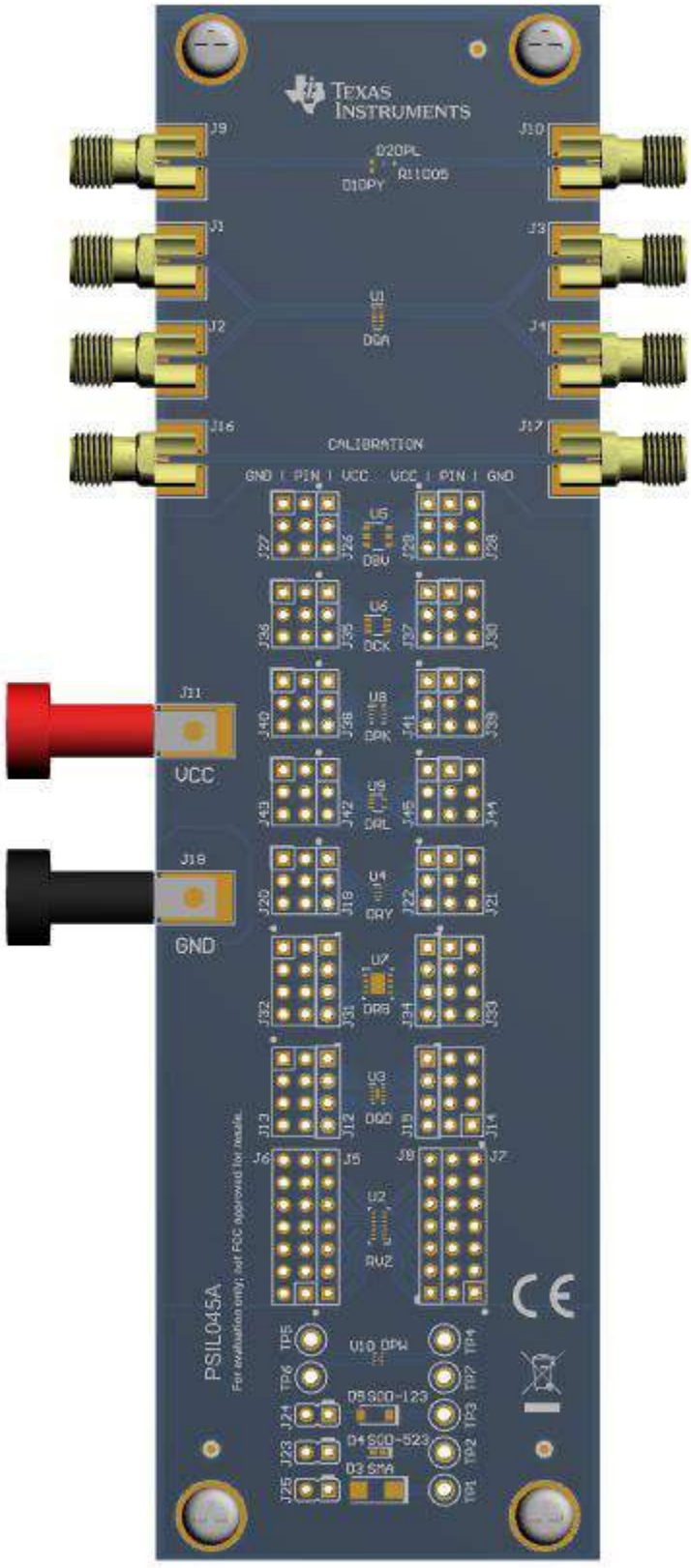

Figure 5-1. 3D Board Image

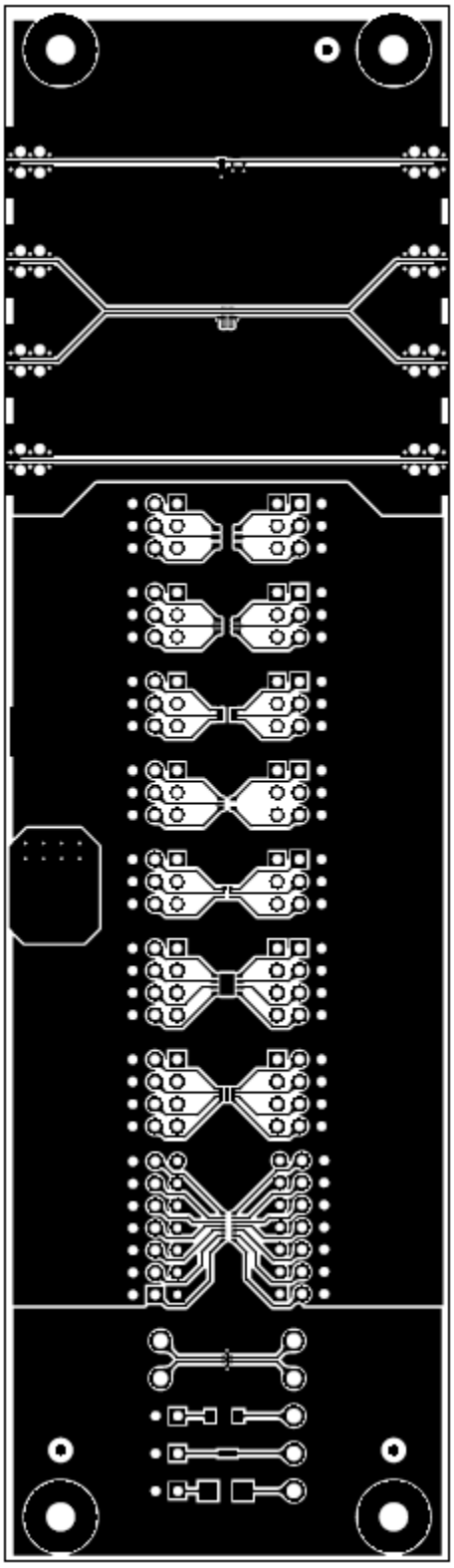

Figure 5-2. ESDEVM Top Layer

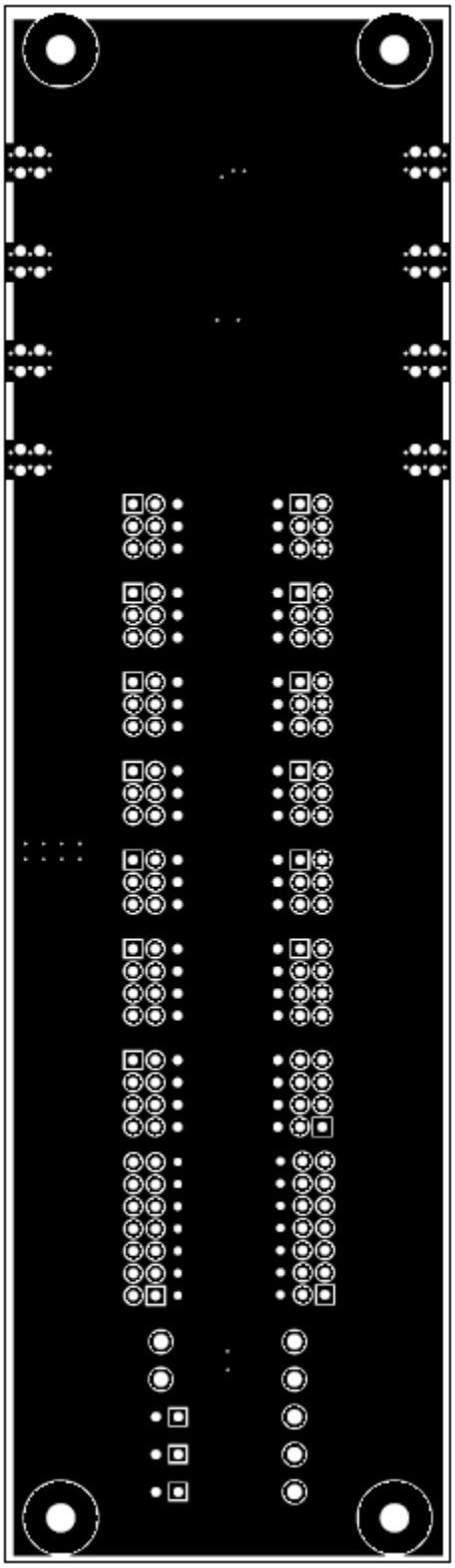

Figure 5-3. ESDEVM Bottom Layer

6 Schematics and Bill of Materials

6.1 Schematics

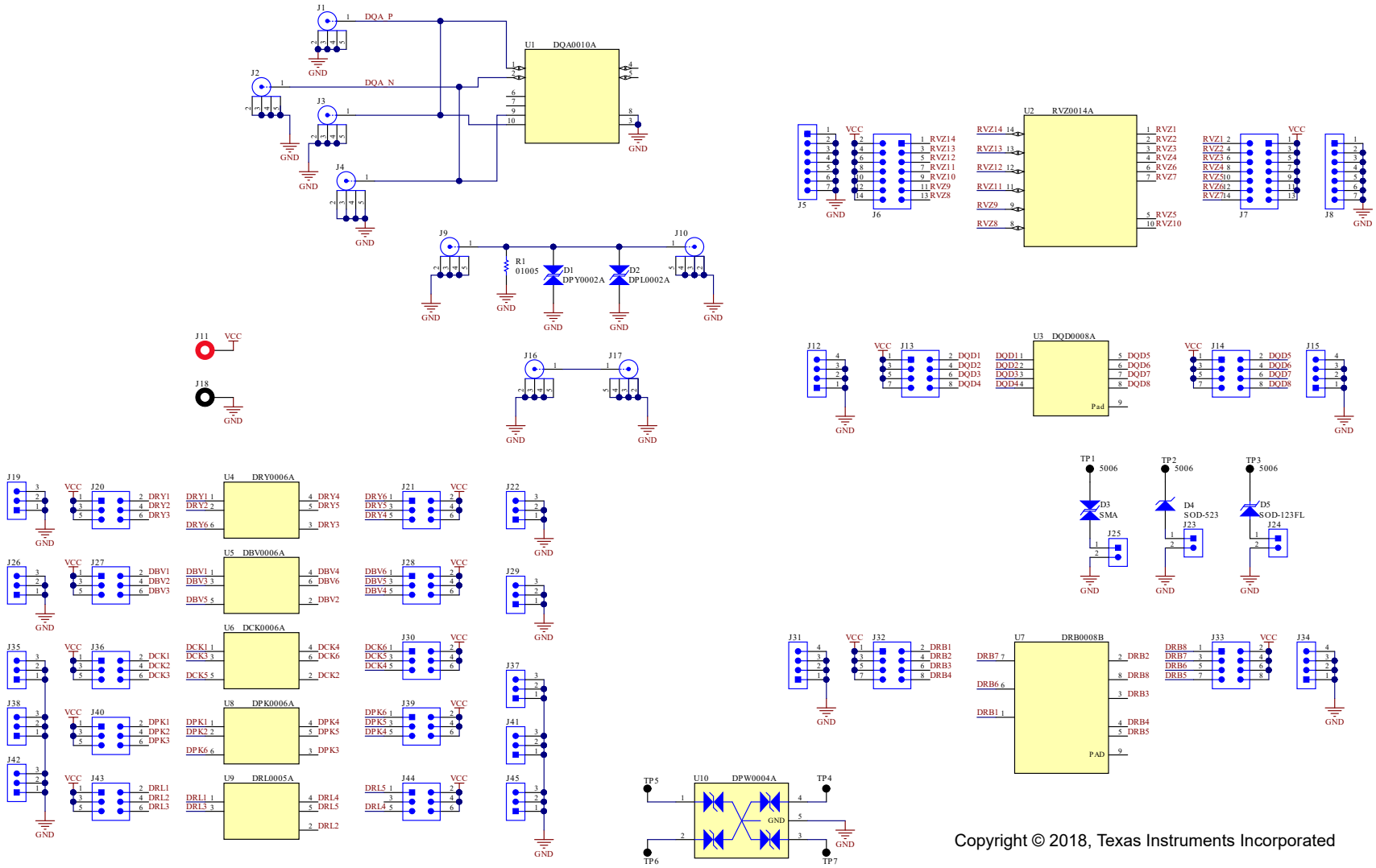

Figure 6-1. ESDEVM Schematic

6.2 Bill of Materials

Table 6-1. Bill of Materials

Count	Reference Designator	Description	Part Number	Manufacturer
8	J1, J2, J3, J4, J9, J10, J16, J17	Connector, End launch SMA 50 Ω, TH	142-0761-881	Cinch Connectivity
1	J11	Standard Banana Jack, Insulated, Red	6091	Keystone
1	J18	Standard Banana Jack, Insulated, Black	6092	Keystone
0	D1	1-Channel ESD Protection Diode for USB Type-C and Thunderbolt 3, DPY0002A (X1SON-2)	DPY0002A	Texas Instruments
0	D2	1-Channel ESD Protection Diode for USB Type-C and Thunderbolt 3, DPL0002A (X2SON-2)	DPL0002A	Texas Instruments
0	D3	Diode, TVS, Bi, 33 V, SMA	SMA	
0	D4	Diode, Zener, 5.1 V, 300 mW, SOD-523	SOD-523 (DYA)	
0	D5	Diode, TVS, Uni, 36 V, 58.1 Vc, SOD-123FL	SOD-123FL	
0	J5, J8	Header, 100 mil, 7x1, TH	800-10-007-10-001 000	Mill-Max
0	J6, J7	Header, 100 mil, 7x2, Tin, TH	PEC07DAAN	Sullins Connector Solutions
0	J12, J15, J31, J34	Header, 100 mil, 4x1, Tin, TH	PEC04SAAN	Sullins Connector Solutions
0	J13, J14, J32, J33	Header, 100 mil, 4x2, Tin, TH	PEC04DAAN	Sullins Connector Solutions
0	J19, J22, J26, J29, J35, J37, J38, J41, J42, J45	Header, 100 mil, 3x1, Tin, TH	PEC03SAAN	Sullins Connector Solutions
0	J20, J21, J27, J28, J30, J36, J39, J40, J43, J44	Header, 100 mil, 3x2, Tin, TH	PEC03DAAN	Sullins Connector Solutions
0	J23, J24, J25	Header, 2.54 mm, 2x1, Gold, TH	GBC02SAAN	Sullins Connector Solutions
0	R1	RES, 0, 5%, 0.03 W, 01005	01005	
0	TP1, TP2, TP3, TP4, TP5, TP6, TP7	Test Point, Compact, Black, TH	5006	Keystone
0	U1	4-Channel ESD Protection Diode for USB Type-C and HDMI 2.0, DQA0010A (USON-10)	DQA	Texas Instruments
0	U2	6-Channel Ultra-Low-Capacitance IEC ESD Protection Diodes, RVZ0014A (USON-14)	RVZ	Texas Instruments
0	U3	ESD Array For Portable Space-Saving Applications, 8 Channels, -40 to +85°C, 8-pin WSON (DQD), Green (RoHS & no Sb/Br)	DQD	Texas Instruments
0	U4	ESD-Protection Array for High-Speed Data Interfaces, 4 Channels, -40 to +85°C, 6-pin SON (DRY), Green (RoHS & no Sb/Br)	DRY	Texas Instruments
0	U5	Low-Capacitance ±15 kV ESD Protection Array for High-Speed Data Interfaces, 4 Channels, -40 to +85°C, 6-pin SOT-23 (DBV), Green (RoHS & no Sb/Br)	DBV	Texas Instruments

Table 6-1. Bill of Materials (continued)

Count	Reference Designator	Description	Part Number	Manufacturer
0	U6	Low-Capacitance ±15 kV ESD Protection Array for High-Speed Data Interfaces, 4 Channels, -40 to +85°C, 6-pin SOT70 (DCK), Green (RoHS & no Sb/Br)	DCK	Texas Instruments
0	U7	40 V, 450 mA, Low IQ, Low-Dropout Voltage Regulator with Power Good, DRB0008B (VSON-8)	DRB	Texas Instruments
0	U8	Low-Capacitance ±15 kV ESD Protection Array for High-Speed Data Interfaces, 4 Channels, -40 to +85°C, 6-pin USON (DPK), Green (RoHS & no Sb/Br)	DPK	Texas Instruments
0	U9	Low-Capacitance Array with ±15 kV ESD Protection, 4 Channels, -40 to +85°C, 5-pin SOT (DRL), Green (RoHS & no Sb/Br)	DRL	Texas Instruments
0	U10	4-Channel ESD Protection With ±15 kV Contact ESD, DPW0004A (X2SON-4)	DPW	Texas Instruments

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2018) to Revision A (September 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2
• Added the DYA (SOD-523) package to the package list and bill of materials	2
• Updated the *Bill of Materials* section	9

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265