INTEGRATED CIRCUITS
UNITRODE

High Power-Factor Preregulator

UC1852
UC2852
UC3852

FEATURES

- Low-Cost Power Factor Correction
- Power Factor Greater Than 0.99
- Few External Parts Required
- Controlled On-Time Boost PWM
- Zero-Current Switching
- Limited Peak Current
- Min and Max Frequency Limits
- Starting Current Less Than 1mA
- High-Current FET Drive Output
- Under-Voltage Lockout

DESCRIPTION

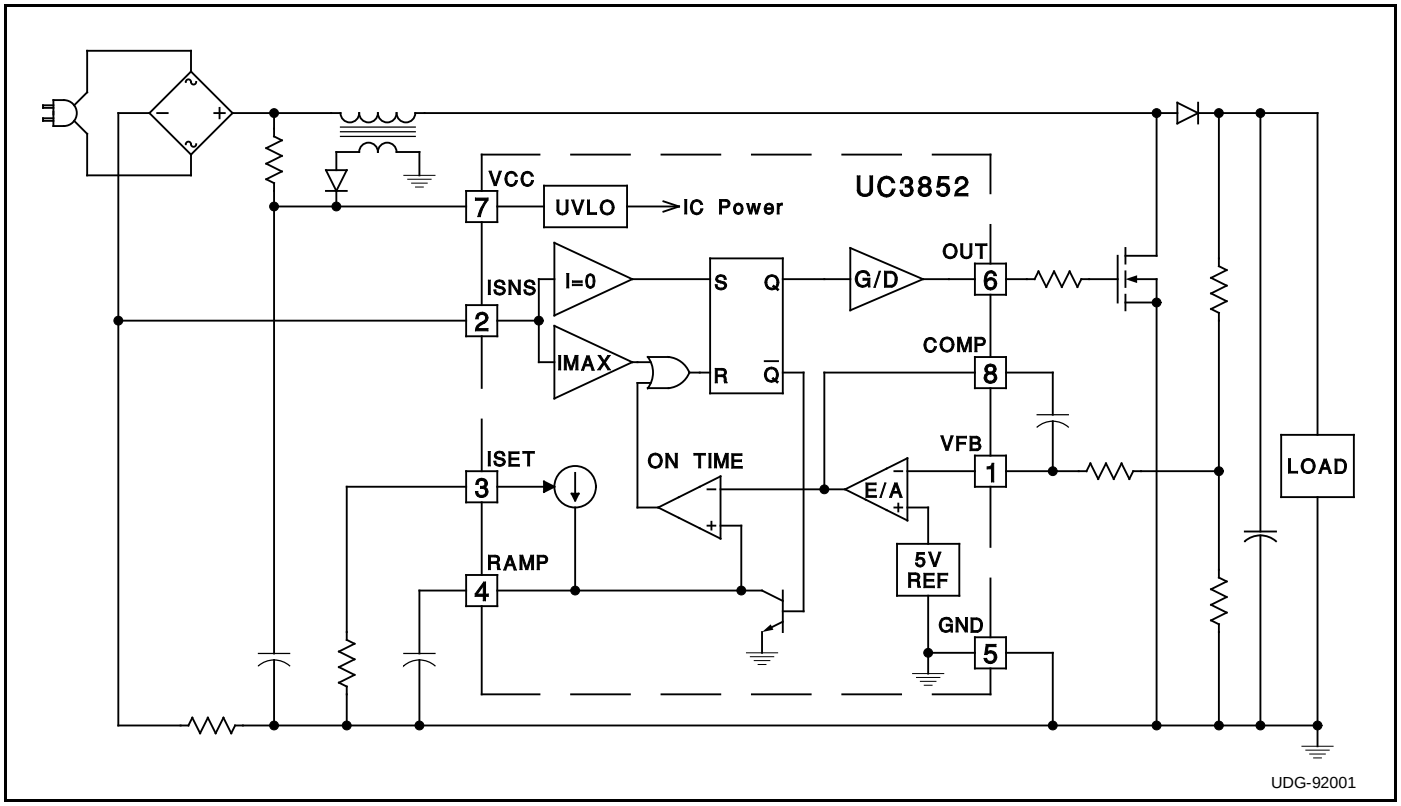
The UC1852 provides a low-cost solution to active power-factor correction (PFC) for systems that would otherwise draw high peak current pulses from AC power lines. This circuit implements zero-current switched boost conversion, producing sinusoidal input currents with a minimum of external components, while keeping peak current substantially below that of fully-discontinuous converters.

The UC1852 provides controlled switch on-time to regulate the output bulk DC voltage, an off-time defined by the boost inductor, and a zero-current sensing circuit to reactivate the switch cycle. Even though switching frequency varies with both load and instantaneous line voltage, it can be maintained within a reasonable range to minimize noise generation.

While allowing higher peak switch currents than continuous PFCs such as the UC1854, this device offers less external circuitry and smaller inductors, yet better performance and easier line-noise filtering than discontinuous current PFCs with no sacrifice in complexity or cost. The ability to obtain a power factor in excess of 0.99 makes the UC1852 an optimum choice for low-cost applications in the 50 to 500 watt power range. Protection features of these devices include under-voltage lockout, output clamping, peak-current limiting, and maximum-frequency clamping.

The UC1852 family is available in 8-pin plastic and ceramic dual in-line packages, and in the 8-pin small outline IC package (SOIC). The UC1852 is specified for operation from -55°C to +125°C, the UC2852 is specified for operation from -40°C to +85°C, and the UC3852 is specified for operation from 0°C to +70°C.

TYPICAL APPLICATION



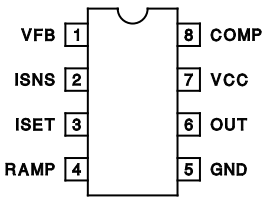
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Low-impedance Source) 30.0V
Supply Current (High-impedance Source) 30.0mA
OUT Current, Peak ..... ±1.0A
OUT Energy, Capacitive Load 5.0µJ
Input Voltage, ISNS ..... ±5.0V
Input Voltage, VFB ..... –0.3V to +10.0V
COMP Current ..... ±10.0mA
ISET Current ..... –10.0mA
Power Dissipation at Ta≤25°C (Note 3) 1.0W
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

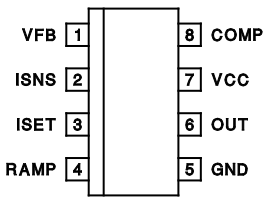
Note 1: All voltages with respect to GND (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: Refers to DIL-8 Package. Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL–8 (TOP VIEW)
J or N Package



SOIC–8 (TOP VIEW)
D Package



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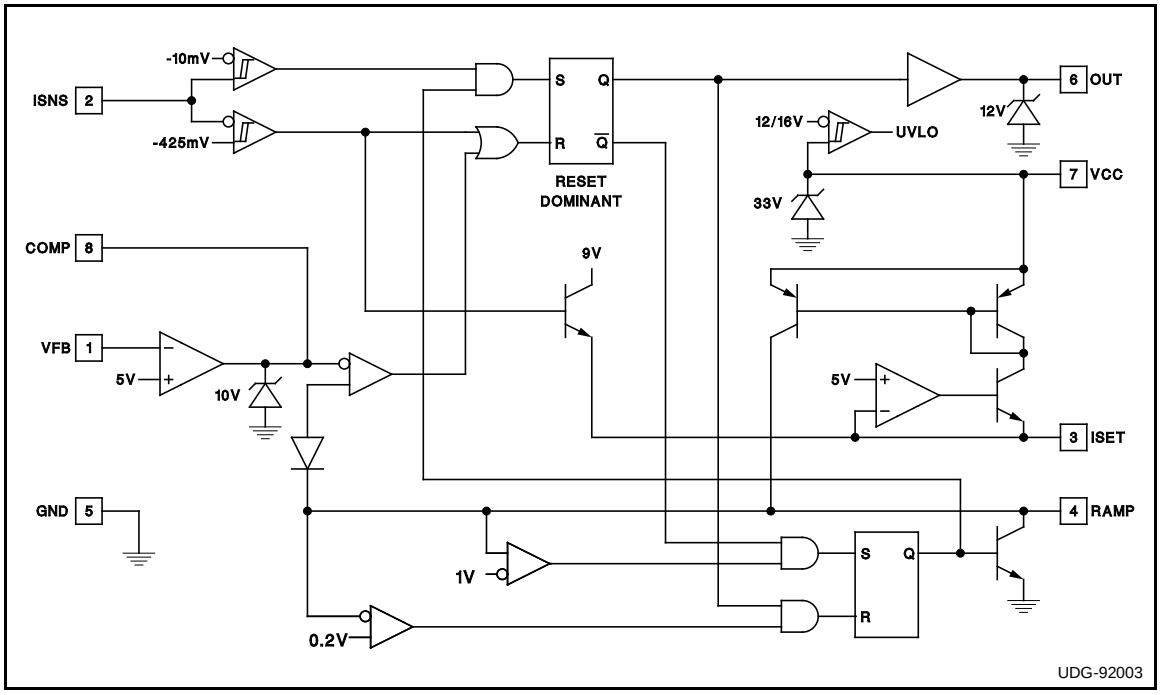
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, VCC=24V, ISET=50kΩ to GND, RAMP=1nF to GND, ISNS= –0.1V, VFB connected to COMP, no load on OUT, –55°C<Ta<+125°C for the UC1852, –40°C<Ta<+85°C for the UC2852, and 0°C<Ta<+70°C for the UC3852, and Ta=Tj.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Timer Section					
ISET Voltage		4.5	5.0	5.5	V
RAMP Charge Current	RAMP=2.5V	88	98	108	µA
RAMP Discharge Current	ISNS= –1.0V, RAMP=1.0V	12	28	50	mA
RAMP Saturation Voltage	ISNS= –1.0V, I_{RAMP}=100µA		0.006	0.200	V
RAMP Threshold - Maximum Frequency	VFB=10V, COMP open	0.92	1.02	1.12	V
RAMP Threshold - PWM Comparator		3.9	4.3	4.8	V
Current Sense Comparator					
ISNS Restart Threshold		–18	–10	–4	mV
ISNS Fault Threshold		–550	–450	–350	mV
ISNS Input Current		–100	–30	100	µA
Error Amplifier Section					
VFB Input Voltage		4.6	5.0	5.3	V
VFB Input Bias Current		–5.00	–0.03	5.00	µA
COMP Sink Current	COMP=7.5V	10			mA
COMP Source Current	COMP=2.5V	–300	–175	–100	µA
COMP Clamp Voltage	VFB=0.0V, COMP open	9.2	10.0	10.6	V
OUT Output					
OUT Saturation Voltage High	VCC=13V, I_{OUT}= –200mA, RAMP=2V	0.5	1.7	2.5	V
OUT Saturation Voltage Low	I_{OUT}=200mA, ISNS= –1.0V	0.5	1.6	2.2	V
OUT Saturation Voltage Low @ 10mA	I_{OUT}=10mA, ISNS= –1.0V		0.05	0.40	V
OUT Clamp Voltage	I_{OUT}= –200mA, RAMP=2V	10.0	12.0	14.5	V
OUT Voltage during UVLO	I_{OUT}=100mA, VCC=0V	0.5	1.0	2.2	V
Overall Section					
Inactive Supply Current	VCC=10V	0.2	0.4	1.0	mA
Active Supply Current		3.0	6.0	10.0	mA
VCC Clamp Voltage	ICC=25mA	30	33	36	V
VCC Turn-On Threshold		14.5	16.3	17.5	V
VCC Turn-Off Threshold		10.5	11.5	13.0	V
VCC Threshold Hysteresis		3	5	7	V

DETAILED BLOCK DIAGRAM



PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. To limit PWM on-time, this pin is clamped to approximately 10V. To implement soft start, the COMP pin can be pulled low and ramped up with a PNP transistor, a capacitor, and a resistor.

GND: Ground for all functions is through this pin.

ISET: The dominant function is of this pin is to program RAMP charging current. RAMP charging current is approximately 5V divided by the external resistor placed from ISET to ground. Resistors in the range of 10kΩ to 50kΩ are recommended, producing currents in the range of 100µA to 500µA.

A second function of ISET is as reference output. The ISET pin is normally regulated to 5V ±10%. It is critical that this pin only see the loading of the RAMP programming resistor, but a high input-impedance comparator or amplifier may be connected to this pin or to a tap on the RAMP programming resistor if required.

The third function of the ISET pin is as a FAULT output. In the event of an over-current fault, the ISET pin is forced to approximately 9V by the fault comparator. This can be used to trip an external protection circuit which can disable the load or start a fault restart cycle.

ISNS: This input to the zero and over current comparators is specially built to allow operation over a ±5V dynamic range. In noisy systems or systems with very high Q inductors, it is desirable to filter the signal entering the ISNS input to prevent premature restart or fault cycles. For best accuracy, ISNS should be connected to a current sense resistor through no more than 200 ohms.

OUT: The output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±500mA. To prevent damage to the power MOSFET, the OUT pin is internally driven by a 12V supply. However, lead inductance between the OUT pin and the load can cause overshoot and ringing. External current boost transistors will increase this overshoot and ringing. If there is any significant distance between the IC and the MOSFET, external clamp diodes and/or series damping resistors may be required. OUT is actively held low when the VCC is below the UVLO threshold.

RAMP: A controlled on-time PWM requires a timer whose time can be modulated by an external voltage. The timer current is programmed by a resistor from ISET to GND. A capacitor from RAMP to GND sets the on time in conjunction with the voltage on COMP. Recommended values for the timer capacitors are between 100pF and 1nF.

VCC: VCC is the logic and control power connection for this device. VCC current is the sum of active device supply current and the average OUT current. Knowing the maximum operating frequency and the MOSFET gate charge (Qg), average OUT current can be estimated by:

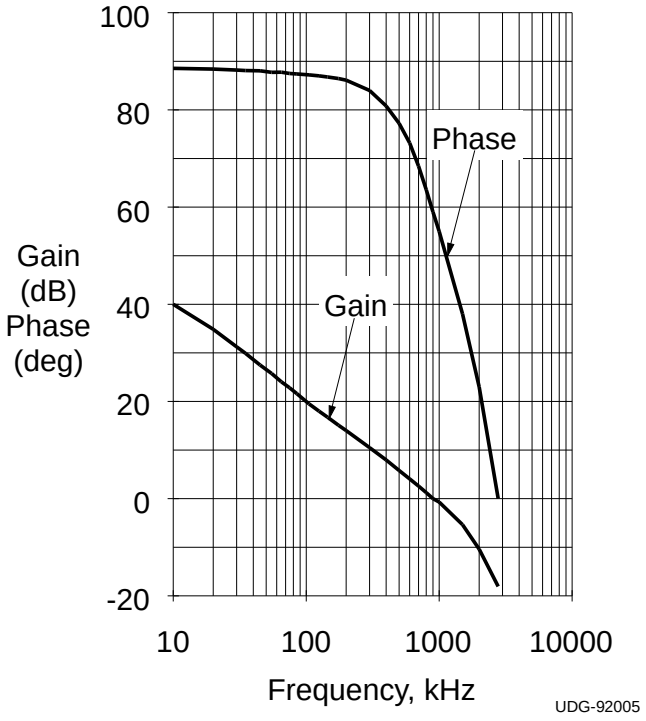
$$I_{OUT} = Q_g \times F$$

To prevent noise problems, bypass VCC to GND with both a ceramic and an electrolytic capacitor.

VFB: VFB is the error amplifier inverting input. This input serves as both the voltage sense input to the error amplifier

TYPICAL CHARACTERISTICS

Error Amplifier Gain and Phase



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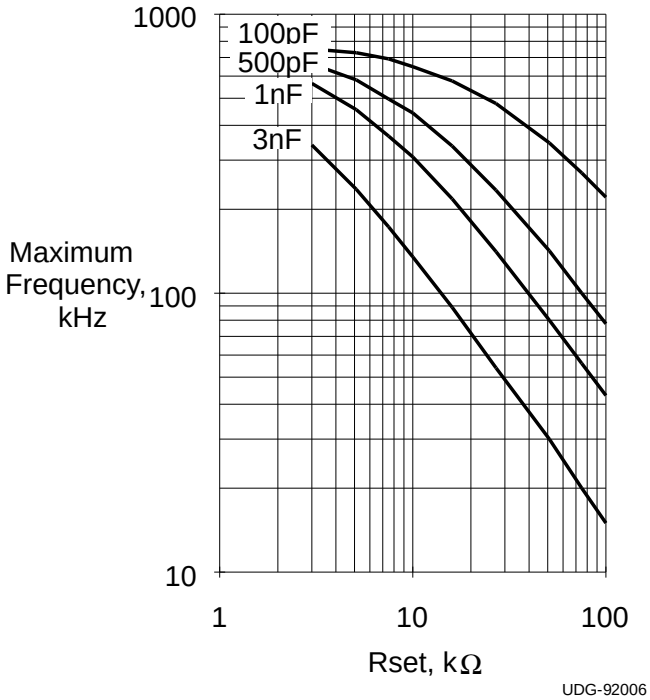
Max Frequency vs. Rset and Ct



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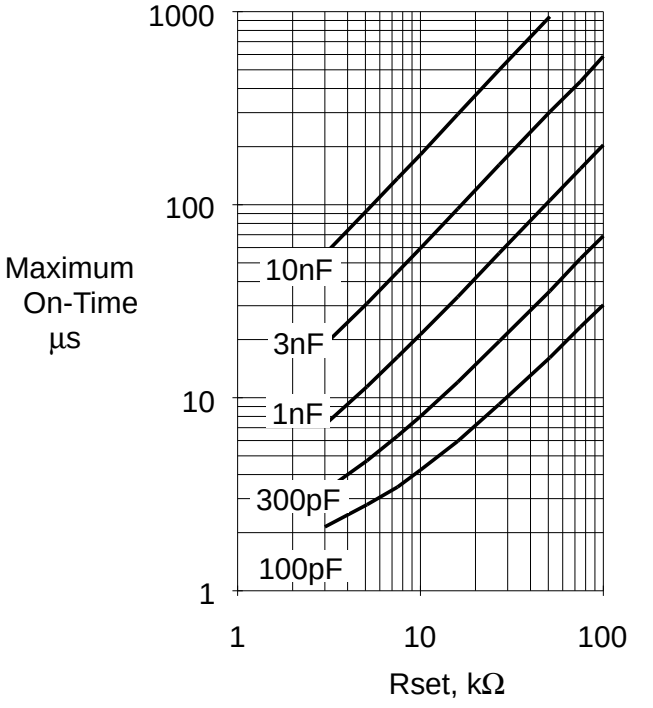
Max On-Time vs. Rset and Ct



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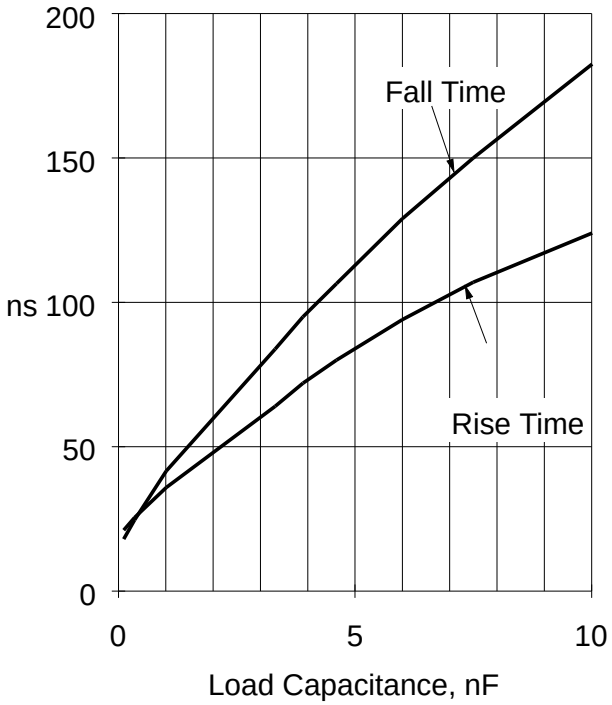
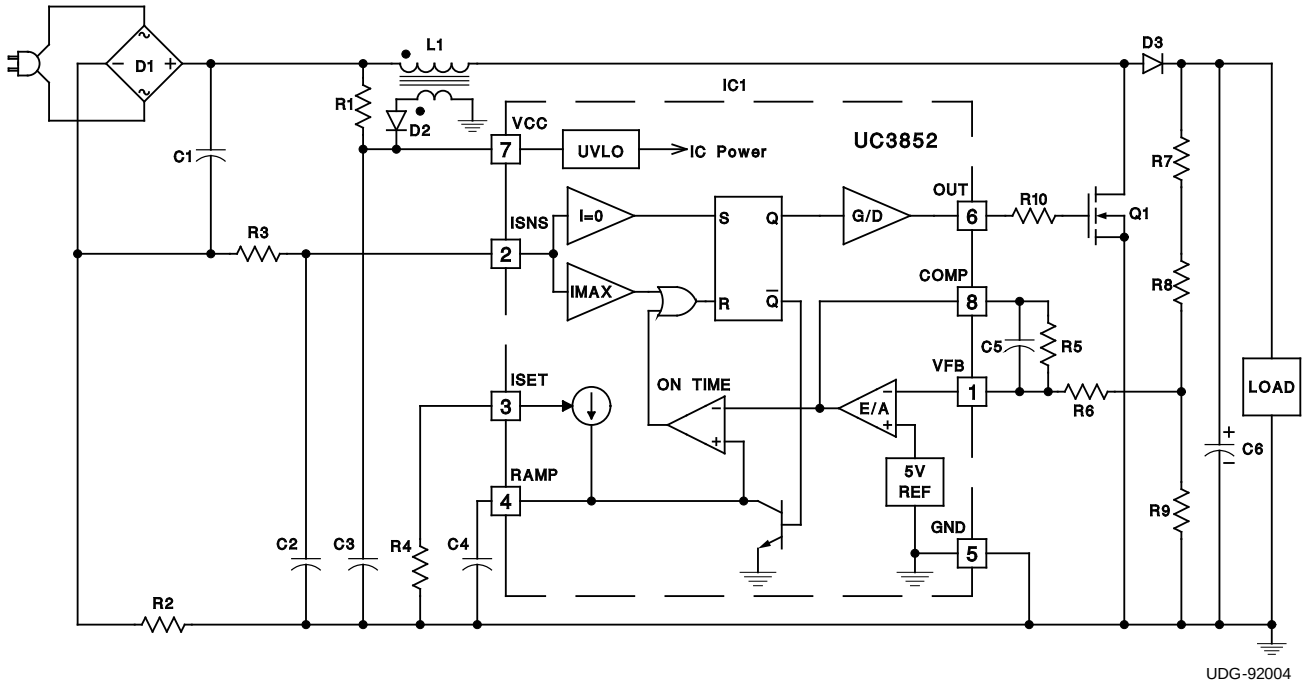
OUT Rise and Fall Time



UDG-92008

APPLICATION INFORMATION: A 100 Watt Power Factor Preregulator



This circuit demonstrates a complete power factor preregulator based on the UC3852. This preregulator will supply up to 100 watts at 400VDC and exhibit power factor greater than 0.995 with less than 10% total harmonic distortion. Operating input range is 90V to 160V RMS at 50Hz to 60Hz.

This design is intentionally simple, yet fully functional. The UC3852 can also be used in designs featuring soft start, over-voltage protection, wide power-line voltage operation, and fault latching. For more information on applying the UC3852, refer to Unitrode Application Note U–132.

PARTS LIST

C1	0.47µF/250VAC X2 Class Polyester	Q1	IRF830 4.5A/500V 1.5Ω Power FET
C2	1nF/16V Ceramic	L1	680µH (Renco RL3792 with 10 Turn 24 AWG Secondary)
C3	68µF/35V Aluminum Electrolytic	R1	150kΩ, ¼W
C4	180pF/16V Ceramic	R2	0.2Ω, ½W Carbon Composition
C5	0.1µF/16V Polyester or Ceramic	R3	10Ω, ¼W
C6	82µF/450V Aluminum Electrolytic	R4	13.3kΩ, ¼W
D1	2A/500V Bridge Rectifier (Collmer KBPC106 or Powertex MB11A02V60)	R5	1MΩ, ¼W
D2	100mA/50V Switching Diode (1N4148)	R6	20kΩ, ¼W
D3	2A/500V 250ns Recovery-Time Rectifier (Motorola MR856)	R7	200kΩ, ½W
IC1	UC3852N Power Factor Controller IC	R8	200kΩ, ½W

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2852D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2852D	Samples
UC2852DTR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2852D	Samples
UC2852N	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UC2852N	Samples
UC3852D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3852D	Samples
UC3852DTR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3852D	Samples
UC3852N	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3852N	Samples
UC3852NG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3852N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

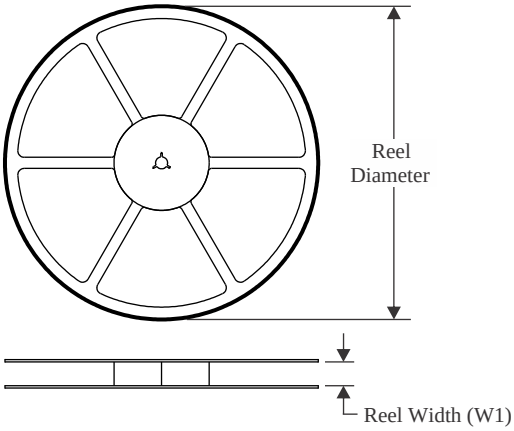
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

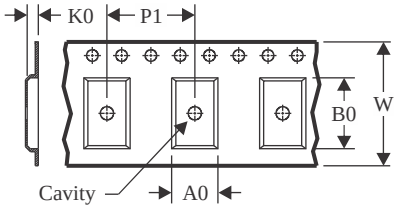
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

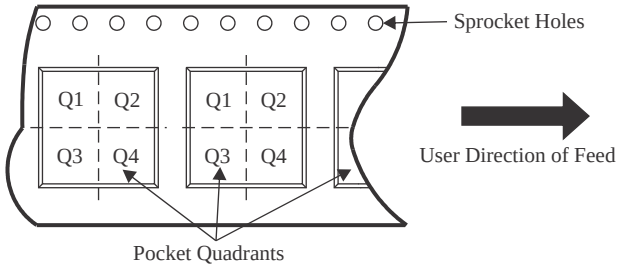


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

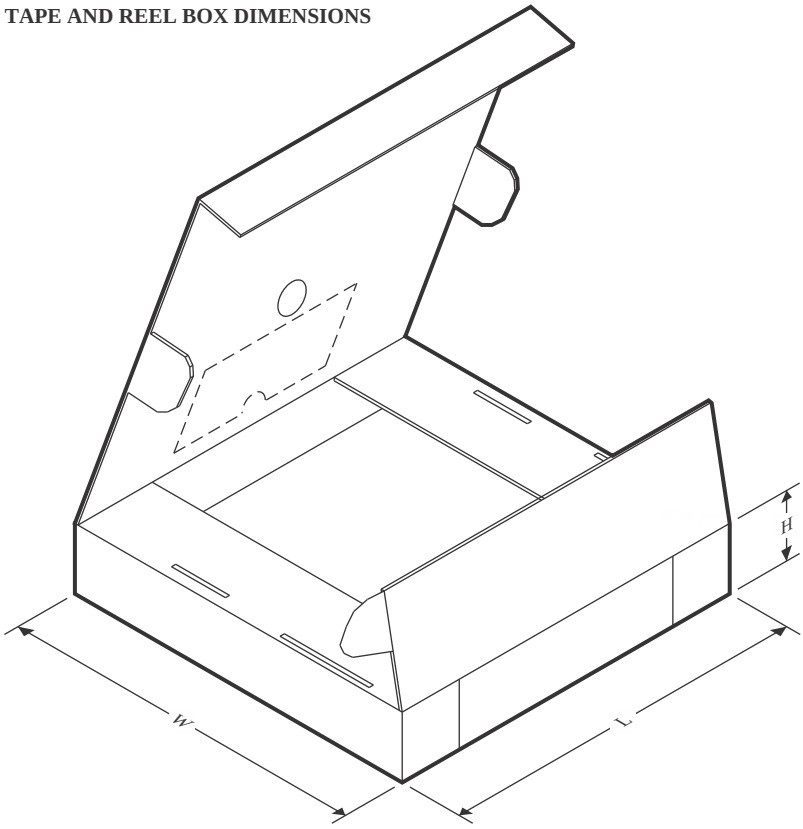
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2852DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3852DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

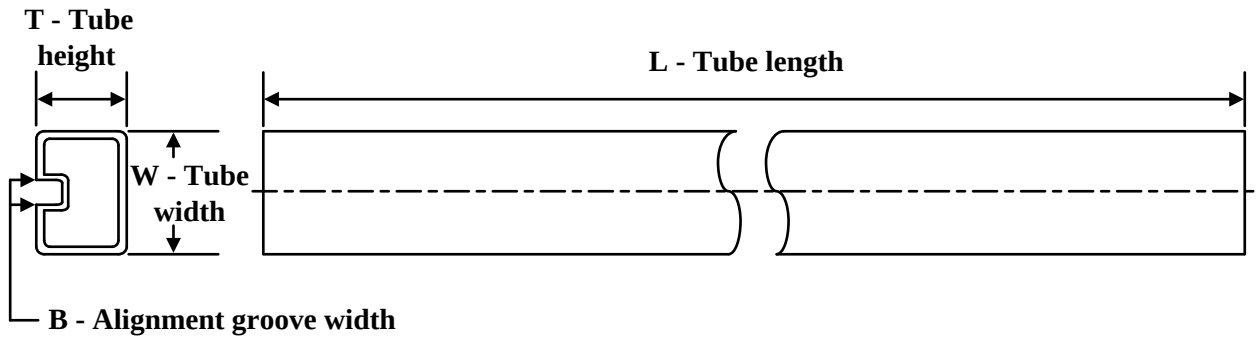
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2852DTR	SOIC	D	8	2500	356.0	356.0	35.0
UC3852DTR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2852D	D	SOIC	8	75	506.6	8	3940	4.32
UC2852N	P	PDIP	8	50	506	13.97	11230	4.32
UC3852D	D	SOIC	8	75	506.6	8	3940	4.32
UC3852N	P	PDIP	8	50	506	13.97	11230	4.32
UC3852NG4	P	PDIP	8	50	506	13.97	11230	4.32

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