April 2015

FDD8445

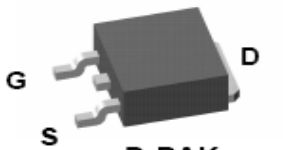
N-Channel PowerTrench® MOSFET
40V, 50A, 8.7mΩ

Features

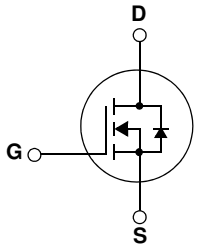
- $R_{DS(ON)}$ = 6.7 mΩ (Typ), V_{GS} = 10V, I_D=50A
- $Q_{g(10)}$ = 45nC (Typ), V_{GS}=10V
- Low Miller Charge
- Low Qrr Body Diode
- UIS Capability (Single Pulse/ Repetitive Pulse)
- RoHS Compliant

Applications

- Powertrain Management
- Electronic Transmission
- Distributed Power Architecture and VRMs
- Primary Switch for 12V Systems



D-PAK
(TO-252)



Absolute Maximum Ratings T_c = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (V_{GS}=10v) (Note 1)	70	A
	Continuous (V_{GS}=10v,with $R_{\theta JA}$ = 52°C/W)	15.2	A
	Pulsed	Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note2)	144	mJ
P_D	Power Dissipation	79	W
	Derate above 25°C	0.53	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient TO-252, lin^2 copper pad area	52	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8445	FDD8445	TO-252AA	13”	16mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 32V, V_{GS} = 0V, T_J=150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2	2.8	4	V
$R_{DS(ON)}$	Drain to Source On Resistance	I_D = 50A, V_{GS} = 10V	-	6.7	8.7	mΩ
		I_D = 50A, V_{GS} = 10V, T_J = 175°C	-	12.5	16.3	
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	3040	4050	pF
C_{OSS}	Output Capacitance		-	295	390	pF
C_{RSS}	Reverse Transfer Capacitance		-	178	270	pF
R_G	Gate Resistance	f = 1MHz	-	1.7	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V, V_{DD} = 20V, I_D = 50A	-	45	59	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0 to 5V, V_{DD} = 20V, I_D = 50A	-	17	22	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 to 2V, V_{DD} = 20V, I_D = 50A	-	5.8	7.6	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 20V, I_D = 50A	-	12.5	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	V_{DD} = 20V, I_D = 50A	-	9.5	-	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 20V, I_D = 50A	-	10.5	-	nC

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Switching Characteristics						
$t_{(on)}$	Turn-On Time	V_{DD} = 20V, I_D = 50A V_{GS} = 10V, R_{GS} = 2Ω	-	-	138	ns
$t_{d(on)}$	Turn-On Delay Time		-	10	-	ns
t_r	Turn-On Rise Time		-	82	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	-	ns
t_f	Turn-Off Fall Time		-	9.6	-	ns
t_{off}	Turn-Off Time		-	-	53	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD}=50A	-	-	1.25	V
		I_{SD}=25A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_F= 50A, dI_F/dt=100A/μs	-	-	39	ns
Q_{rr}	Reverse Recovery Charge	I_F= 50A, dI_F/dt=100A/μs	-	-	38	nC

Notes:
1: Maximum package current capability is 50A.
2: Starting T_J = 25°C, L=0.18mH, I_{AS}=40A.

Typical Characteristics

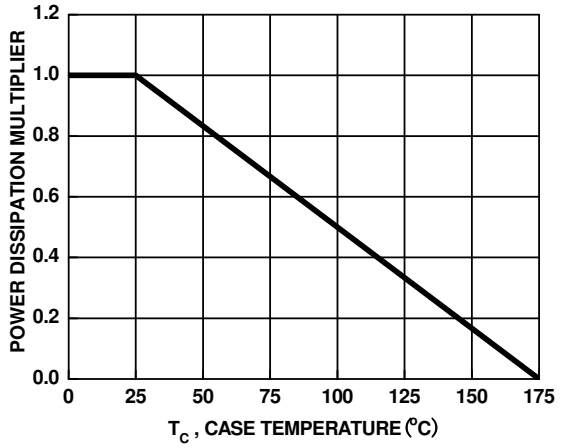


Figure 1. Normalized Power Dissipation vs Case Temperature

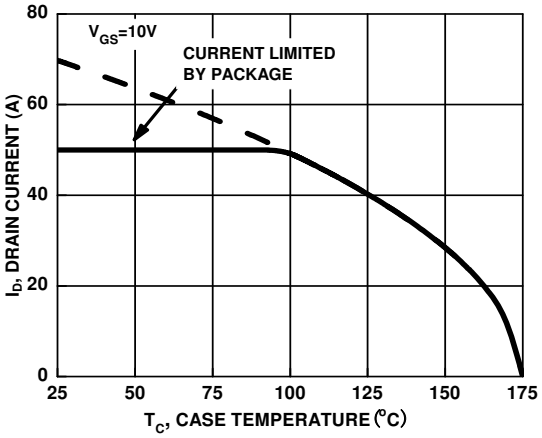


Figure 2. Maximum Continuous Drain Current vs Case Temperature

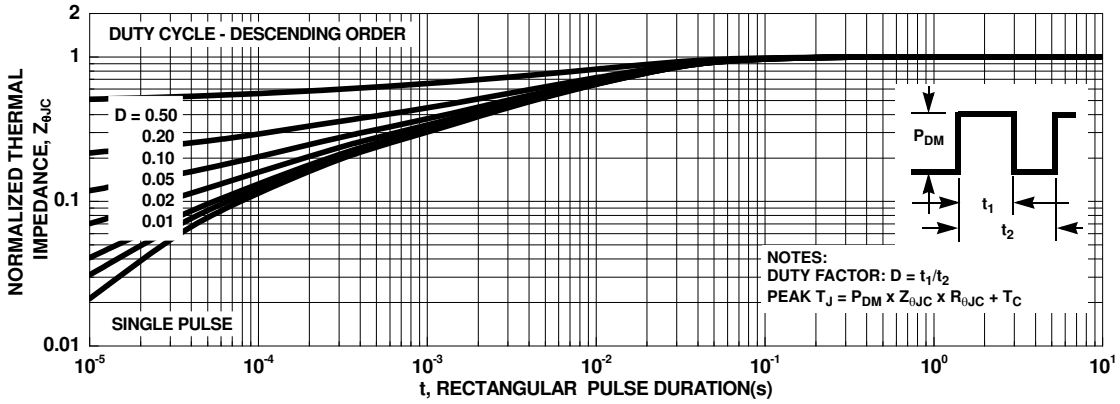


Figure 3. Normalized Maximum Transient Thermal Impedance

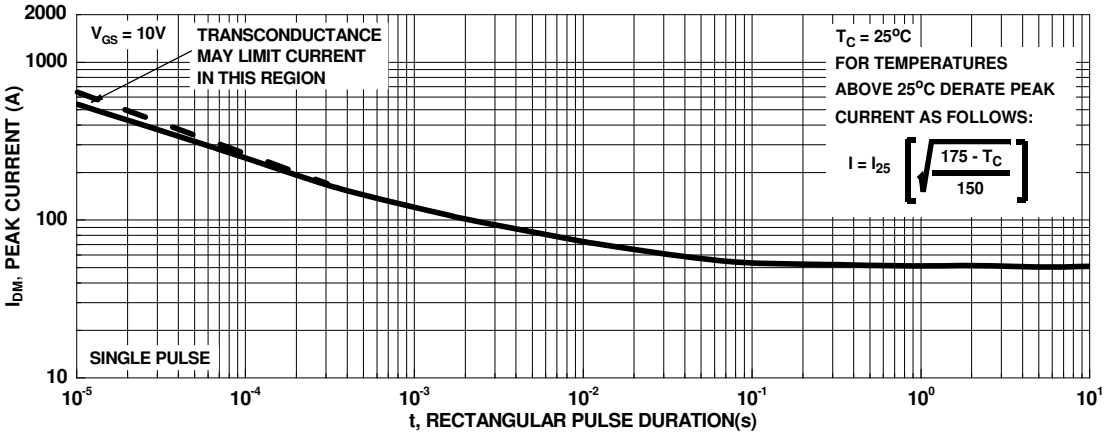


Figure 4. Peak Current Capability

Typical Characteristics

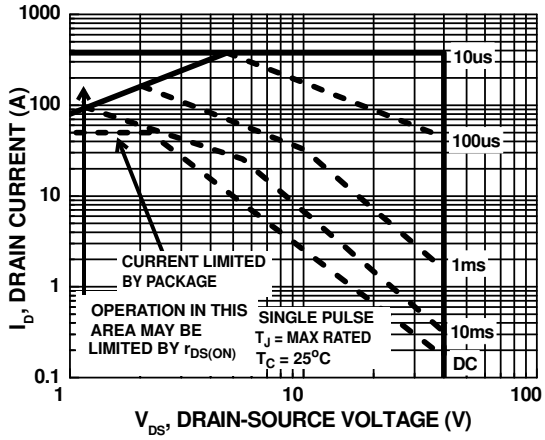
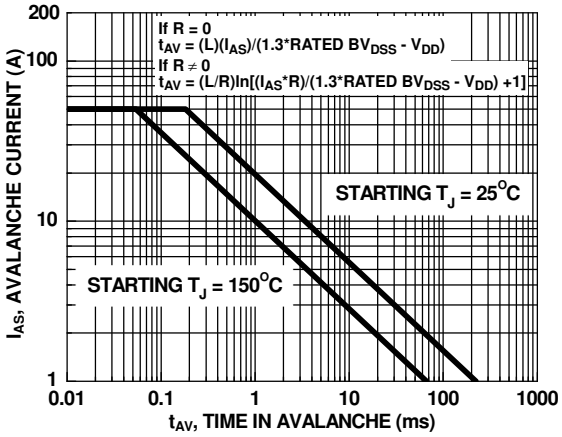


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Indutive Switching Capability

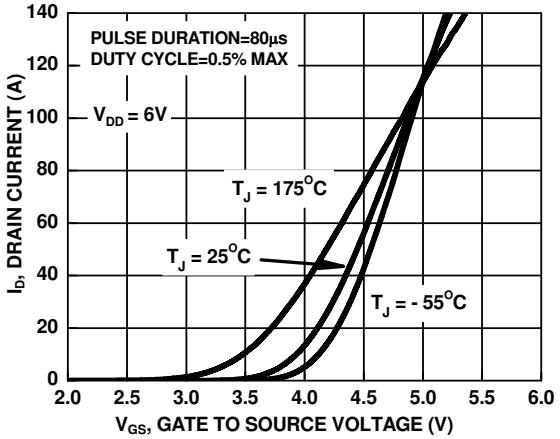


Figure 7. Transfer Characteristics

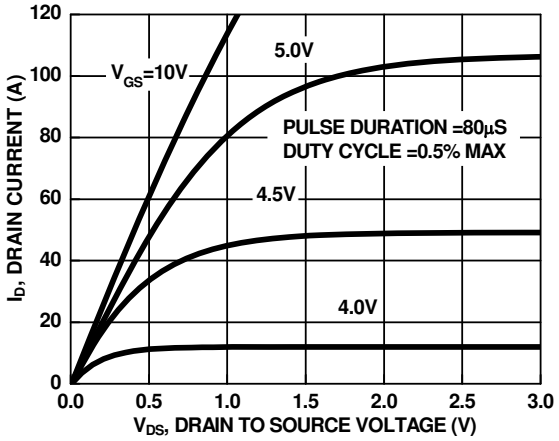


Figure 8. Saturation Characteristics

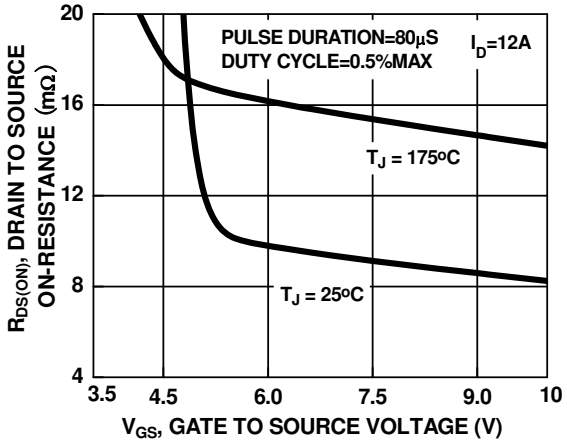


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

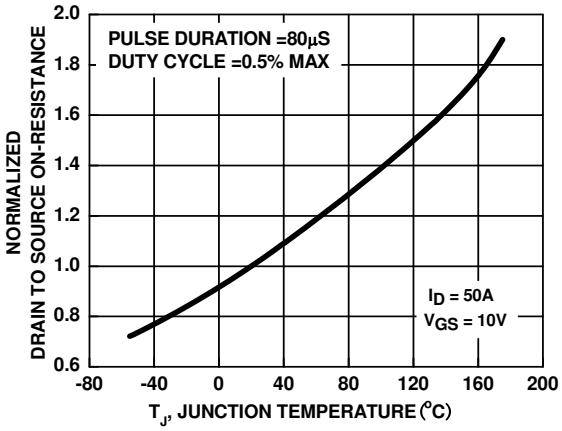


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics

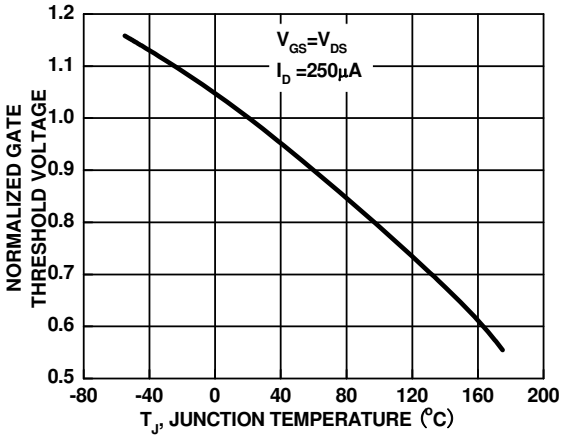


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

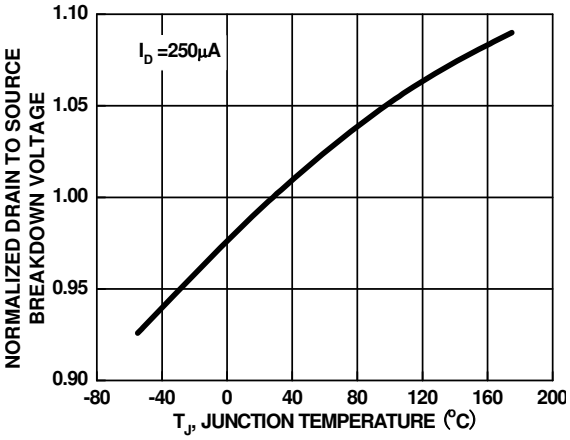


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

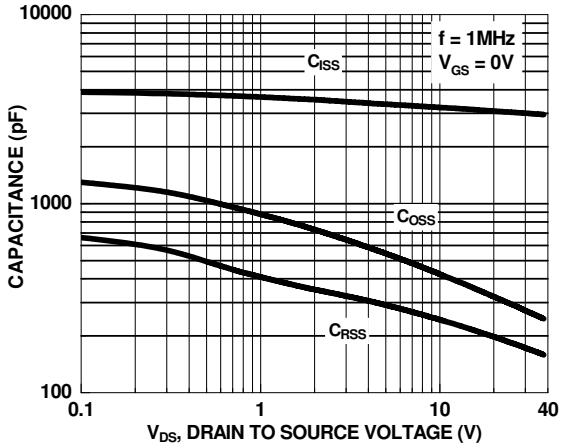


Figure 13. Capacitance vs Drain to Source Voltage

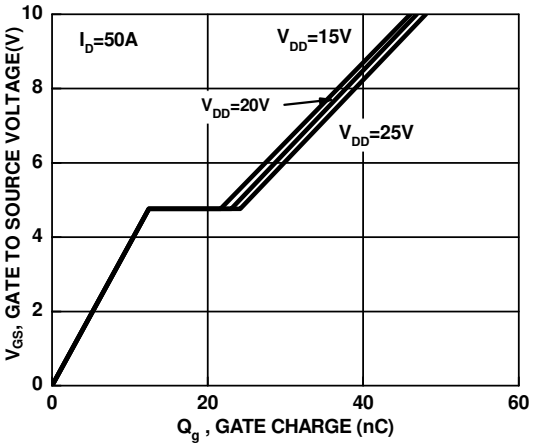
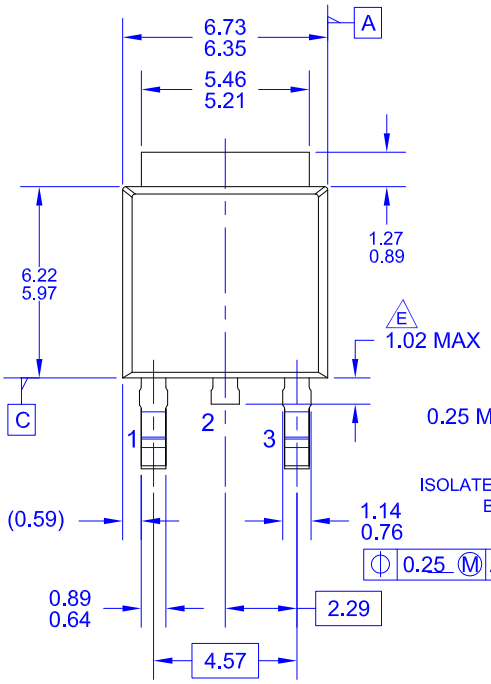
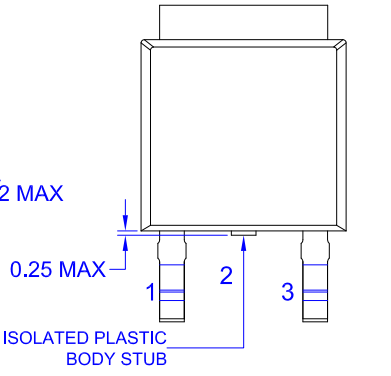


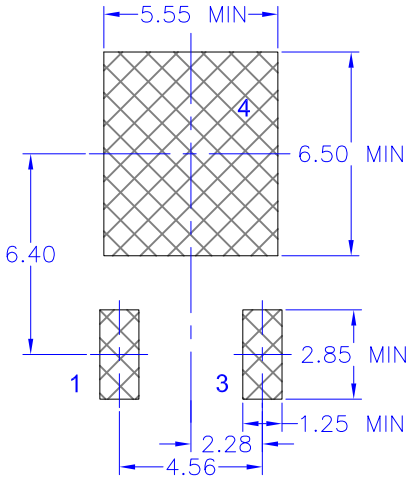
Figure 14. Gate Charge vs Gate to Source Voltage



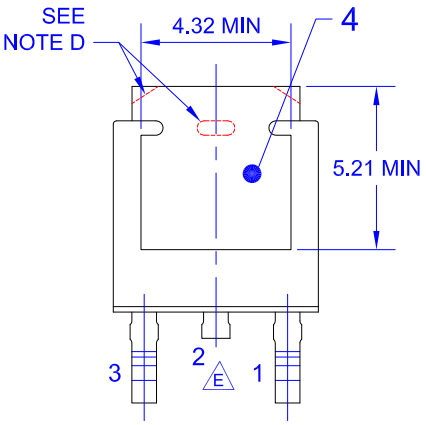
NON-DIODE PRODUCTS VERSION



DIODE PRODUCTS VERSION



LAND PATTERN RECOMMENDATION



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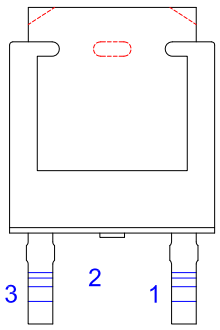

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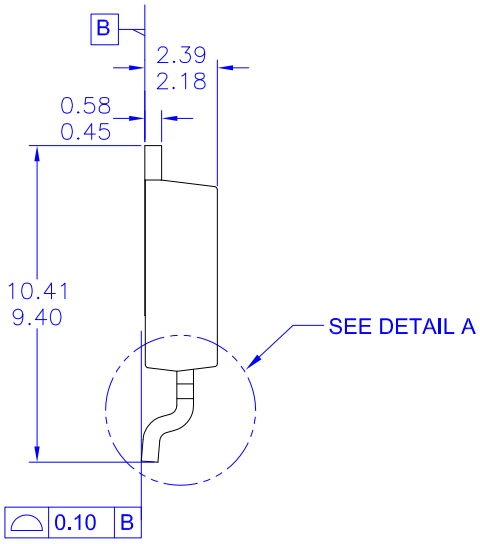
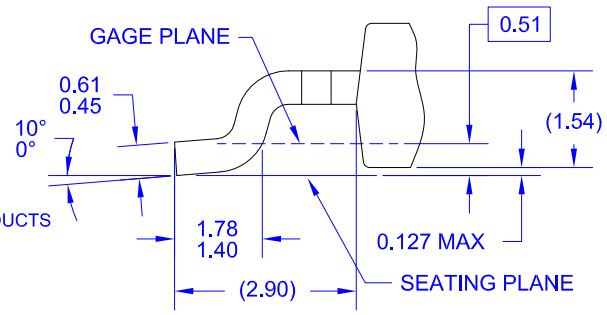


NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A
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SCALE: 12X

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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