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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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## RENESAS

# MOS FIELD EFFECT TRANSISTOR NP52N055SUG

### SWITCHING N-CHANNEL POWER MOS FET

#### DESCRIPTION

The NP52N055SUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

#### FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance

 $R_{DS(on)}$  = 14 m $\Omega$  MAX. (V<sub>GS</sub> = 10 V, I<sub>D</sub> = 26 A)

• Low Ciss: Ciss = 2100 pF TYP.

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGS = 0 V)	VDSS	55	V
Gate to Source Voltage (VDs = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	D(DC)	±52	А
Drain Current (pulse) Note1	D(pulse)	±170	А
Total Power Dissipation (Tc = $25^{\circ}$ C)	PT1	56	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	Pt2	1.2	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	–55 to +175	°C
Repetitive Avalanche Current Note2	lar	21	А
Repetitive Avalanche Energy Note2	Ear	44	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

**2.** Tch  $\leq$  150°C, VDD = 28 V, RG = 25  $\Omega$ , VGS = 20  $\rightarrow$  0 V

#### THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	2.68	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	125	°C/W

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#### ORDERING INFORMATION

PART NUMBER	PACKAGE
NP52N055SUG	TO-252 (MP-3ZK)



(TO-252)

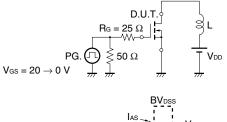
ELECTRICAL CHARACTERISTICS (TA = 25°C)

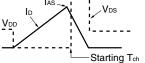
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 55 V, V <sub>GS</sub> = 0 V			1.0	μA
Gate Leakage Current	lgss	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{\text{GS(th)}}$	Vds = Vgs, Id = 250 <i>µ</i> A	2.0	3.0	4.0	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 26 A	8	17		S
Drain to Source On-state Resistance Note	RDS(on)	Vgs = 10 V, Id = 26 A		11	14	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 25 V		2100	3200	pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		170	260	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		110	200	pF
Turn-on Delay Time	<b>t</b> d(on)	V <sub>DD</sub> = 28 V, I <sub>D</sub> = 26 A		17	38	ns
Rise Time	tr	V <sub>GS</sub> = 10 V		14	35	ns
Turn-off Delay Time	td(off)	Rg = 0 Ω		47	94	ns
Fall Time	tr			7	18	ns
Total Gate Charge	QG	V <sub>DD</sub> = 44 V		38	57	nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		8		nC
Gate to Drain Charge	Qgd	ID = 52 A		13		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 52 A, VGS = 0 V		0.97	1.5	V
Reverse Recovery Time	trr	IF = 52 A, VGS = 0 V		32		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		34		nC

Note Pulsed

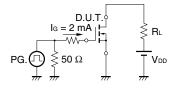
#### TEST CIRCUIT 1 AVALANCHE CAPABILITY

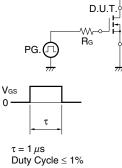
#### **TEST CIRCUIT 2 SWITCHING TIME**

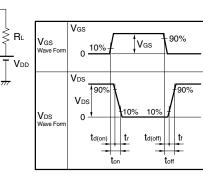




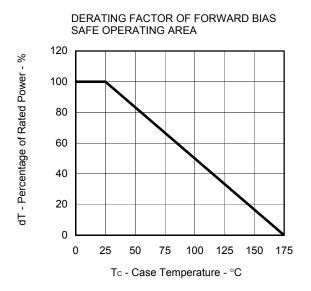
#### TEST CIRCUIT 3 GATE CHARGE

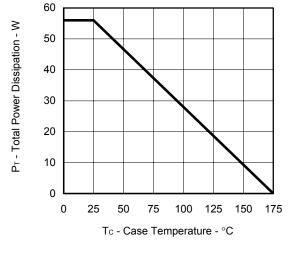






#### TYPICAL CHARACTERISTICS ( $T_A = 25^{\circ}C$ )

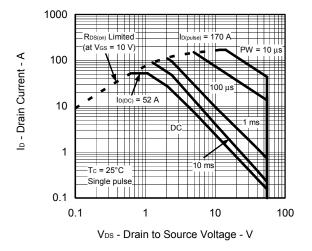


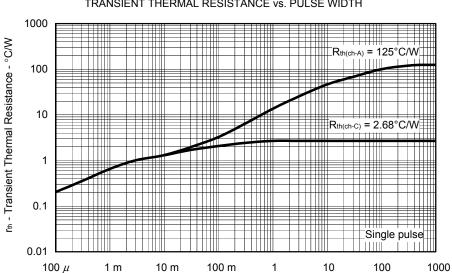


TOTAL POWER DISSIPATION vs.

CASE TEMPERATURE

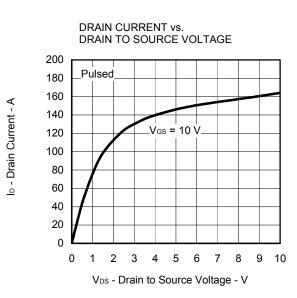
FORWARD BIAS SAFE OPERATING AREA



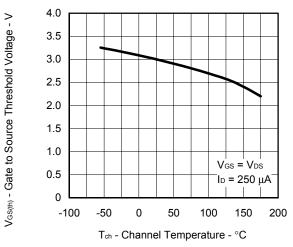


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

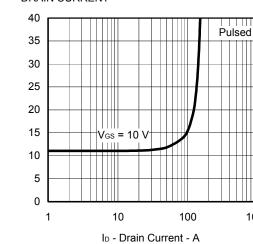
PW - Pulse Width - s



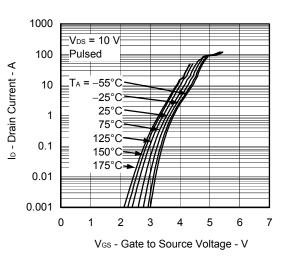




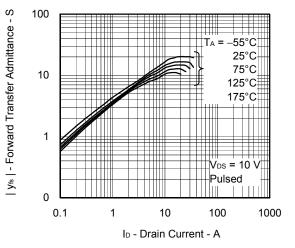
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



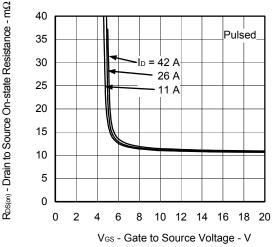




FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



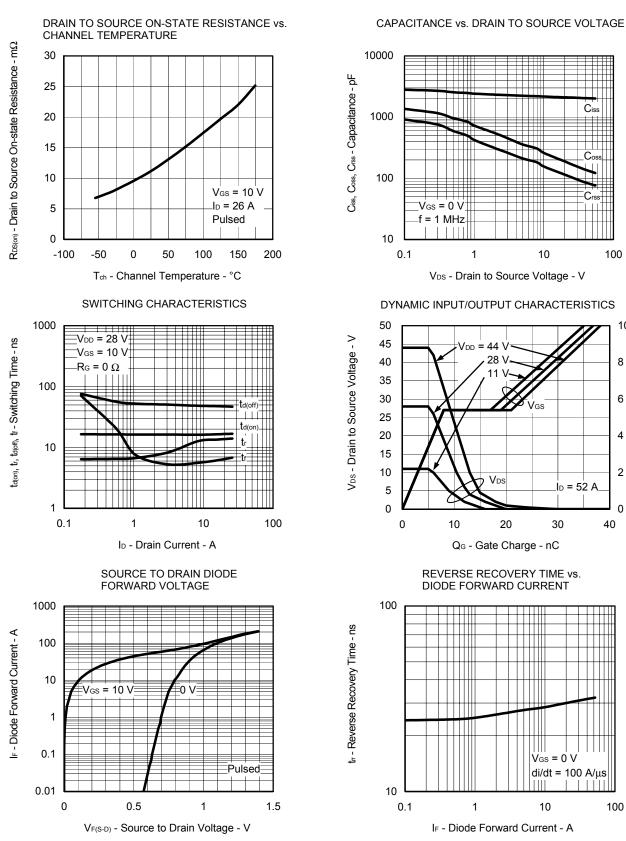
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



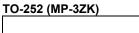
1000

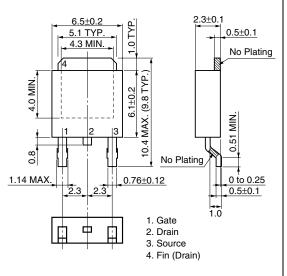
 $R_{DS(cn)}$  - Drain to Source On-state Resistance - m $\Omega$ 

V<sub>GS</sub> - Gate to Source Voltage - V

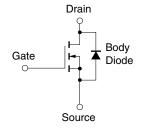


#### ★ PACKAGE DRAWING (Unit: mm)





#### EQUIVALENT CIRCUIT



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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