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AMIS-30660

High Speed CAN Transceiver

Description

The AMIS-30660 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

Due to the wide common-mode voltage range of the receiver inputs, the AMIS-30660 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

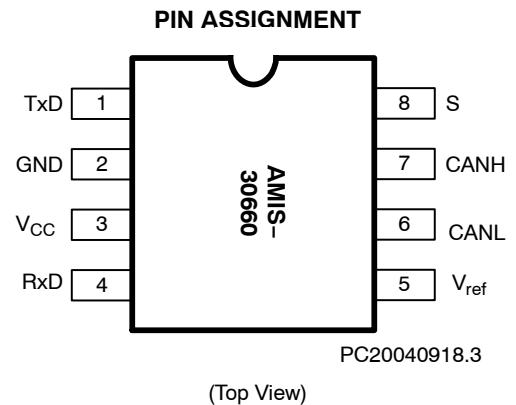
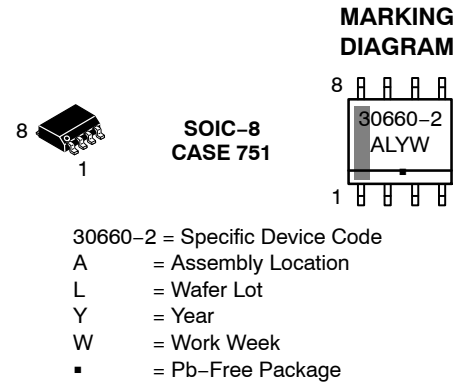
Features

- Fully Compatible with the ISO 11898-2 Standard
- Certified “Authentication on CAN Transceiver Conformance (d1.1)”
- High Speed (up to 1 Mbit/s)
- Ideally Suited for 12 V and 24 V Industrial and Automotive Applications
- Low EME Common-Mode Choke is No Longer Required
- Differential Receiver with Wide Common-Mode Range (± 35 V) for High EMS
- No Disturbance of the Bus Lines with an Unpowered Node
- Transmit Data (TxD) Dominant Time-out Function
- Thermal Protection
- Bus Pins Protected Against Transients in an Automotive Environment
- Silent Mode in which the Transmitter is Disabled
- Short Circuit Proof to Supply Voltage and Ground
- Logic Level Inputs Compatible with 3.3 V Devices
- These are Pb-Free Devices*



ON Semiconductor®

<http://onsemi.com>



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 1. TECHNICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------------|---|--|------|-----|------|
| V_{CANH} | DC Voltage at Pin CANH | $0 < V_{CC} < 5.25 \text{ V}$; No Time Limit | -45 | +45 | V |
| V_{CANL} | DC Voltage at Pin CANL | $0 < V_{CC} < 5.25 \text{ V}$; No Time Limit | -45 | +45 | V |
| $V_{o(dif)(bus_dom)}$ | Differential Bus Output Voltage in Dominant State | $42.5 \Omega < R_{LT} < 60 \Omega$ | 1.5 | 3 | V |
| $t_{pd(rec-dom)}$ | Propagation Delay TxD to RxD | See Figure 6 | 70 | 245 | ns |
| $t_{pd(dom-rec)}$ | Propagation Delay TxD to RxD | See Figure 6 | 100 | 245 | ns |
| $C_{M-range}$ | Input Common-Mode Range for Comparator | Guaranteed Differential Receiver Threshold and Leakage Current | -35 | +35 | V |
| $V_{CM-peak}$ | Common-Mode Peak | See Figures 7 and 8 (Note 1) | -500 | 500 | mV |
| $V_{CM-step}$ | Common-Mode Step | See Figures 7 and 8 (Note 1) | -150 | 150 | mV |

1. The parameters $V_{CM-peak}$ and $V_{CM-step}$ guarantee low electromagnetic emission.

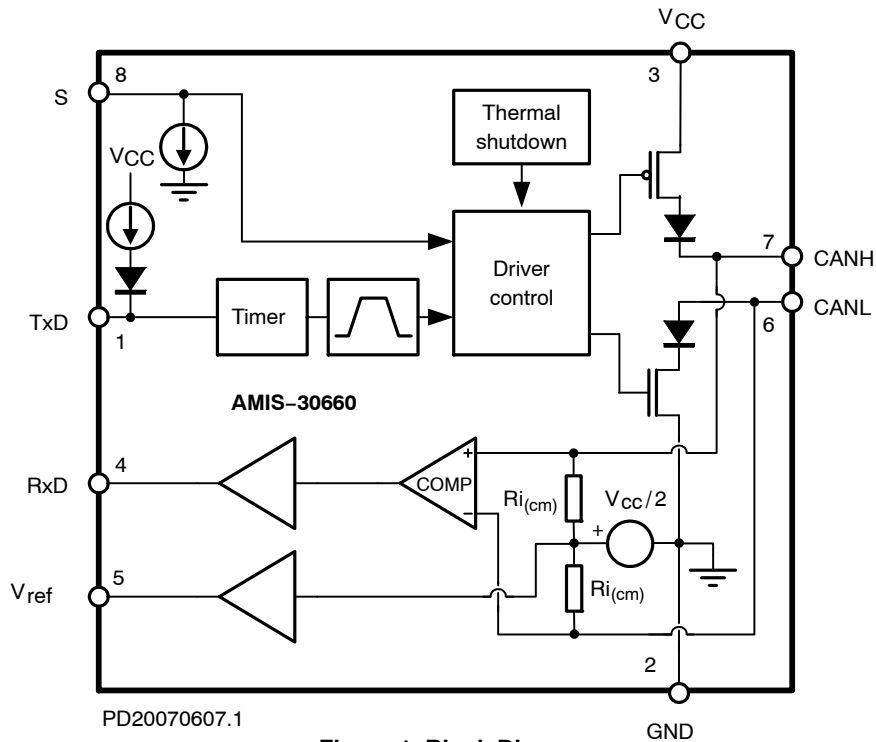


Figure 1. Block Diagram

Table 2. PIN LIST AND DESCRIPTIONS

| Pin | Name | Description |
|-----|------------------|--|
| 1 | TxD | Transmit data input; low input → dominant driver; internal pull-up current |
| 2 | GND | Ground |
| 3 | V _{CC} | Supply voltage |
| 4 | RxD | Receive data output; dominant transmitter → low output |
| 5 | V _{REF} | Reference voltage output |
| 6 | CANL | Low-level CAN bus line (low in dominant mode) |
| 7 | CANH | High-level CAN bus line (high in dominant mode) |
| 8 | S | Silent mode control input; internal pull-down current |

Table 3. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------------|---|--|------------|-----------------------|---------|
| V _{CC} | Supply Voltage | | -0.3 | +7 | V |
| V _{CANH} | DC Voltage at Pin CANH | 0 < V _{CC} < 5.25 V; No Time Limit | -45 | +45 | V |
| V _{CANL} | DC Voltage at Pin CANL | 0 < V _{CC} < 5.25 V; No Time Limit | -45 | +45 | V |
| V _{TxD} | DC Voltage at Pin TxD | | -0.3 | V _{CC} + 0.3 | V |
| V _{RxD} | DC Voltage at Pin RxD | | -0.3 | V _{CC} + 0.3 | V |
| V _S | DC Voltage at Pin S | | -0.3 | V _{CC} + 0.3 | V |
| V _{ref} | DC Voltage at Pin V _{REF} | | -0.3 | V _{CC} + 0.3 | V |
| V _{tran(CANH)} | Transient Voltage at Pin CANH | (Note 2) | -150 | +150 | V |
| V _{tran(CANL)} | Transient Voltage at Pin CANL | (Note 2) | -150 | +150 | V |
| V _{esd} | Electrostatic Discharge Voltage at All Pins | (Note 3) (Note 5) | -4 -500 | +4 +500 | kV V |
| Latchup | Static Latchup at All Pins | (Note 4) | | 100 | mA |
| T _{stg} | Storage Temperature | | -55 | +155 | °C |
| T _{amb} | Ambient Temperature | | -40 | +125 | °C |
| T _{Junc} | Maximum Junction Temperature | | -40 | +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Applied transient waveforms in accordance with ISO 7637 part 3, test pulses 1, 2, 3a, and 3b (see Figure 4).
3. Standardized human body model ESD pulses in accordance to MIL883 method 3015.7.
4. Static latch-up immunity: static latch-up protection level when tested according to EIA/JESD78.
5. Standardized charged device model ESD pulses when tested according to EOS/ESD DS5.3-1993.

Table 4. THERMAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Value | Unit |
|-----------------------|---|-------------|-------|------|
| R _{th(vj-a)} | Thermal Resistance from Junction-to-Ambient in SOIC-8 Package | In Free Air | 150 | K/W |
| R _{th(vj-s)} | Thermal resistance from Junction-to-Substrate of Bare Die | In Free Air | 45 | K/W |

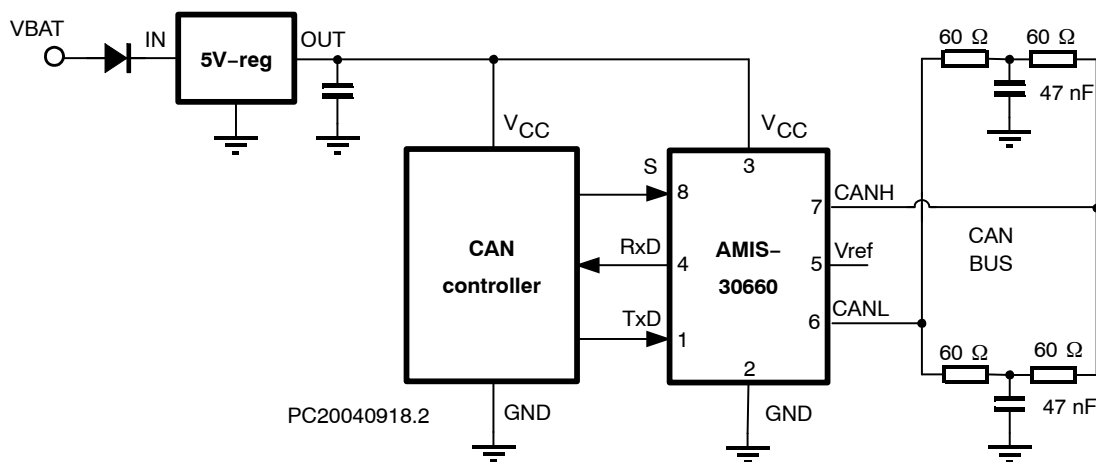


Figure 2. Application Diagram

FUNCTIONAL DESCRIPTION

Operating Modes

The behavior of AMIS-30660 under various conditions is illustrated in Table 5 below. In case the device is powered, one of two operating modes can be selected through Pin S.

Table 5. FUNCTIONAL TABLE OF AMIS-30660 (X = DON'T CARE)

| VCC | Pin TxD | Pin S | Pin CANH | Pin CANL | Bus State | Pin RxD |
|---|-----------------|-----------------|--------------------------------------|--------------------------------------|-----------|---------|
| 4.75 V to 5.25 V | 0 | 0 (or Floating) | High | Low | Dominant | 0 |
| 4.75 V to 5.25 V | X | 1 | $V_{CC} / 2$ | $V_{CC} / 2$ | Recessive | 1 |
| 4.75 V to 5.25 V | 1 (or Floating) | X | $V_{CC} / 2$ | $V_{CC} / 2$ | Recessive | 1 |
| $V_{CC} < \text{PORL}$ (Unpowered) | X | X | $0 \text{ V} < \text{CANH} < V_{CC}$ | $0 \text{ V} < \text{CANL} < V_{CC}$ | Recessive | 1 |
| $\text{PORL} < V_{CC} < 4.75 \text{ V}$ | $> 2 \text{ V}$ | X | $0 \text{ V} < \text{CANH} < V_{CC}$ | $0 \text{ V} < \text{CANL} < V_{CC}$ | Recessive | 1 |

High-Speed Mode

If Pin S is pulled low (or left floating), the transceiver is in its high-speed mode and is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the Pins TxD and RxD. The slopes on the bus line outputs are optimized to give extremely low electromagnetic emissions.

Silent Mode

In silent mode, the transmitter is disabled. All other IC functions continue to operate. The silent mode is selected by connecting Pin S to V_{CC} and can be used to prevent network communication from being blocked, due to a CAN controller which is out of control.

Overtemperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 160°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when Pin TxD goes high. The thermal protection

circuit is particularly necessary when a bus line short-circuits.

TxD Dominant Time-out Function

A TxD dominant time-out timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if Pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low-level on Pin TxD exceeds the internal timer value t_{dom} , the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on Pin TxD.

Fail-Safe Features

A current-limiting circuit protects the transmitter output stage from damage caused by an accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The Pins CANH and CANL are protected from automotive electrical transients (according to “ISO 7637”; see Figure 3). Pin TxD is pulled high internally should the input become disconnected.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (Pin 2). Positive currents flow into the IC. Sinking current means the current

is flowing into the pin; sourcing current means the current is flowing out of the pin.

Table 6. DC AND TIMING CHARACTERISTICS

(V_{CC} = 4.75 V to 5.25 V; T_{junc} = -40°C to +150°C; R_{LT} = 60 Ω unless specified otherwise.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|---|---------------------------|---------------------------|---------------------------|------|
| SUPPLY (Pin V_{CC}) | | | | | | |
| I _{CC} | Supply Current | Dominant; V _{TxD} = 0 V Recessive; V _{TxD} = V _{CC} | 25 2 | 45 4 | 65 8 | mA |
| I _{CCS} | Supply Current in silent mode | V _S = V _{CC} | 2 | 4 | 8 | mA |
| TRANSMITTER DATA INPUT (Pin TxD) | | | | | | |
| V _{IH} | High-level input voltage | Output recessive | 2.0 | - | V _{CC} +0.3 | V |
| V _{IL} | Low-level input voltage | Output dominant | -0.3 | - | +0.8 | V |
| I _{IH} | High-level input current | V _{TxD} = V _{CC} | -1 | 0 | +1 | μA |
| I _{IL} | Low-level input current | V _{TxD} = 0 V | -75 | -200 | -350 | μA |
| C _i | Input capacitance | Not tested | - | 5 | 10 | pF |
| MODE SELECT (Pin S) | | | | | | |
| V _{IH} | High-level input voltage | Silent mode | 2.0 | - | V _{CC} +0.3 | V |
| V _{IL} | Low-level input voltage | High-speed mode | -0.3 | - | +0.8 | V |
| I _{IH} | High-level input current | V _S = 2 V | 20 | 30 | 50 | μA |
| I _{IL} | Low-level input current | V _S = 0.8 V | 15 | 30 | 45 | μA |
| RECEIVER DATA OUTPUT (Pin RxD) | | | | | | |
| V _{OH} | High-level output voltage | I _{RxD} = - 10 mA | 0.6 x V _{CC} | 0.75 x V _{CC} | | V |
| V _{OL} | Low-level output voltage | I _{RxD} = 6 mA | | 0.25 | 0.45 | V |
| REFERENCE VOLTAGE OUTPUT (Pin V_{ref}) | | | | | | |
| V _{REF} | Reference output voltage | -50 μA < I _{VREF} < +50 μA | 0.45 x V _{CC} | 0.50 x V _{CC} | 0.55 x V _{CC} | V |
| V _{REF_CM} | Reference output voltage for full common mode range | -35 V < V _{CANH} < +35V; -35 V < V _{CANL} < +35V | 0.40 x V _{CC} | 0.50 x V _{CC} | 0.60 x V _{CC} | V |
| BUS LINES (Pins CANH and CANL) | | | | | | |
| V _{o(reces)} (CANH) | Recessive bus voltage at pin CANH | V _{TxD} = V _{CC} ; no load | 2.0 | 2.5 | 3.0 | V |
| V _{o(reces)} (CANL) | Recessive bus voltage at pin CANL | V _{TxD} = V _{CC} ; no load | 2.0 | 2.5 | 3.0 | V |
| I _{o(reces)} (CANH) | Recessive output current at pin CANH | -35 V < V _{CANH} < +35 V; 0 V < V _{CC} < 5.25 V | -2.5 | - | +2.5 | mA |
| I _{o(reces)} (CANL) | Recessive output current at pin CANL | -35 V < V _{CANL} < +35 V; 0V < V _{CC} < 5.25 V | -2.5 | - | +2.5 | mA |
| V _{o(dom)} (CANH) | Dominant output voltage at pin CANH | V _{TxD} = 0 V | 3.0 | 3.6 | 4.25 | V |
| V _{o(dom)} (CANL) | Dominant output voltage at pin CANL | V _{TxD} = 0 V | 0.5 | 1.4 | 1.75 | V |
| V _{o(dif)} (bus) | Differential bus output voltage (V _{CANH} - V _{CANL}) | V _{TxD} = 0 V; dominant; 42.5 Ω < R _{LT} < 60 Ω | 1.5 | 2.25 | 3.0 | V |
| | | V _{TxD} = V _{CC} ; recessive; No load | -120 | 0 | +50 | mV |
| I _{o(sc)} (CANH) | Short circuit output current at pin CANH | V _{CANH} = 0 V; V _{TxD} = 0 V | -45 | -70 | -95 | mA |
| I _{o(sc)} (CANL) | Short circuit output current at pin CANL | V _{CANL} = 36V; V _{TxD} = 0V | 45 | 70 | 120 | mA |

Table 6. DC AND TIMING CHARACTERISTICS

($V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $T_{junc} = -40^{\circ}\text{C to }+150^{\circ}\text{C}$; $R_{LT} = 60\ \Omega$ unless specified otherwise.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|--|------|------|------|--------------------|
| BUS LINES (Pins CANH and CANL) | | | | | | |
| $V_{i(dif)}(th)$ | Differential receiver threshold voltage | $-5\text{ V} < V_{CANL} < +10\text{ V}$; $-5\text{ V} < V_{CANH} < +10\text{ V}$; See Figure 4 | 0.5 | 0.7 | 0.9 | V |
| $V_{ihcm(dif)}(th)$ | Differential receiver threshold voltage for high common-mode | $-35\text{ V} < V_{CANL} < +35\text{ V}$; $-35\text{ V} < V_{CANH} < +35\text{ V}$; See Figure 4 | 0.25 | 0.7 | 1.05 | V |
| $V_{i(dif)}(hys)$ | Differential receiver input voltage hysteresis | $-5\text{ V} < V_{CANL} < +10\text{ V}$; $-5\text{ V} < V_{CANH} < +10\text{ V}$; See Figure 4 | 50 | 70 | 100 | mV |
| $R_{i(cm)}(CANH)$ | Common-mode input resistance at pin CANH | | 15 | 25 | 37 | K Ω |
| $R_{i(cm)}(CANL)$ | Common-mode input resistance at pin CANL | | 15 | 25 | 37 | K Ω |
| $R_{i(cm)}(m)$ | Matching between pin CANH and pin CANL common-mode input resistance | $V_{CANH} = V_{CANL}$ | -3 | 0 | +3 | % |
| $R_{i(dif)}$ | Differential input resistance | | 25 | 50 | 75 | K Ω |
| $C_{i(CANH)}$ | Input capacitance at pin CANH | $V_{TxD} = V_{CC}$; not tested | | 7.5 | 20 | pF |
| $C_{i(CANL)}$ | Input capacitance at pin CANL | $V_{TxD} = V_{CC}$; not tested | | 7.5 | 20 | pF |
| $C_{i(dif)}$ | Differential input capacitance | $V_{TxD} = V_{CC}$; not tested | | 3.75 | 10 | pF |
| $I_{LI}(CANH)$ | Input leakage current at pin CANH | $V_{CC} = 0\text{ V}$; $V_{CANH} = 5\text{ V}$ | 10 | 170 | 250 | μA |
| $I_{LI}(CANL)$ | Input leakage current at pin CANL | $V_{CC} = 0\text{ V}$; $V_{CANL} = 5\text{ V}$ | 10 | 170 | 250 | μA |
| $V_{CM-peak}$ | Common-mode peak during transition from dom \rightarrow rec or rec \rightarrow dom | See Figures 7 and 8 | -500 | | 500 | mV |
| $V_{CM-step}$ | Difference in common-mode between dominant and recessive state | See Figures 7 and 8 | | -150 | 150 | mV |
| POWER-ON-RESET (POR) | | | | | | |
| PORL | POR level | CANH, CANL, V_{ref} in tri-state below POR level | 2.2 | 3.5 | 4.5 | V |
| THERMAL SHUTDOWN | | | | | | |
| $T_{j(sd)}$ | Shutdown junction temperature | | 150 | 160 | 180 | $^{\circ}\text{C}$ |
| TIMING CHARACTERISTICS (see Figures 5 and 6) | | | | | | |
| $t_{d(TxD-BUSon)}$ | Delay TxD to bus active | $V_s = 0\text{ V}$ | 40 | 85 | 130 | ns |
| $t_{d(TxD-BUSoff)}$ | Delay TxD to bus inactive | $V_s = 0\text{ V}$ | 30 | 60 | 105 | ns |
| $t_{d(BUSon-RxD)}$ | Delay bus active to RxD | $V_s = 0\text{ V}$ | 25 | 55 | 105 | ns |
| $t_{d(BUSoff-RxD)}$ | Delay bus inactive to RxD | $V_s = 0\text{ V}$ | 65 | 100 | 135 | ns |
| $t_{pd(rec-dom)}$ | Propagation delay TxD to RxD from recessive to dominant | $V_s = 0\text{ V}$ | 70 | | 245 | ns |
| $t_{d(dom-rec)}$ | Propagation delay TxD to RxD from dominant to recessive | $V_s = 0\text{ V}$ | 100 | | 245 | ns |
| $t_{dom(TxD)}$ | TxD dominant time for time out | $V_{TxD} = 0\text{ V}$ | 250 | 450 | 750 | μs |

AMIS-30660

MEASUREMENT SEUPS AND DEFINITIONS

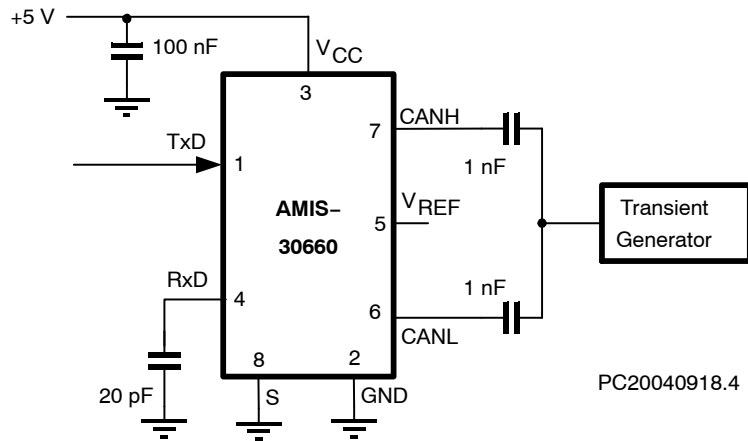


Figure 3. Test Circuit for Automotive Transients

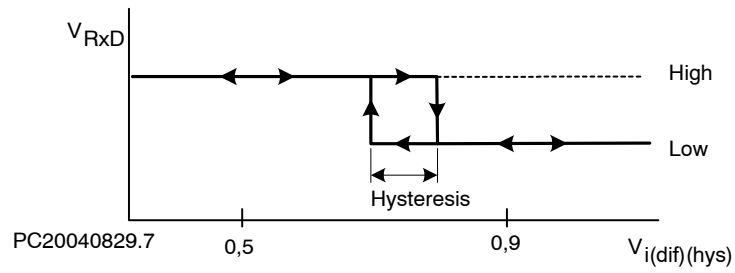


Figure 4. Hysteresis of the Receiver

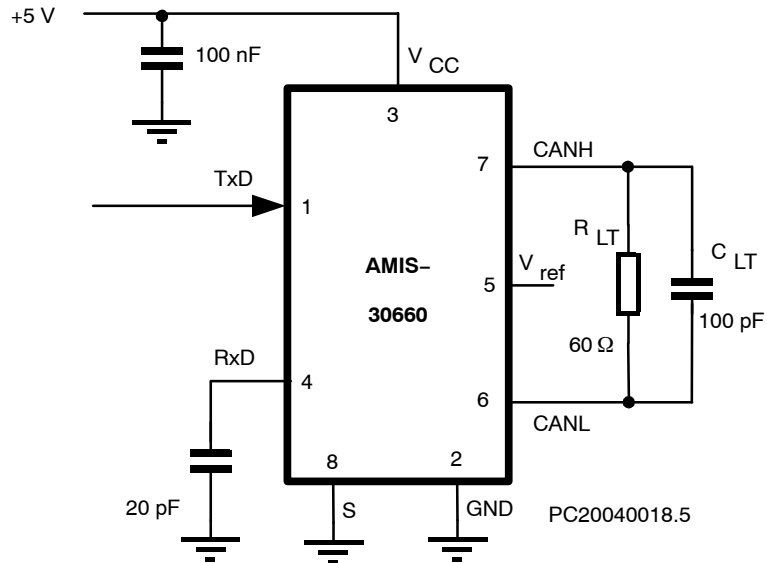


Figure 5. Test Circuit for Timing Characteristics

AMIS-30660

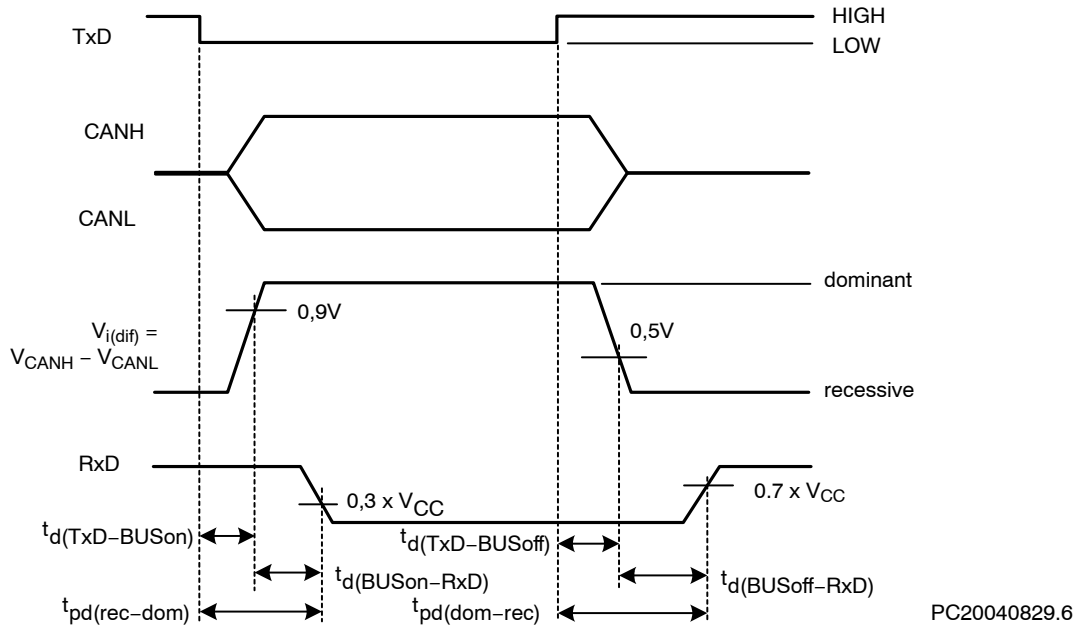


Figure 6. Timing Diagram for AC Characteristics

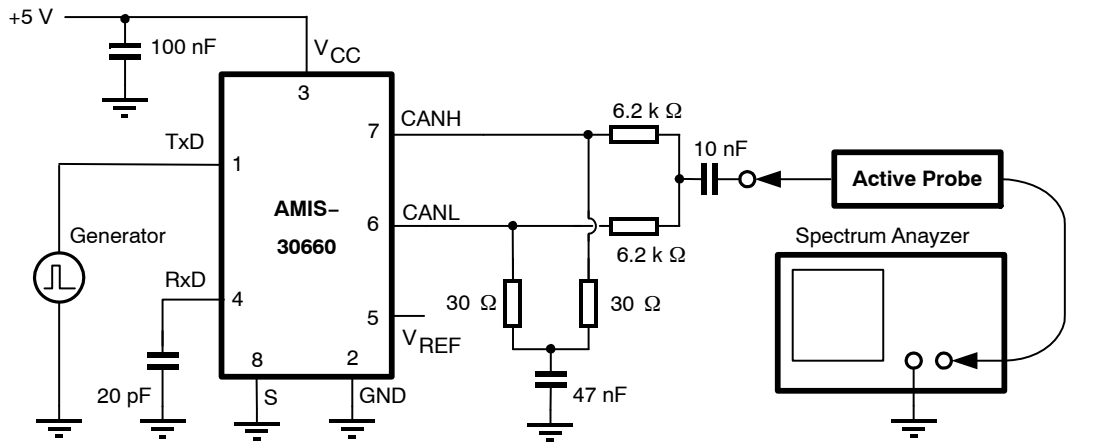


Figure 7. Basic Test Set-up for Electromagnetic Measurement

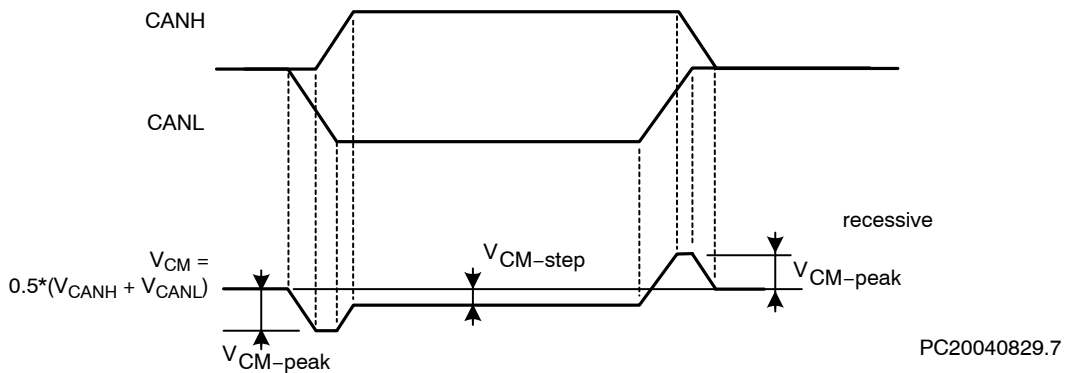


Figure 8. Common-Mode Voltage Peaks (see Measurement Setup)

AMIS-30660

DEVICE ORDERING INFORMATION

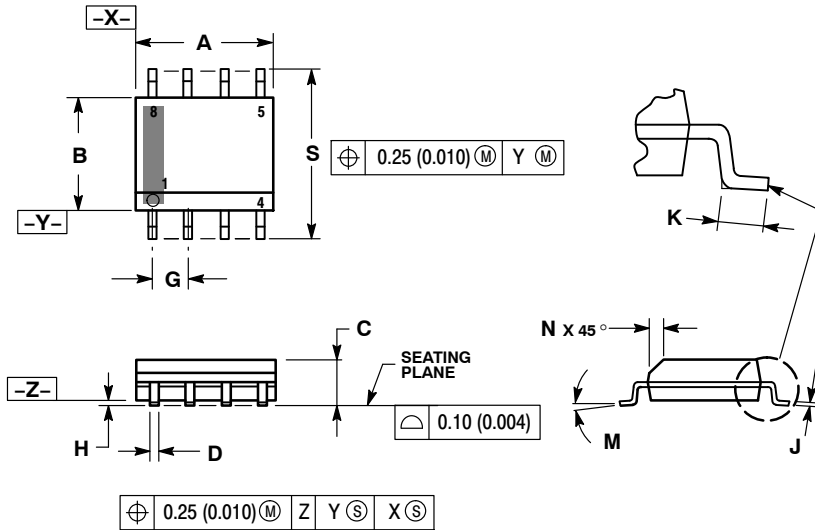
| Part Number | Description | Temperature Range | Package Type | Shipping† |
|------------------|---------------------------------|-------------------|---------------------|--------------------|
| AMIS30660CANH2G | HS CAN Transc. (5 V) (Matte Sn) | -40°C – 125°C | SOIC-8 (Pb-Free) | 96 Tube / Tray |
| AMIS30660CANH2RG | HS CAN Transc. (5 V) (Matte Sn) | -40°C – 125°C | SOIC-8 (Pb-Free) | 3000 / Tape & Reel |
| AMIS30660CANH6G | HS CAN Transc. (5 V) (NiPdAu) | -40°C – 125°C | SOIC-8 (Pb-Free) | 96 Tube / Tray |
| AMIS30660CANH6RG | HS CAN Transc. (5 V) (NiPdAu) | -40°C – 125°C | SOIC-8 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

AMIS-30660

PACKAGE DIMENSIONS

SOIC-8
CASE 751-07
ISSUE AK

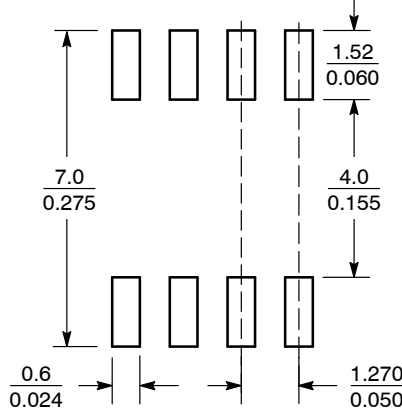


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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