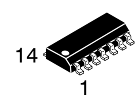
Half-Bridge Gate Driver

1200 V 2.5 A Source/3.4 A Sink

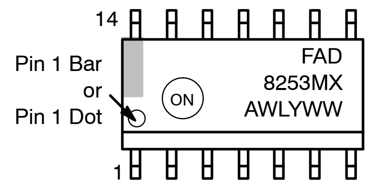
FAD8253MX-1

DATA SHEET
www.onsemi.com



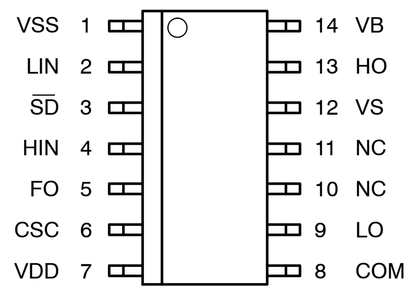
SOIC−14 NB
CASE 751A

MARKING DIAGRAM



FAD8253MX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FAD8253MX−1	SOIC−14 NB (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Description

The FAD8253 is a monolithic half−bridge gate driver IC designed for driving high voltage, high speed and high power IGBTs up to +1200 V. The FAD8253 employs ON's high−voltage process and common−mode noise canceling technique to provide stable operation of high−side driver under high dv/dt noise circumstances. The gate driver includes UVLO circuits tailored to IGBT threshold for both high side and low side outputs to prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The FAD8253 offers a built−in low−side current detection circuitry with an additional provision for soft shutdown (for low side) during overcurrent or short−circuit conditions. The driver can provide adequate protection during short−circuits by turning off its outputs while simultaneously generating a fault output for fault reporting purposes. The driver also provides additional flexibility by providing a shutdown pin to disable driver outputs externally.

Features

- Floating Channel for Bootstrap Operation to +1200 V
- Peak Output Current Capability of 2.5 A Source/3.4 A Sink
- Allowable Negative V_S Transient Swing of up to −15 V at V_{BS} = 15 V
- Built−in Common Mode dv/dt Noise Canceling Circuit
- Separate Power and Signal Ground for Enhanced dI/dt Immunity
- Matched Propagation Delay < 50 ns
- 3.3 V and 5 V Input Logic Compatible
- Built in Shoot−through Prevention Logic with 120 ns (Typ) Dead Time
- Built−in UVLO Functions for both High and Low Side with Thresholds Optimized for IGBTs
- Built−in Low Side Short−circuit Protection with Soft Shutdown
- In SOIC14NB with Non Connected Pins for High Voltage Creepage and Clearance Requirements
- Fault Reporting during Overcurrent or Short−circuit Condition
- External Shutdown Pin to Enable or Disable Driver Outputs
- AEC−Q100 Qualified and PPAP Capable
- Pb−Free Devices

Typical Applications

- High Voltage Auxiliary Motor Drive
- Generic Half−Bridge and Full−Bridge Driver
- On−Board Chargers & DC/DC Converters
- Traction Inverters

August, 2022 − Rev. 3

Publication Order Number:
FAD8253/D

APPLICATION DIAGRAMS

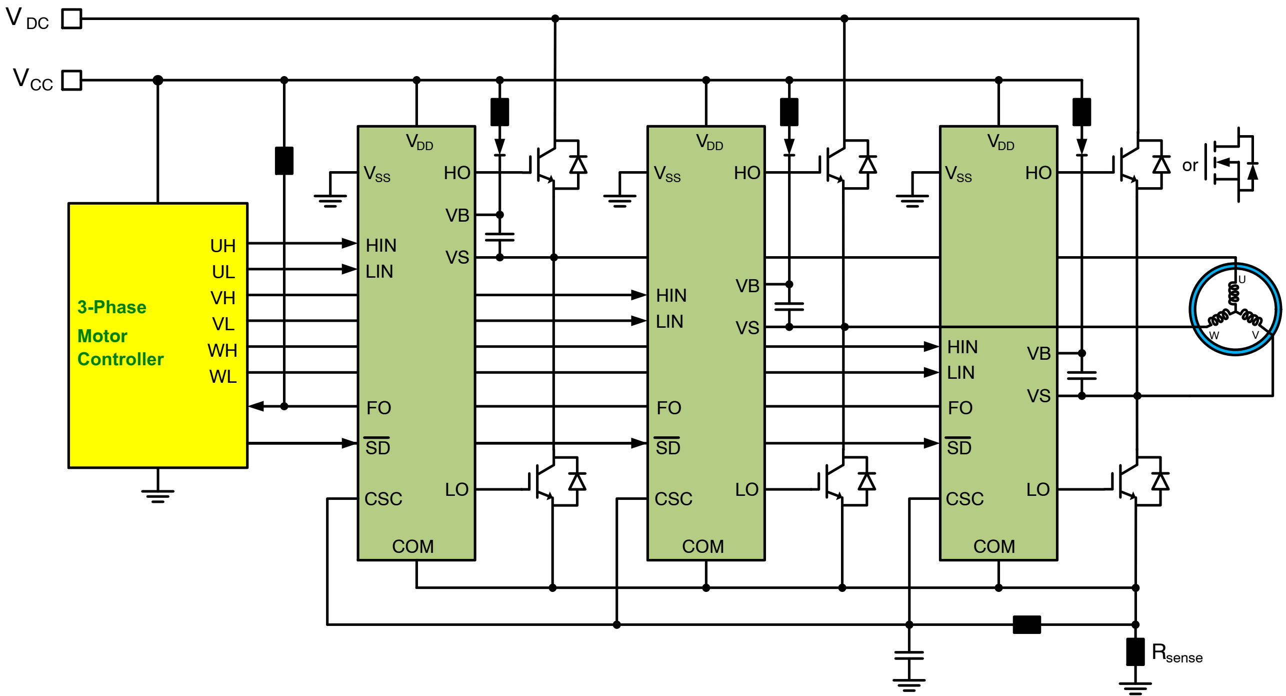


Figure 1. 3−Phase Motor Drive Application

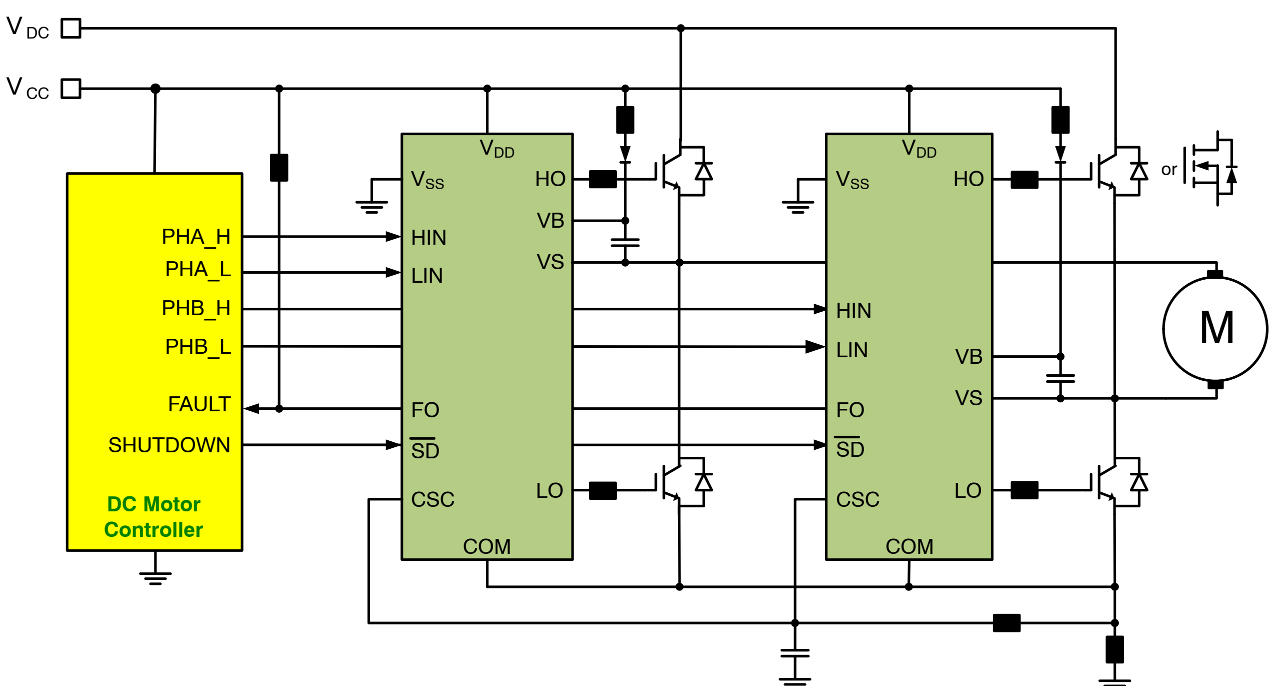


Figure 2. DC Motor Drive Application

BLOCK DIAGRAM

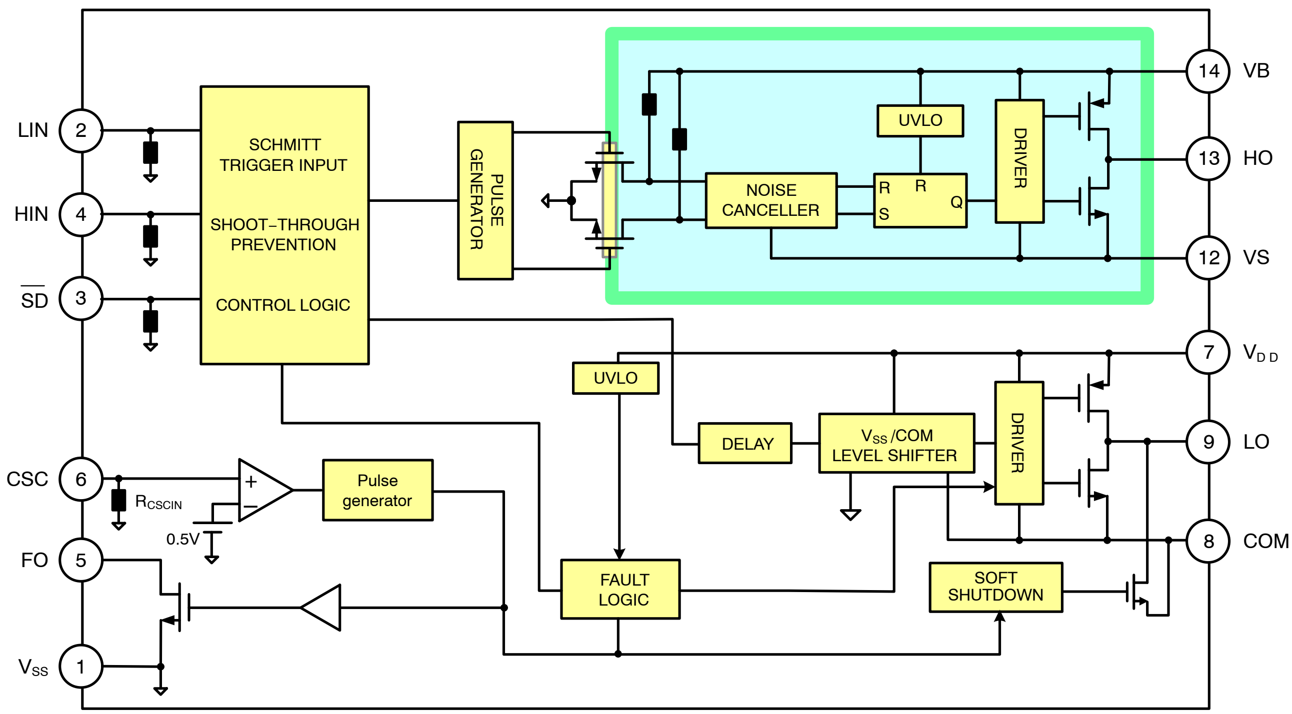


Figure 3. Block Diagram

PIN DESCRIPTION

PIN FUNCTION DESCRIPTION

Pin No.	Name	Description
1	VSS	Logic Ground
2	LIN	Logic Input for Low−Side Gate Driver Output
3	$\overline{SD}$	Shutdown Control Input with Active Low
4	HIN	Logic Input for High−Side Gate Driver Output
5	FO	Fault Output with Open Drain (Low True)
6	CSC	Short−Circuit Current Detection Input
7	VDD	Low−Side and Logic Power Supply Voltage
8	COM	Low−side Driver Return
9	LO	Low−Side Driver Output
12	VS	High−Side Floating Supply Return
13	HO	High−Side Driver Output
14	VB	High−Side Floating Supply
10, 11	NC	No Connect

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified.)

Symbol	Rating	Value	Unit
V_S	High−side Offset Voltage V_S	(V_B – 25) to (V_B + 0.3)	V
V_B	High−side Floating Supply Voltage V_B	−0.3 to 1225	V
V_{HO}	High−side Floating Output Voltage	(V_S – 0.3) to (V_B + 0.3)	V
V_{DD}	Low−side and Logic−fixed Supply Voltage	−0.3 to 25	V
V_{IN}	Logic Input Voltage (HIN, LIN, $\overline{SD}$)	−0.3 to (V_{DD} + 0.3)	V
V_{CSC}	Current Sense Input Voltage	−0.3 to (V_{DD} + 0.3)	V
dV_S/dt	Allowable Offset Voltage Slew Rate	50	V/ns
P_D	Power Dissipation (SO14NB) (Note 1)	0.8	W
θ_{JA}	Thermal Resistance, Junction−to−Ambient (SO14NB)	156	°C/W
$T_{J(max)}$	Junction Temperature	+150	°C
TSTG	Storage Temperature	−55 to +150	°C
ESDHBM	ESD, Human Body Model (Note 3)	2500	V
ESDCDM	ESD, Charged Device Model (Note 3)	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Do not exceed PD under any circumstances.
2. Mounted on 76.2 × 114.3 × 1.6 mm PCB (FR−4 glass epoxy material). Refer to the following standards:
   – JESD51−2: Integral circuits thermal test method environmental conditions – natural convection
   – JESD51−3: Low effective thermal conductivity test board for leaded surface mount packages
3. This device series incorporates ESD protection and is tested by the following methods:
   – ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001−2012
   – ESD Charged Device Model tested per JESD22−C101

RECOMMENDED OPERATING RANGES (Parameters are referenced to V_{SS})

Symbol	Rating	Min	Max	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_S	High−Side V_S Floating Supply Offset Voltage (Note 4)	5 – V_{BS}	1200	V
V_{BS}	High−side V_{BS} Bootstrap Voltage	V_{BSUV+}	22	V
V_{HO}	High−Side Output Voltage	V_S	V_B	V
V_{DD}	Low−Side and Logic Supply Voltage	V_{DDUV+}	22	V
V_{LO}	Low−Side Output Voltage	COM	V_{DD}	V
V_{IN}	Logic Input Voltage (IN, $\overline{SD}$)	V_{SS}	V_{DD}	V
COM	Power Ground	V_{DD} – 22	V_{DD}	V
T_A	Ambient Temperature (Note 5)	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Recommended based on min 5 V on V_B, for proper operation of the level shifter circuit and ensure proper propagation of the signal from the input to the output.
5. Power and thermal impedance should be determined with care so that T_j does not exceed 150°C.

ELECTRICAL CHARACTERISTICS

(V_{BIAS} (V_{DD}, V_{BS}) = 15 V, T_A = −40°C to 125°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS}. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LOW SIDE POWER SUPPLY SECTION						
I_{QDD}	Quiescent V_{DD} Supply Current	V_{LIN} = 0 V or 5 V	50	280	400	μA
I_{PDD}	Operating V_{DD} Supply Current	C_L = 1 nF, f_{LIN} = 20 kHz, rms value	400	660	800	μA
V_{DDUV+}	V_{DD} Supply Under−Voltage Positive−going Threshold	V_{DD} = Rising	11	12	12.9	V
V_{DDUV-}	V_{DD} Supply Under−voltage Negative going Threshold	V_{DD} = Falling	10.5	11.4	12.4	V
V_{DDHYS}	V_{DD} Supply Under−voltage Lockout Hysteresis		–	0.6	–	V
BOOSTRAPPED POWER SUPPLY SECTION						
I_{QBS}	Quiescent V_{BS} Supply Current	V_{HIN} = 0 V or 5 V	–	25	45	μA
I_{PBS}	Operating V_{BS} Supply Current	C_L = 1 nF, f_{HIN} = 20 kHz, rms value	–	430	550	μA
I_{LK}	Offset Supply Leakage Current	V_B = V_S = 1200 V	–	–	120	μA
V_{BSUV+}	V_{BS} Supply Under−Voltage Positive−going Threshold	V_{BS} = Rising	10.6	11.7	12.5	V
V_{BSUV-}	V_{BS} Supply Under−voltage Negative Going Threshold	V_{BS} = Falling	10.1	11.1	11.9	V
V_{BSHYS}	V_{BS} Supply Under−voltage Lockout Hysteresis		–	0.6	–	V
GATE DRIVER OUTPUT SECTION						
V_{OH}	High−level Output Voltage, V_{BIAS}−V_O	I_O = 0 mA (No Load)	–	–	50	mV
V_{OL}	Low−level Output Voltage, V_O	I_O = 0 mA (No Load)	–	–	50	mV
I_{O+}	Output HIGH Short−circuit Pulsed Current	V_O = 0 V, V_{IN} = 5 V with PW < 10 μs	1200	2700	–	mA
I_{O-}	Output LOW Short−circuit Pulsed Current	V_O = 15 V, V_{IN} = 0 V with PW < 10 μs	1200	4200	–	mA
V_S	Allowable Negative V_S Pin Voltage, with Signal Propagation Capability from HIN to HO	V_{BS} = 15 V	−10.0	–	–	V
V_S (Note 6)	Allowable Transient Negative V_S Pin Voltage, No Signal Propagation Capability from HIN to HO	V_{BS} = 15 V	−15.0	–	–	V
COM−V_{SS}	Allowable COM−V_{SS} Power/Signal Grounds Offset	V_{DD} = 15 V, V_{SS} = 0 V	−7.0	–	–	V
LOGIC INPUT SECTION (HIN, LIN, $\overline{SD}$)						
V_{IH}	Logic “1” Input Voltage Threshold		–	–	2.5	V
V_{IL}	Logic “0” Input Voltage Threshold		1.2	–	–	V
V_{INHYS}	Logic Input Hysteresis Voltage		–	0.5	–	V
I_{IN+}	Logic “1” Input Bias Current (HIN, LIN)	V_{IN} = 5 V	–	23	–	μA
I_{IN-}	Logic “0” Input Bias Current (HIN, LIN)	V_{IN} = 0 V	–	–	2.0	μA
$I_{\overline{SD}+}$	Logic “1” Input Bias Current ($\overline{SD}$)	$V_{\overline{SD}}$ = 5 V	–	15.7	–	μA
$I_{\overline{SD}-}$	Logic “0” Input Bias Current ($\overline{SD}$)	$V_{\overline{SD}}$ = 0 V	–	–	2.0	μA
SHORT−CIRCUIT PROTECTION						
V_{CSCREF}	Short−circuit detector reference voltage		0.45	0.50	0.6	V
R_{CSCIN}	Input Pull Down Short Circuit Resistance		–	210	–	kΩ
I_{CSCIN}	Short−Circuit Input Current	V_{CSCIN} = 5 V	15	23.5	37.5	μA
I_{SOFT}	Soft Turn−off Source Current	V_{DD} = 15 V, L_O = 7.5 V	70	110	140	mA

ELECTRICAL CHARACTERISTICS (continued)
(V_{BIAS} (V_{DD}, V_{BS}) = 15 V, T_A = −40°C to 125°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS}. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
FAULT DETECTION SECTION						
V_{FOH}	Fault Output High Level Voltage	V_{CSC} = 0 V, $R_{PULL-UP}$ = 4.7 kΩ	4.7	–	–	V
V_{FOL}	Fault Output Low Level Voltage	V_{CSC} = 1 V, I_{FO} = 2 mA	–	–	0.8	V
DYNAMIC OUTPUT SECTION (V_{BIAS} (V_{DD}, V_{BS}) = 15.0 V, T_A = −40°C to 125°C, V_S = V_{SS}, C_{LOAD} = 1000 pF unless otherwise specified.)						
t_{on}	Turn−on Propagation Delay (Note 7)	V_S = 0 V	65	100	145	ns
t_{off}	Turn−off Propagation Delay	V_S = 0 V or 1200 V	65	90	145	ns
t_{SDOFF_LO}	$\overline{SD}$ to Low−side Propagation Delay		25	45	70	ns
t_{SDOFF_HO}	$\overline{SD}$ to How−side Propagation Delay		65	95	145	ns
t_r	Turn−on Rise Time		–	13	25	ns
t_f	Turn−off Fall Time		–	15	26	ns
Mt_{ON}	Delay Matching HO and LO Turn−On		–	–	25	ns
Mt_{OFF}	Delay Matching HO and LO Turn−Off		–	–	25	ns
DT	Dead−time (Note 8)		70	120	200	ns
t_{UVFLT}	Under−voltage Filtering Time (Note 6)		–	10	–	μs
t_{CSCFLT}	CSC Pin Filtering Time (Note 6)		–	300	–	ns
t_{CSCFO}	Time from CSC Triggering to FO		–	530	1250	ns
t_{FO}	Fault Output Pulse Width		24	65	140	μs
t_{CSCLO}	Time from CSC Triggering to Low−side and High−side Gate Output	From V_{CSC} = 1 V to starting gate turn−off	–	600	1350	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Parameter guaranteed by design.
7. The turn−on propagation delay does not includes the dead time.
8. The dead time includes the turn on propagation time.

TYPICAL CHARACTERISTICS

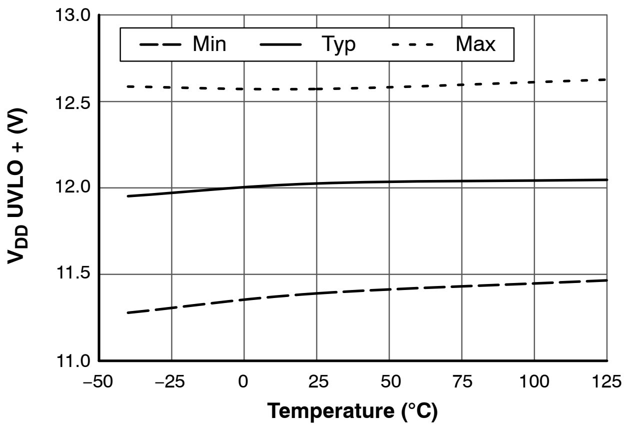


Figure 4. V_{DD} UVLO (+) vs. Temperature

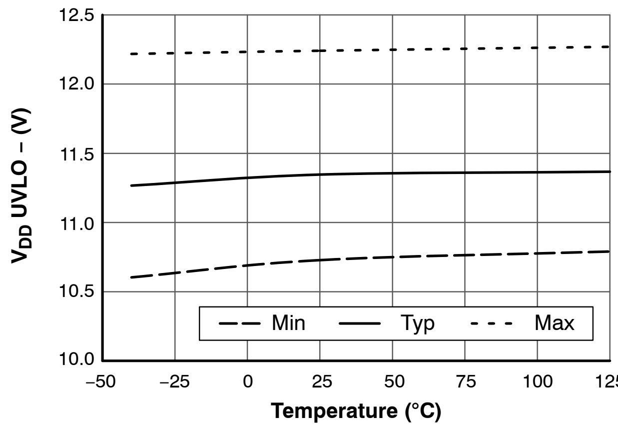


Figure 5. V_{DD} UVLO (−) vs. Temperature

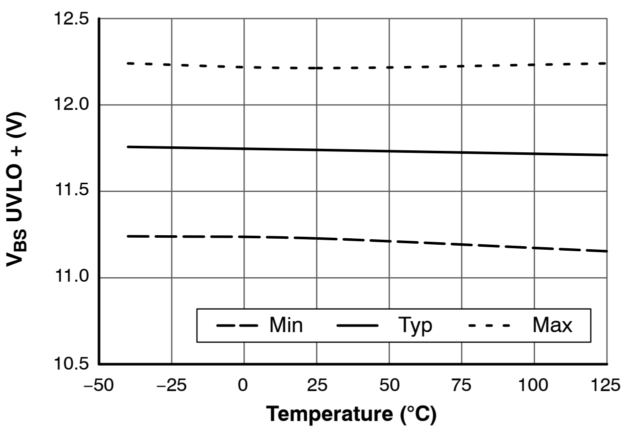


Figure 6. V_{BS} UVLO (+) vs. Temperature

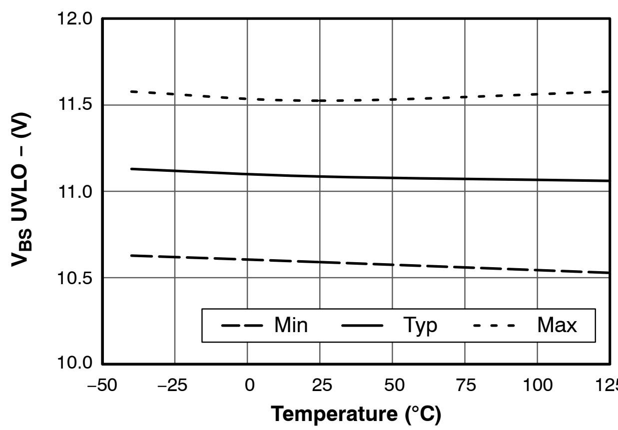


Figure 7. V_{BS} UVLO (−) vs. Temperature

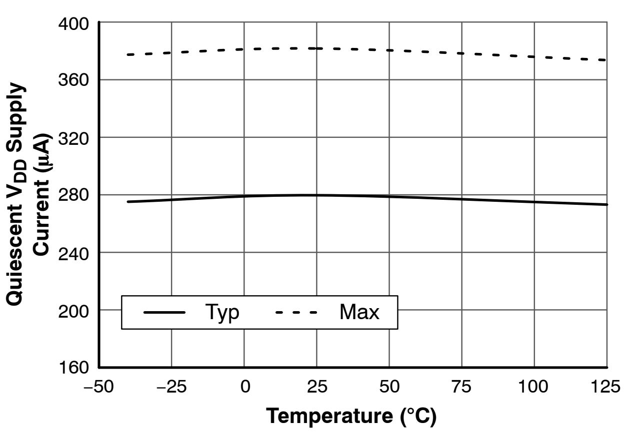


Figure 8. V_{DD} Quiescent Current vs. Temperature

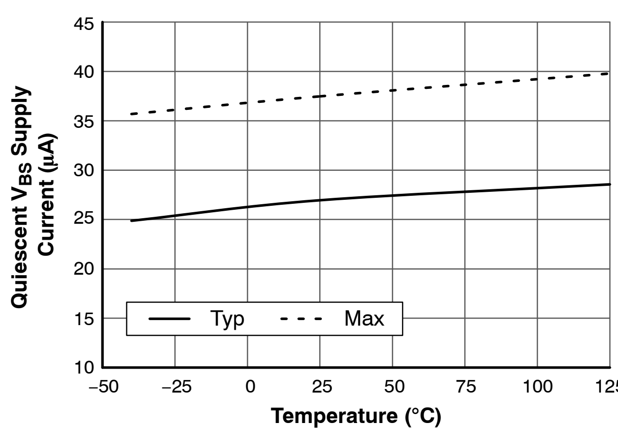


Figure 9. V_{BS} Quiescent Current vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

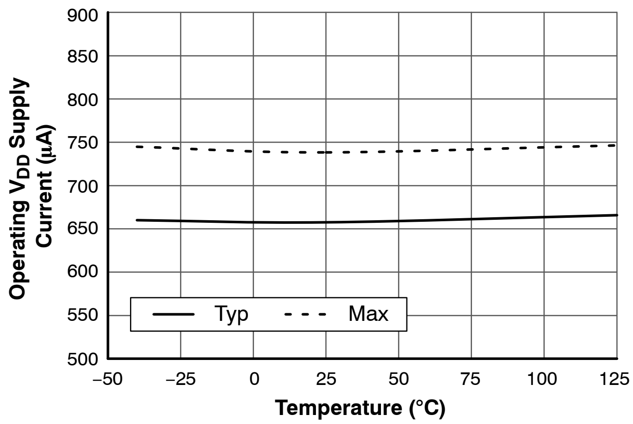


Figure 10. V_{DD} Operating Current vs. Temperature

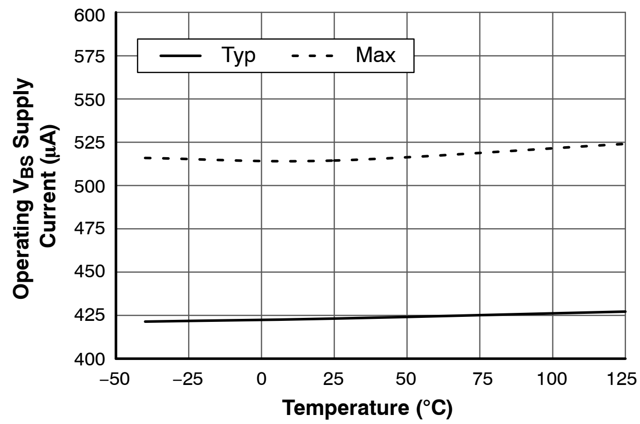


Figure 11. V_{BS} Operating Current vs. Temperature

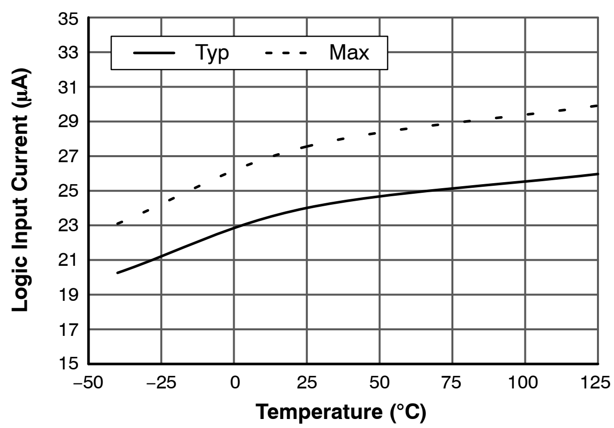


Figure 12. Logic High Input Bias Current vs. Temperature

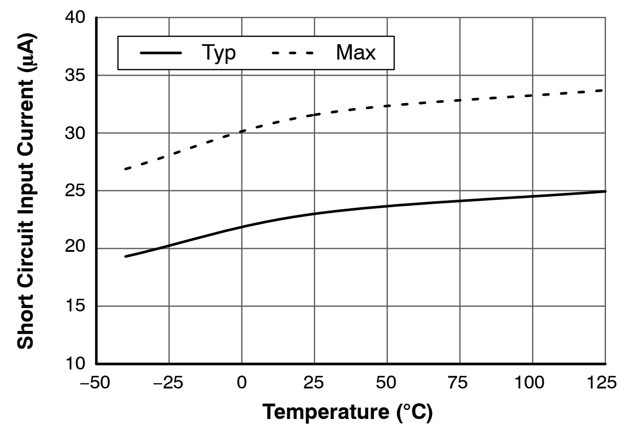


Figure 13. I_{CSCIN} vs. Temperature

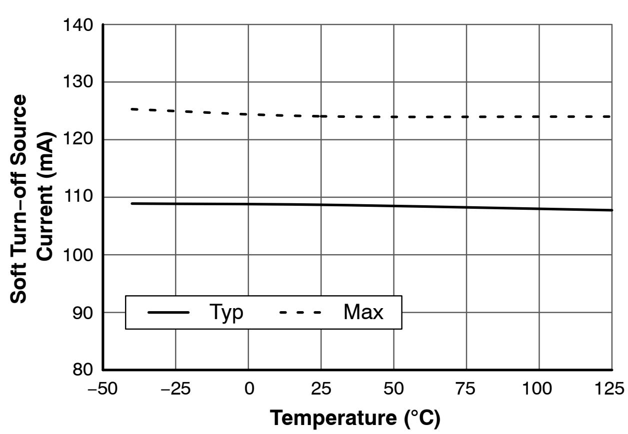


Figure 14. I_{SOFT} vs. Temperature

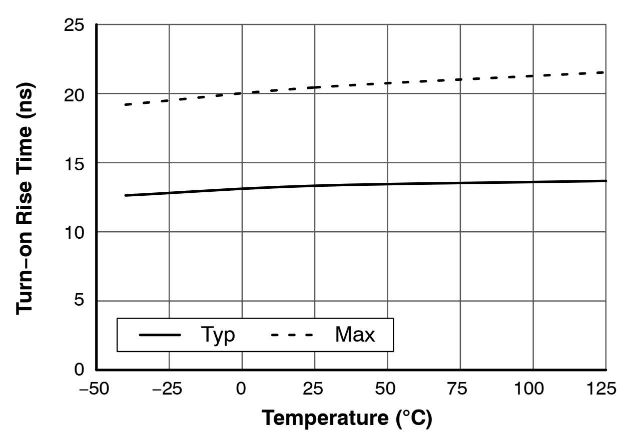


Figure 15. Turn−on Rising Time vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

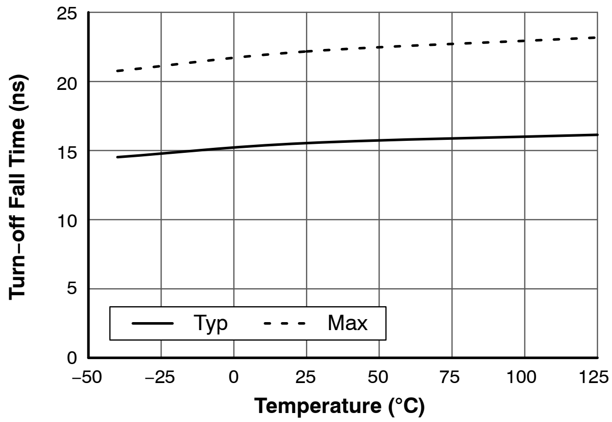


Figure 16. Turn−off Falling Time vs. Temperature

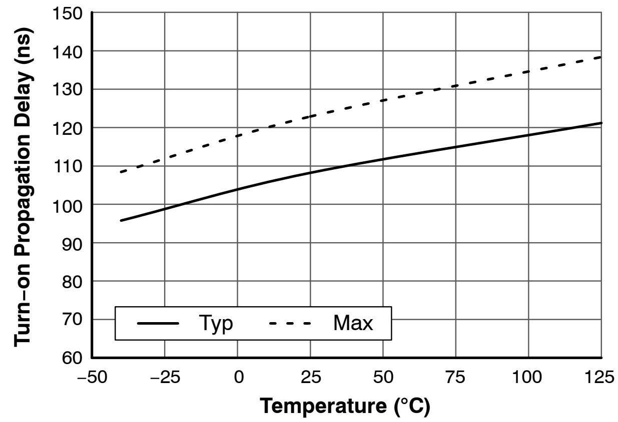


Figure 17. Turn−on Delay Time vs. Temperature

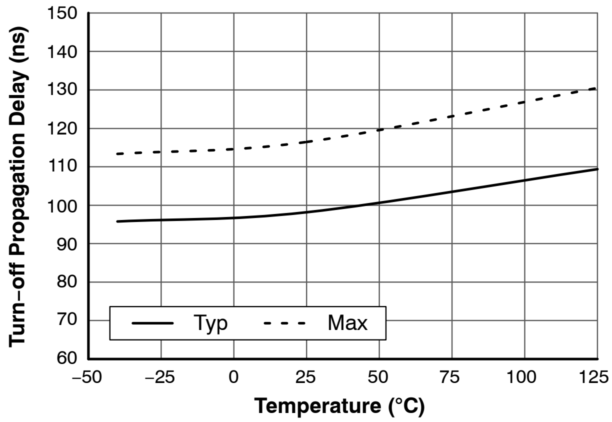


Figure 18. Turn−off Delay time vs. Temperature

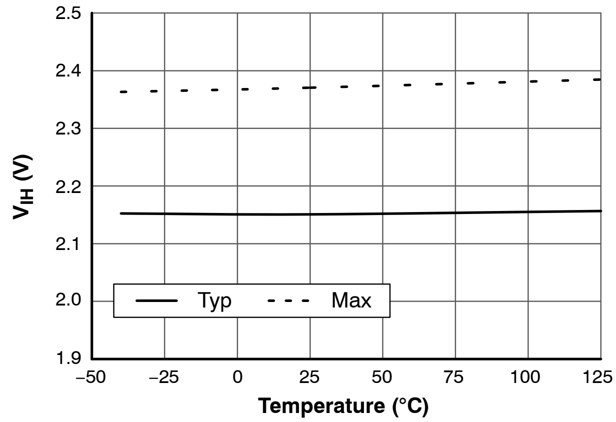


Figure 19. Logic High Input Voltage Threshold vs. Temperature

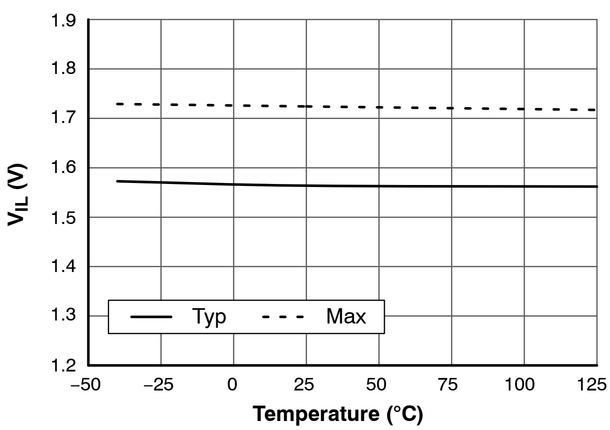


Figure 20. Logic Low Input Voltage Threshold vs. Temperature

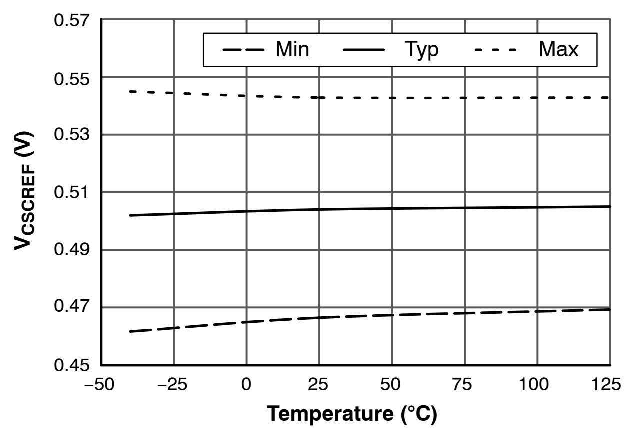


Figure 21. V_{CSCREF} vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

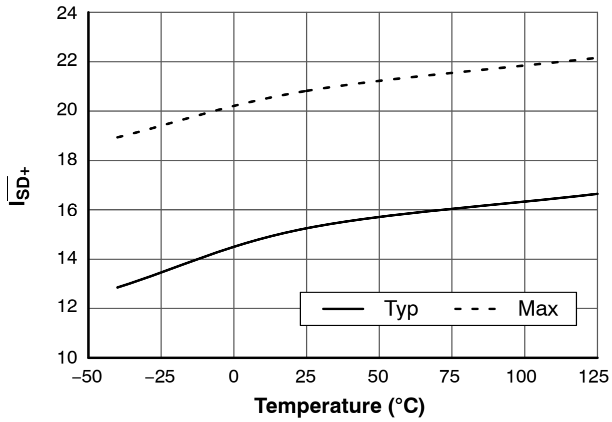


Figure 22. $\overline{SD}$ Logic High Input Bias Current vs. Temperature

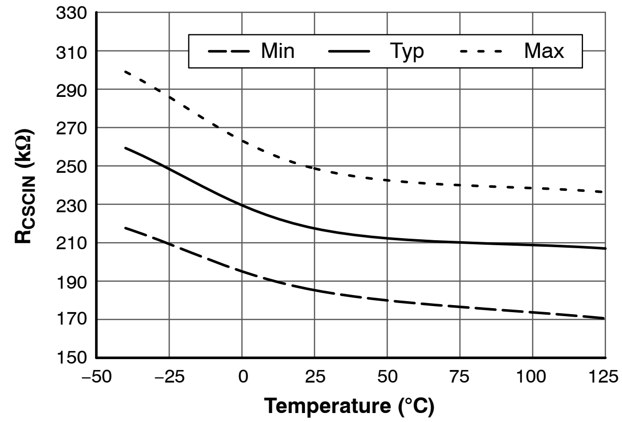


Figure 23. Input Pull Down Short Circuit Resistance vs. Temperature

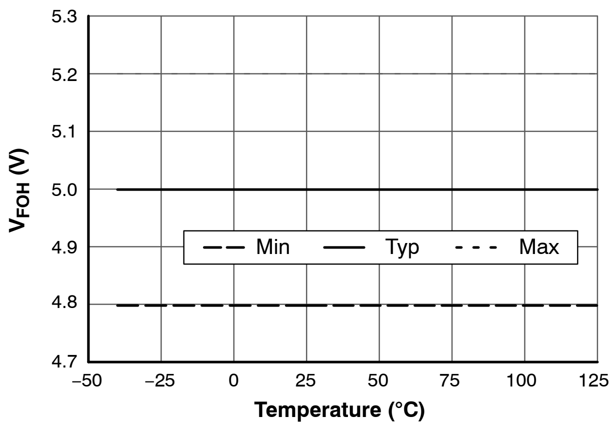


Figure 24. Fault Output High Level Voltage vs. Temperature

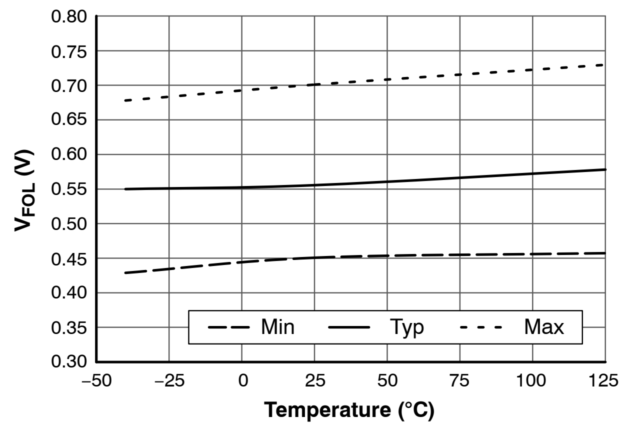


Figure 25. Fault Output Low Level Voltage vs. Temperature

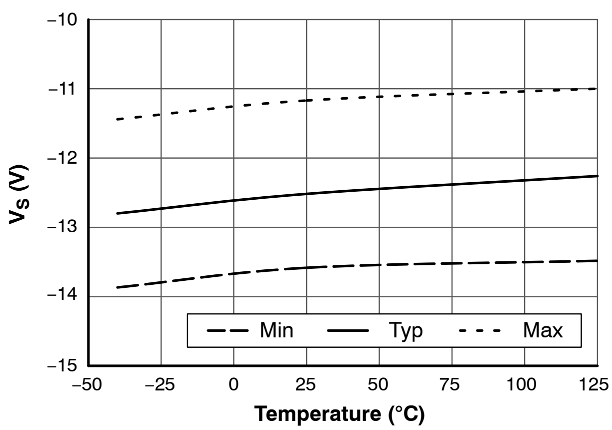


Figure 26. Allowable Negative V_S Voltage vs. Temperature

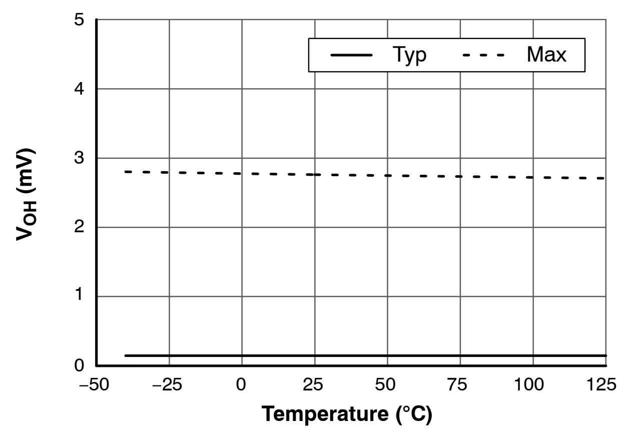


Figure 27. High−level Output Voltage vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

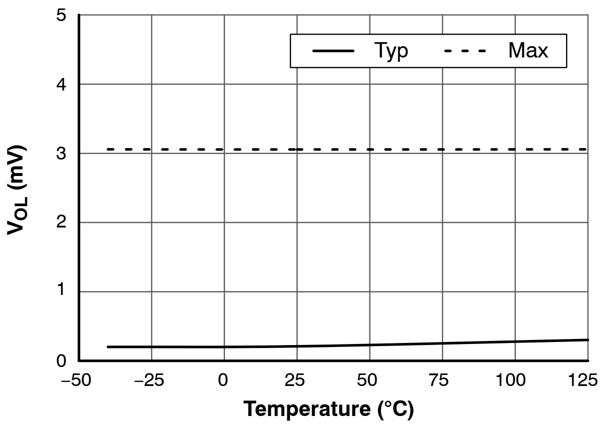


Figure 28. Low−level Output Voltage vs. Temperature

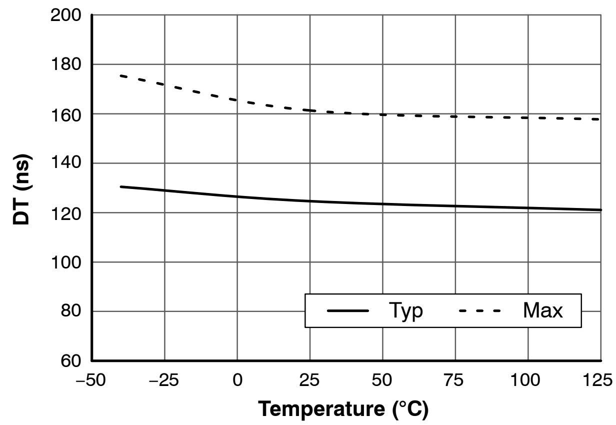


Figure 29. Dead Time vs. Temperature

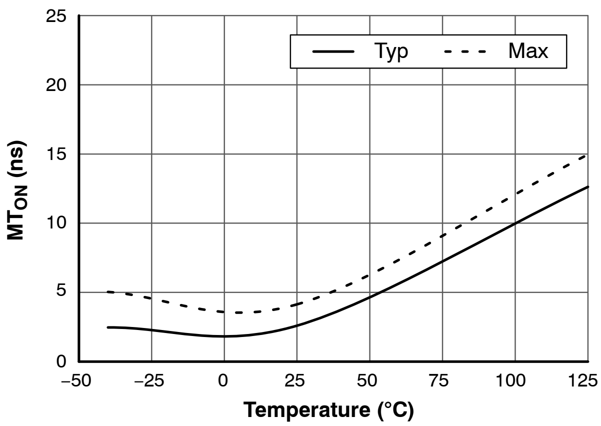


Figure 30. Delay Matching HO and LO Turn−on vs. Temperature

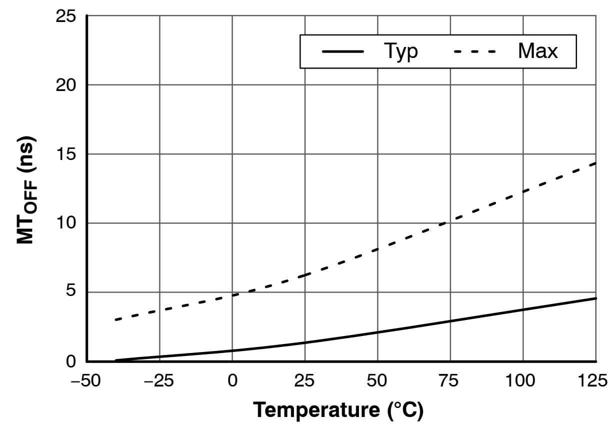


Figure 31. Delay Matching HO and LO Turn−off vs. Temperature

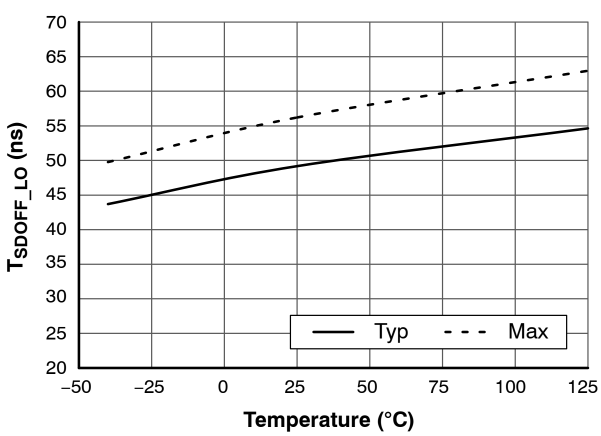


Figure 32. $\overline{SD}$ to Low−side Propagation Delay vs. Temperature

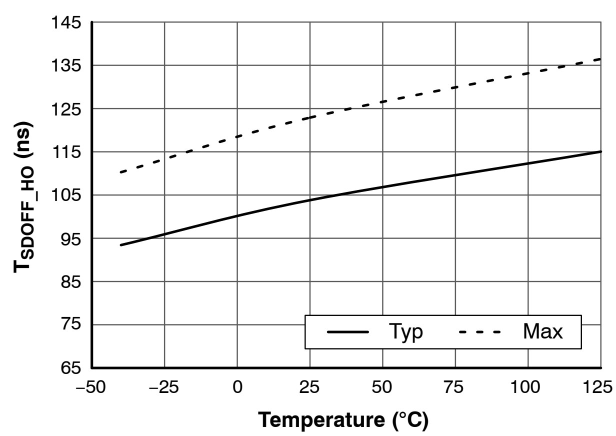


Figure 33. $\overline{SD}$ to High−side Propagation Delay vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

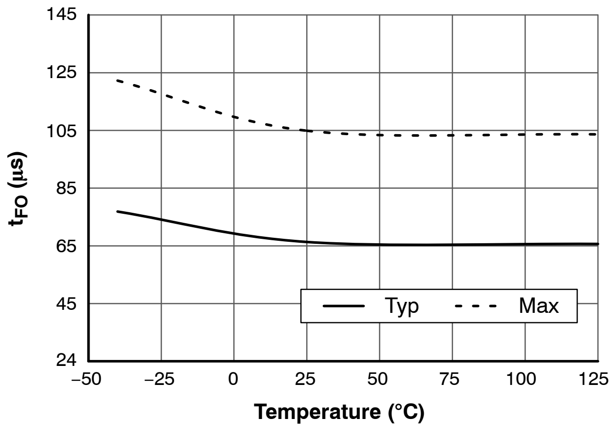


Figure 34. Fault Output Minimum Pulse Width vs. Temperature

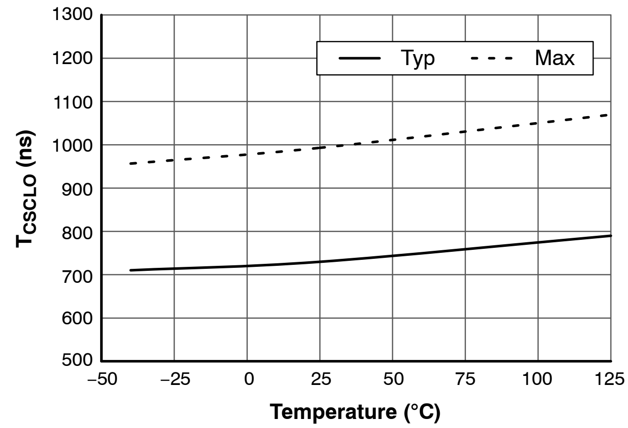


Figure 35. Time from CSC Triggering to Low−side Gate Output vs. Temperature

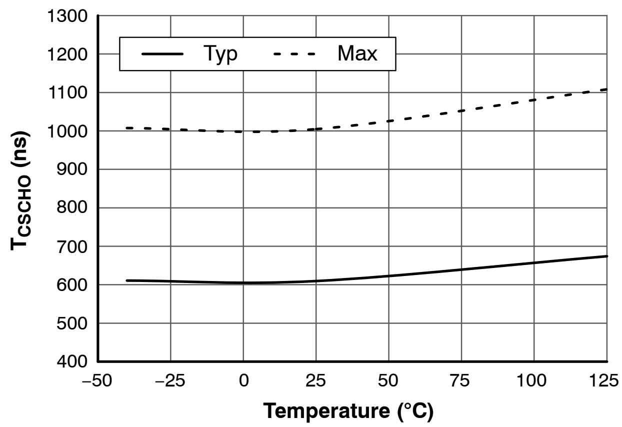


Figure 36. Time from CSC Triggering to High−side Gate Output vs. Temperature

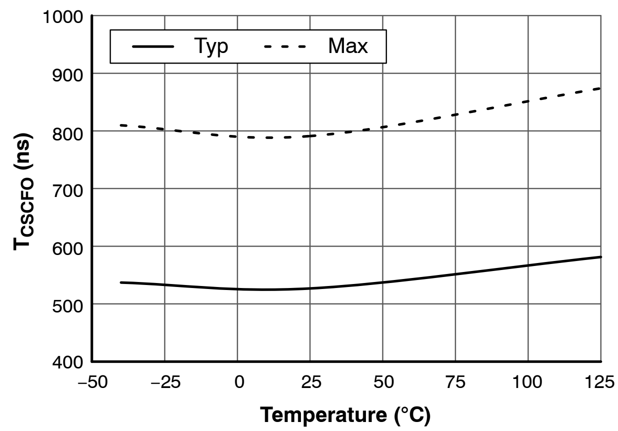


Figure 37. Time from CSC Triggering to FO vs. Temperature

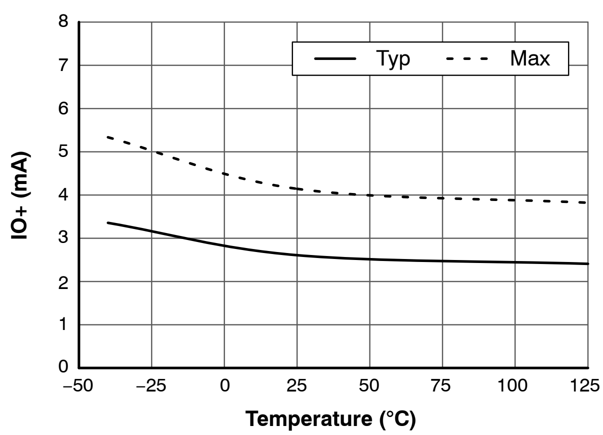


Figure 38. Output High Short−circuit Pulsed Current vs. Temperature

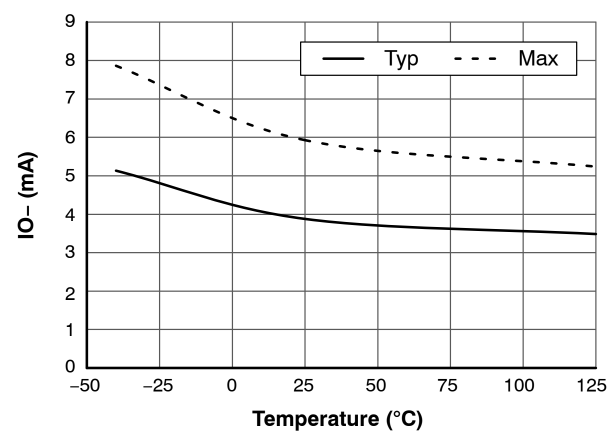


Figure 39. Output Low Short−circuit Pulsed Current vs. Temperature

SWITCHING TIME DEFINITIONS

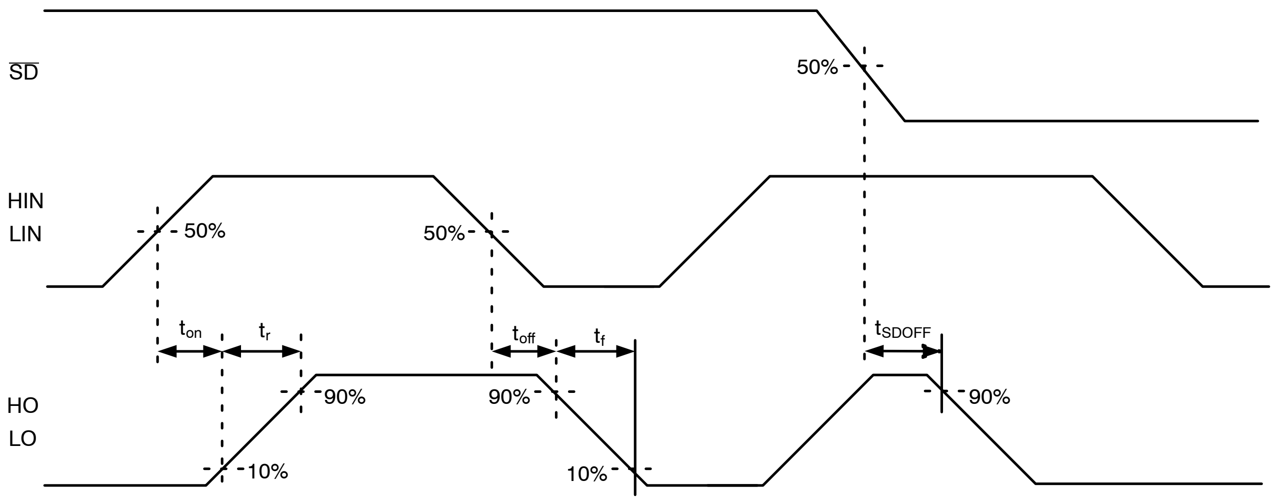


Figure 40. Switching Timing Waveforms Definition (Propagation Delay, Rise and Fall Time)

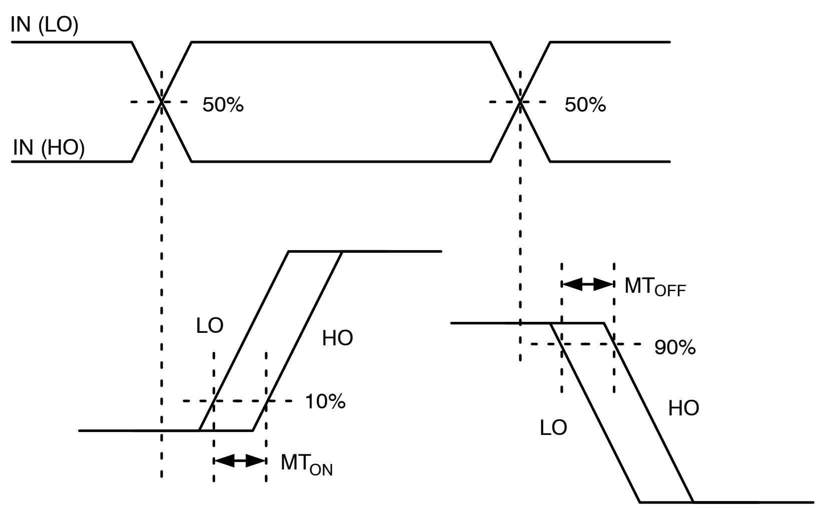


Figure 41. Switching Timing Waveforms Definition (Matching Delay)

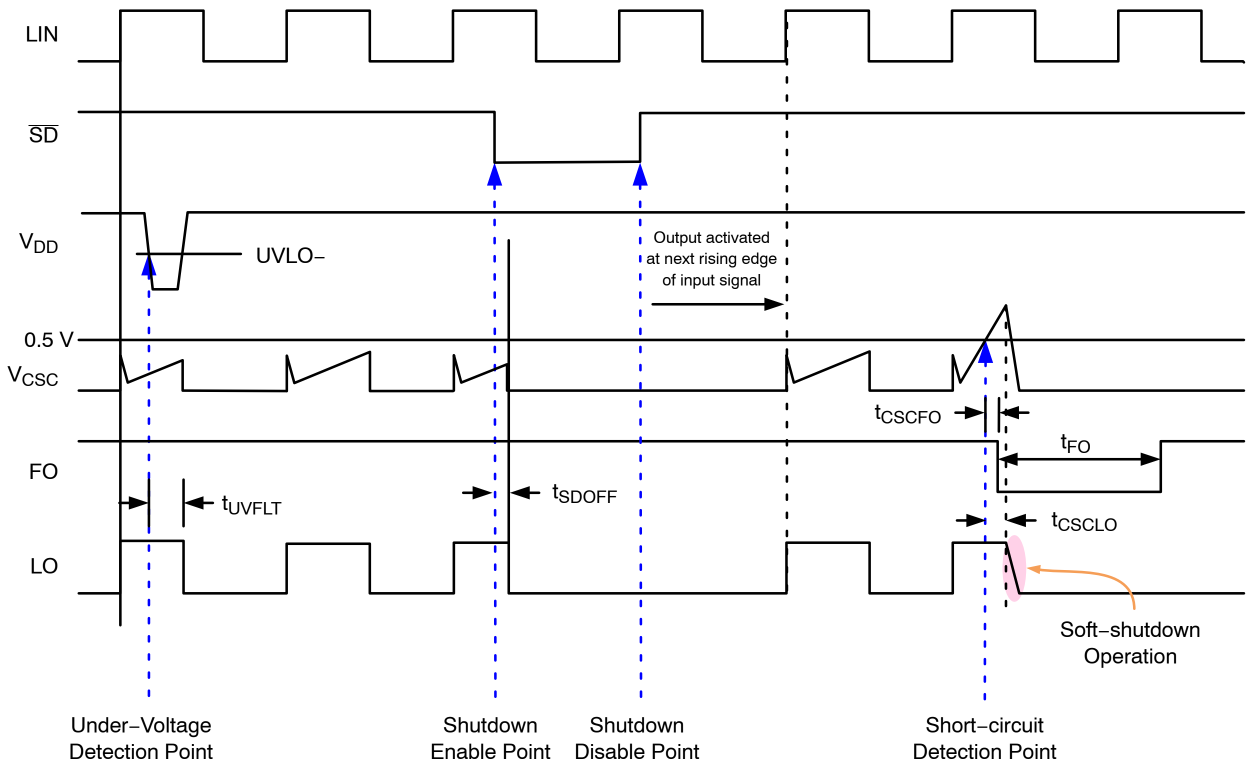


Figure 42. Switching Timing Waveforms Definition – Low Side

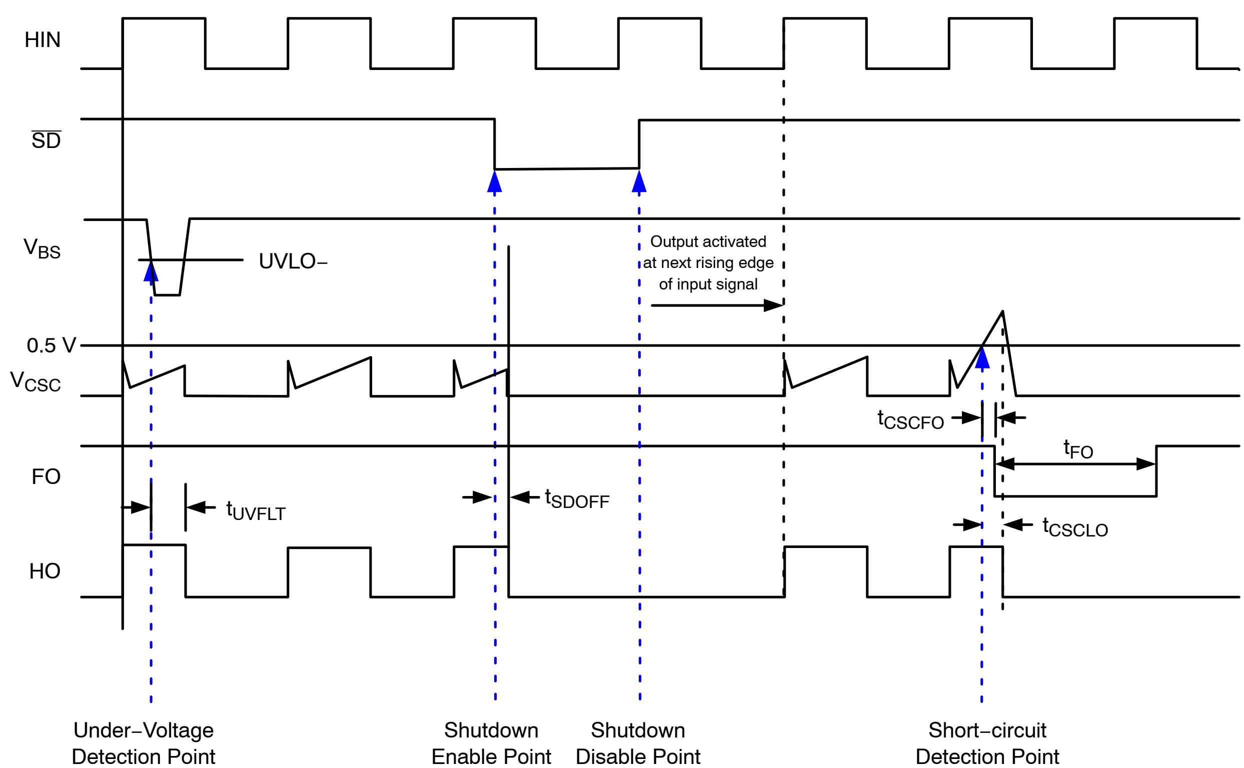


Figure 43. Switching Timing Waveforms Definition – High Side

APPLICATIONS INFORMATION

Protection Function

Shutdown ($\overline{SD}$) Function

The shutdown ($\overline{SD}$) pin of FAD8253 is active low, meaning that the driver outputs are enabled when $\overline{SD}$ pin is pulled up and vice versa. If $\overline{SD}$ pin is pulled low for a time equivalent to propagation delay, the outputs of both high and low side driver stages are turned off. The outputs are reactivated on the next rising edge of the input signal, once the $\overline{SD}$ pin is pulled up.

Under−Voltage Lockout (UVLO)

The FAD8253 has an internal under−voltage lockout (UVLO) protection circuitry for both high−side and low−side driver stages, with a threshold optimized for IGBTs. The UVLO independently monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (V_{BS}) to prevent malfunction if V_{DD} and V_{BS} drop lower than the specified threshold voltage in the manner explained below:

- If V_{BS} drops below its negative−going threshold voltage, the output of the high side driver stage is pulled down (or turned off).
- If V_{DD} voltage drops below its negative−going threshold voltage, the outputs of both the low side and high side driver stages are pulled down (or turned off).

In either of the above cases, the outputs will resume their normal operation once the V_{BS}/V_{DD} voltages have risen back to the necessary positive going threshold, as shown in Figure 44. Moreover, the UVLO hysteresis and the UV filtering time prevent chattering during power supply transitions. If the supply voltage (V_{DD} or V_{BS}) maintains an under−voltage condition for a duration longer than the under−voltage filtering time, the high and low side driver outputs are turned off. Note that an UVLO event has no impact to the Fault Output flag.

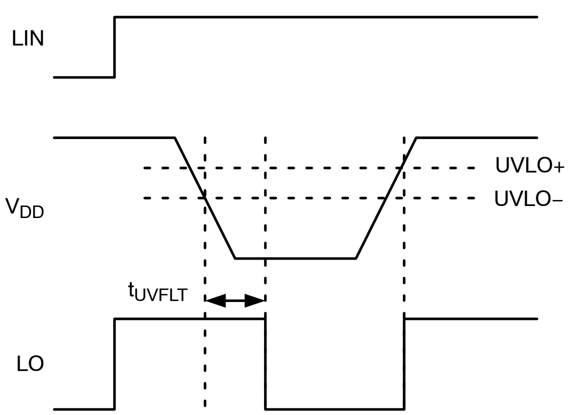


Figure 44. Waveforms for Under−Voltage Lockout

Shoot−Through Prevention Function

The FAD8253 has a shoot−through prevention circuitry that monitors both the high−side and low−side inputs. It is designed to prevent the outputs of the high−side and low−side stages from turning on at the same time.

As shown in Figure 45, if the low−side input (LIN) signal is provided to the driver while the high−side input (HIN) signal is already present, the high side output (HO) is turned off immediately while the low−side output (LO) is kept turned off. In addition, both driver outputs are kept turned off for as long as both HIN and LIN are present. This prevents the shoot−through of the high−side and low−side devices in an application. Similarly, as shown in Figure 46, if HIN signal is provided to the driver while LIN signal is already present, LO is turned off immediately while HO is kept turned off.

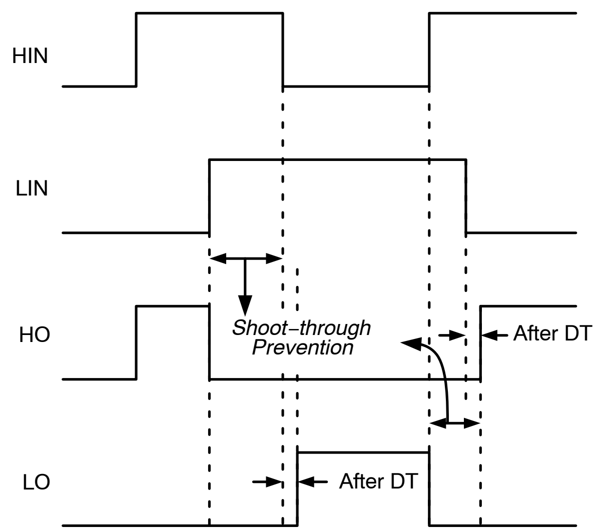


Figure 45. Example Waveforms for Shoot−through Prevention

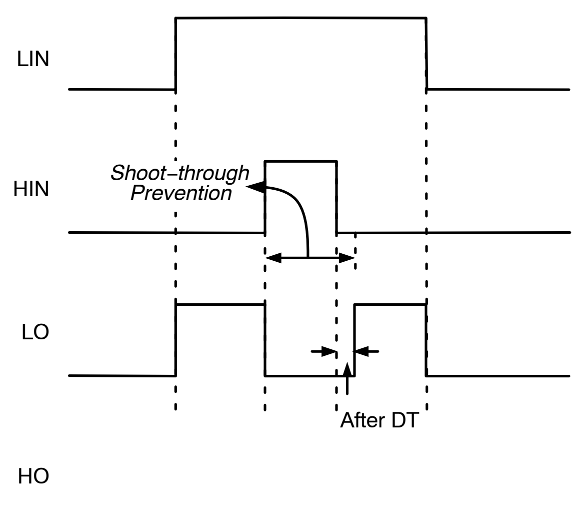


Figure 46. Example waveforms for Shoot−through Prevention

Please note that the driver resumes normal operation with a built−in dead time of 120 ns (typ.) between HO and LO, only when LIN and HIN signals are not provided at the same time.

Over−Current/Short−Circuit Protection Function

The FAD8253 has a low side over−current detection circuitry that monitors the voltage across the low side current sensing resistor (R_{CSR}) through the short−circuit current detection input (CSC) pin.

The input stage of the over current circuitry is depicted in Figure 47. The principle of overcurrent/short−circuit detection feature is to monitor the voltage at point A (which appears due to the phase current flowing into R_{CSR}). If the sensed voltage exceeds the short−circuit detector reference voltage V_{CSCREF} (typ. 0.5 V), this indicates an over−current condition and the driver outputs are turned off.

For example, if R_{CSC}= 1 mΩ, the driver will activate the short circuit protection for a phase current exceeding 500 A (1 mΩ × 500 A = 0.5 V ≥ V_{CSCREF}).

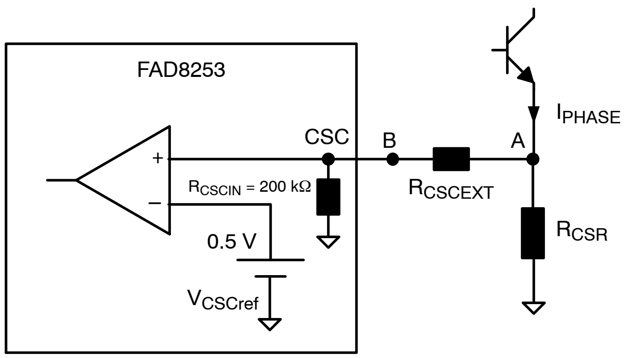


Figure 47. Input Circuit of the Overcurrent/Short−circuit Protection Block

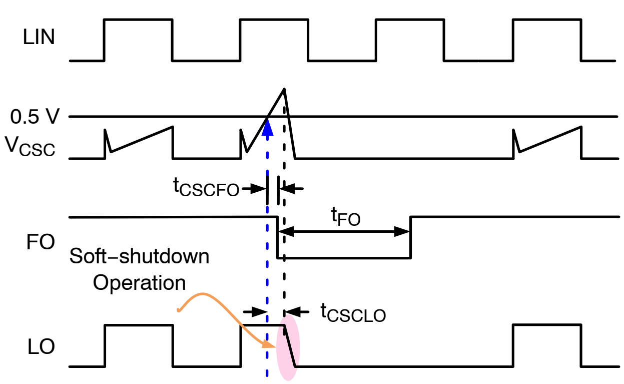


Figure 48. Waveforms for Short Circuit Protection

It is recommended to place a series resistance R_{CSCEXT} to limit the input current that may flow into the driver during transient conditions. Note that R_{CSCEXT} and R_{CSCIN} form a voltage divider that could lower the voltage at the CSC pin (at point B in Figure 47). To minimize the voltage difference, a value of 1 kΩ is recommended for R_{CSCEXT}. As a result, the voltage at point B (or CSC pin) will be R_{CSCEXT} / (R_{CSCEXT} + R_{CSCIN}) = 200 kΩ / (200 kΩ + 1 kΩ), which is only 0.5% lower than at point A.

An over−current condition must last for a minimum duration of t_{CSCFLT} (typ. 300 ns) to trigger the short− circuit protection. This duration has been defined to provide adequate noise filtering against high frequency noises during IGBT switching. If this time is not sufficient, an additional capacitor can be placed at the input of the CSC pin to further extend the filtering time.

Upon detection of a short circuit through the CSC pin:

- the high side output turns off immediately;
- the low side driver output initiates a soft shutdown to turn off the low side IGBT slowly to prevent it from entering the avalanche mode;
- the Fault Output (FO) pin generates a fault signal for a duration of t_{FO} (typ. 60 μs).

Please note that once the FO is triggered, the driver outputs can be reactivated on the next rising edge of input signal only after the duration of t_{FO} has passed.

Layout Considerations

For optimum performance, considerations must be taken during printed circuit board (PCB) layout.

Power Supply Bypass Capacitors

The implementation of bypass capacitors is essential to optimal operation of gate drivers like FAD8253 and so, special attention is required.

The local bypass capacitor between V_{DD} and V_{SS} needs to provide pulsed currents for the low side driver output. At the same time, if a high−side bootstrap circuit is employed, it has to rapidly charge the bootstrap capacitor as well.

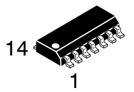
A typical criterion for choosing the value of bypass capacitor is to keep the ripple voltage on the supply pin to ≤5%. Typically, two capacitors in parallel are recommended. Often, a capacitor of smaller value is placed very close to the V_{DD} pin in parallel with another capacitor of higher value to reduce impedance. For sizing of the bootstrap capacitor please refer to application note AN−6076.

Gate−Drive Loop

Current loops behave like antennae, able to receive and transmit noise. To reduce the noise coupling/emission and improve the power switch turn−on and off performance, gate−drive loops must be reduced as much as possible.

Ground Plane

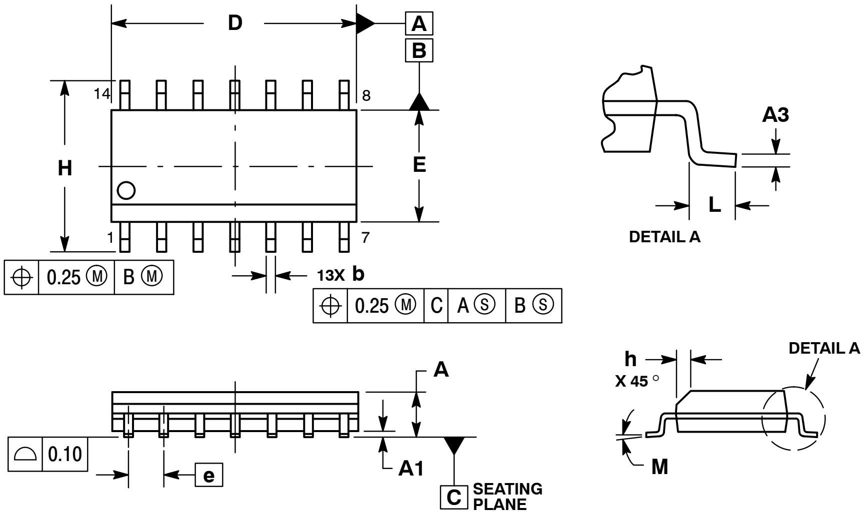
To minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.



SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

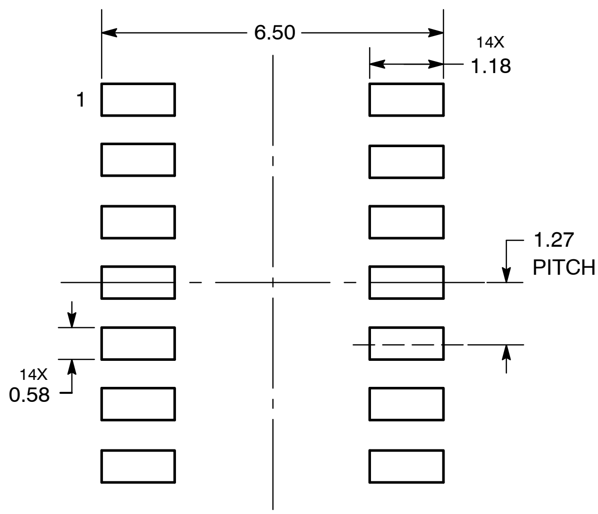
DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

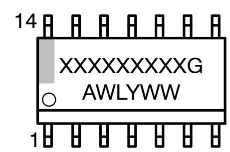
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
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11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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