Features

- **Standard-Voltage Operation**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
- **Internally Organized 4096 x 8 (32K), 8192 x 8 (64K)**
- **Automotive Temperature Range –40°C to +125°C**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **400 kHz Clock Rate**
- **Write Protect Pin for Hardware Data Protection**
- **32-byte Page Write Mode (Partial Page Writes Allowed)**
- **Self-timed Write Cycle (5 ms Max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **Lead-free/Halogen-free Devices Available**
- **8-lead JEDEC SOIC and 8-lead TSSOP Packages**

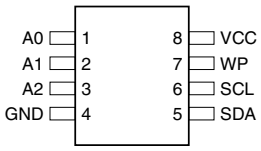
Description

The AT24C32A/64A provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common two-wire bus. The device is optimized for use in many automotive applications where low power and low voltage operation are essential. The AT24C32A/64A is available in space saving 8-lead JEDEC SOIC and 8-lead TSSOP packages and is accessed via a 2-wire serial interface and is available in a 2.7V (2.7V to 5.5V) version.

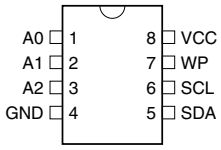
Table 1. Pin Configuration

Pin Name	Function
A0 – A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

8-lead SOIC



8-lead TSSOP



Two-wire Automotive Serial EEPROM 32K (4096 x 8) 64K (8192 x 8)

AT24C32A[1] AT24C64A

1. AT24C32A not recommended for new design; replaced by AT24C32D Automotive.
2. AT24C64A not recommended for new design; replaced by AT24C64D Automotive.

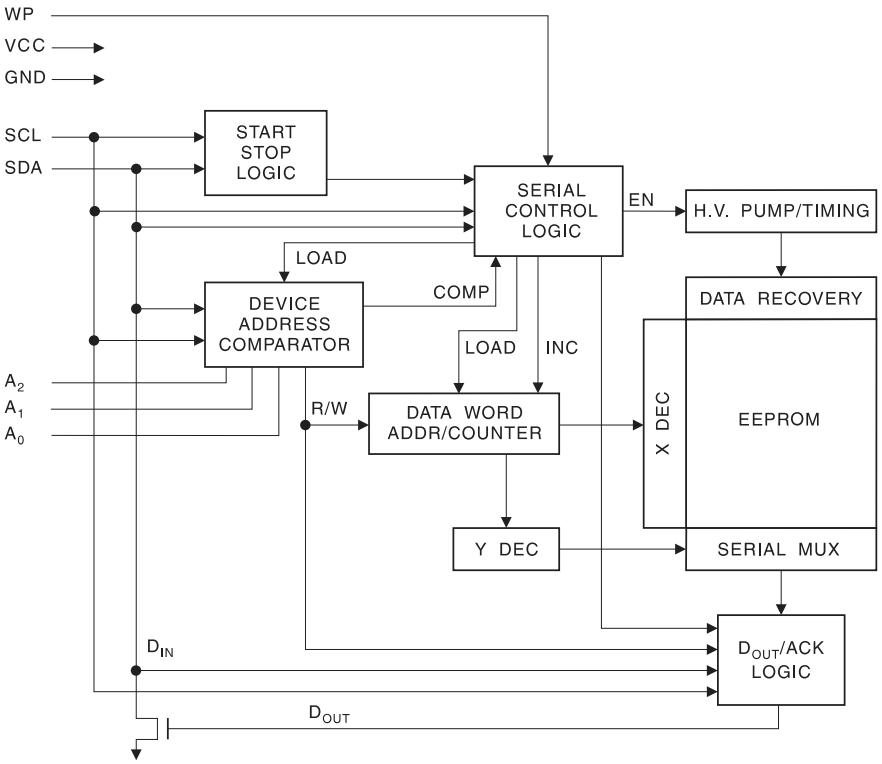
5120D–SEEPR–6/08

Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other AT24Cxx devices. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3 pF. If coupling is >3 pF, Atmel recommends connecting the address pins to GND.

WRITE PROTECT (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected high to V_{CC}, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3 pF. If coupling is >3 pF, Atmel recommends connecting the pin to GND. Switching WP to V_{CC} prior to a write operation creates a software write protect function.

Memory Organization

AT24C32A/64A, 32K/64K SERIAL EEPROM: The 32K/64K is internally organized as 128/256 pages of 32 bytes each. Random word addressing requires a 12/13-bit data word address.

Table 2. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +2.7V to +5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 3. DC Characteristics

Applicable over recommended operating range from: T_A = –40°C to +125°C, V_{CC} = +2.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC3}	Supply Voltage			2.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	READ at 400 kHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	WRITE at 400 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.0	3.0	µA
		V_{CC} = 5.0V			3.0	5.0	
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}[1]	Input Low Level			–0.6		V_{CC} x 0.3	V
V_{IH}[1]	Input High Level			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 4. AC Characteristics

Applicable over recommended operating range from T_A = –40°C to +125°C, V_{CC} = +2.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	AT24C32A/AT24C64A 2.7V – 5.5V Min	AT24C32A/AT24C64A 2.7V – 5.5V Max	Units
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.6		µs
t_I	Noise Suppression Time(1)		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.2		µs
$t_{HD.STA}$	Start Hold Time	0.6		µs
$t_{SU.STA}$	Start Set-up Time	0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		ns
t_R(1)	Inputs Rise Time		0.3	µs
t_F(1)	Inputs Fall Time		300	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		5	ms
Endurance(1)	5.0V, 25·C, Page Mode	1M		Write Cycles

Notes: 1. This parameter is ensured by characterization only.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 5 on page 8).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 5 on page 8).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The AT24C32A/64A features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the stop bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Figure 2. Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

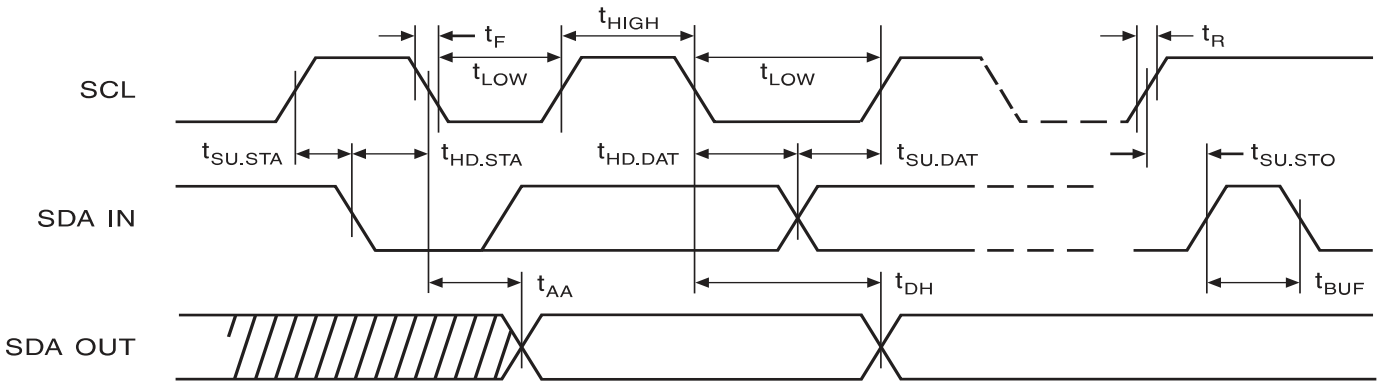
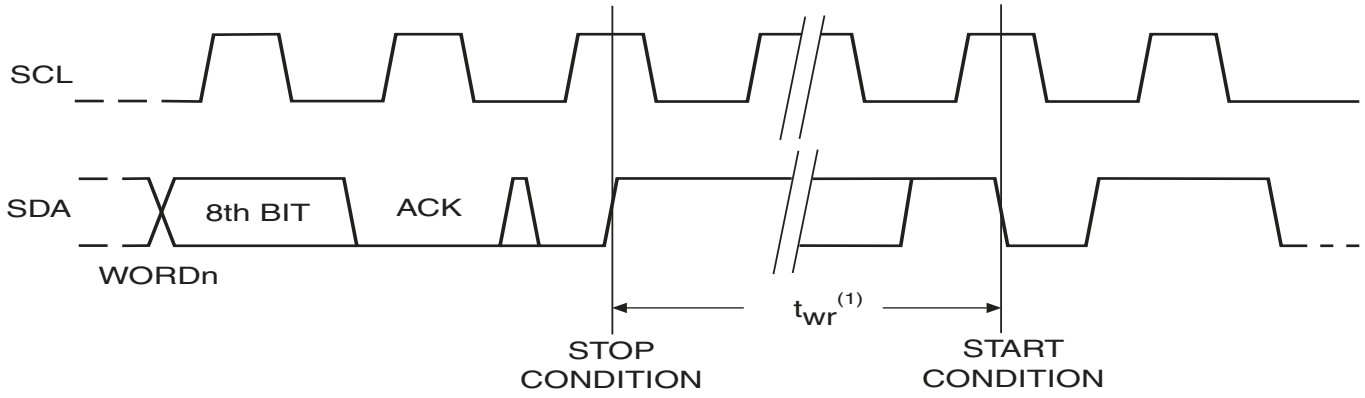


Figure 3. Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4. Data Validity

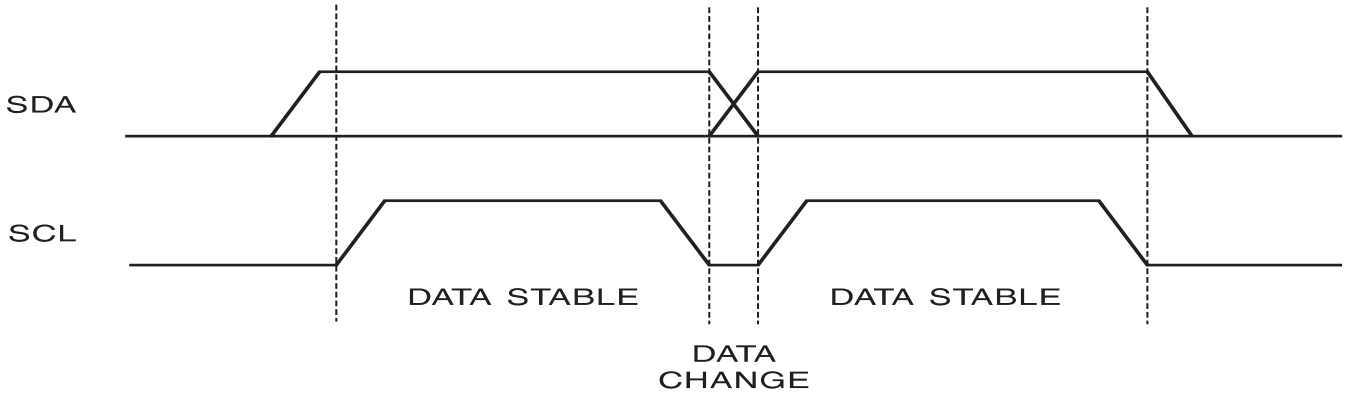


Figure 5. Start and Stop Definition

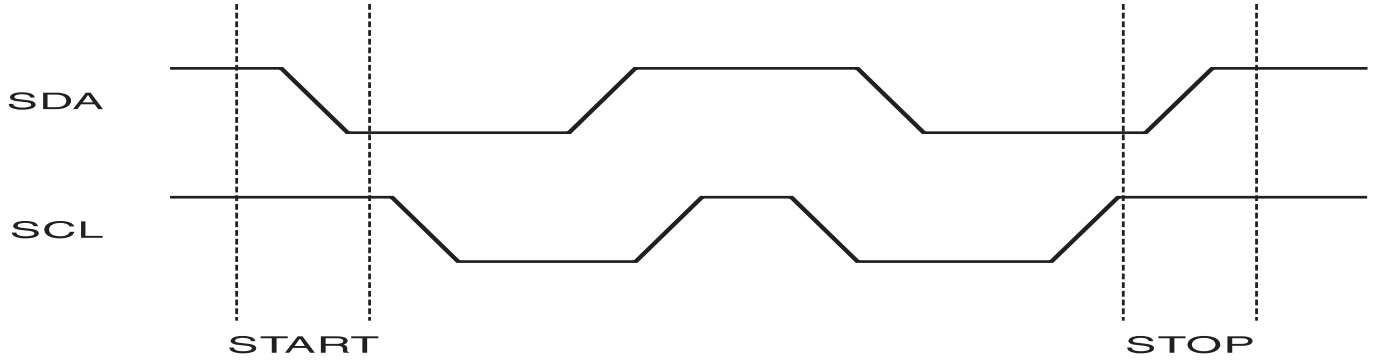
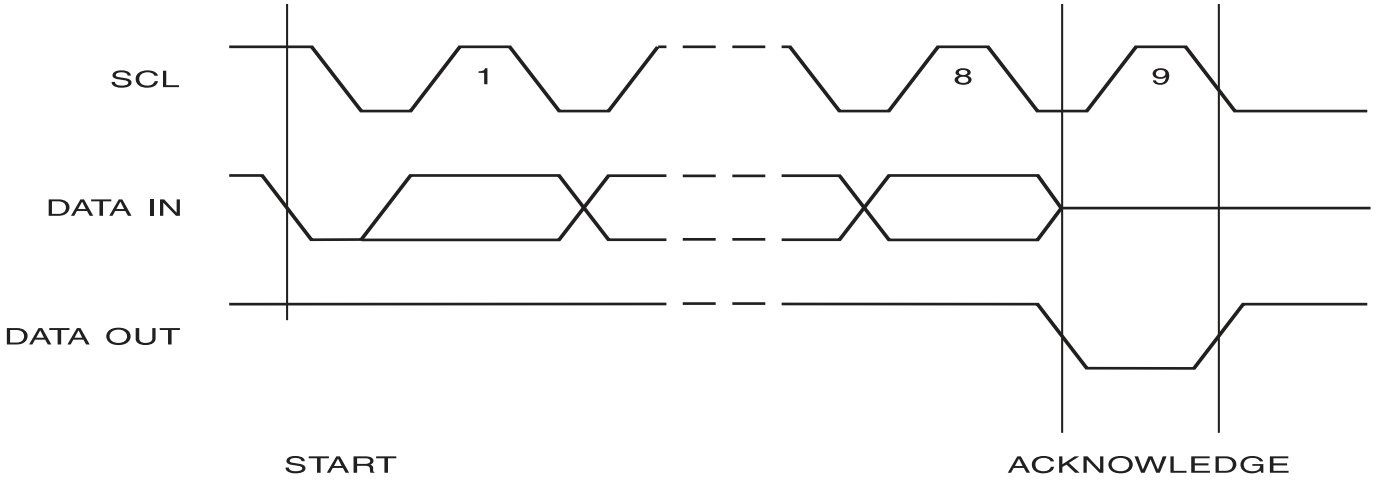


Figure 6. Output Acknowledge



Device Addressing

The 32K/64K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 7 on page 11). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 32K/64K uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device.

DATA SECURITY: The AT24C32A/64A has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8 on page 11).

PAGE WRITE: The 32K/64K EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 9 on page 11).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page, to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 10 on page 11).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 11 on page 12).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 12 on page 12).

Figure 7. Device Address

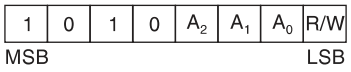


Figure 8. Byte Write

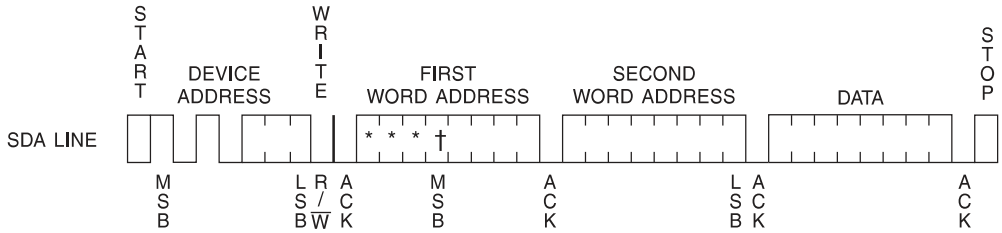
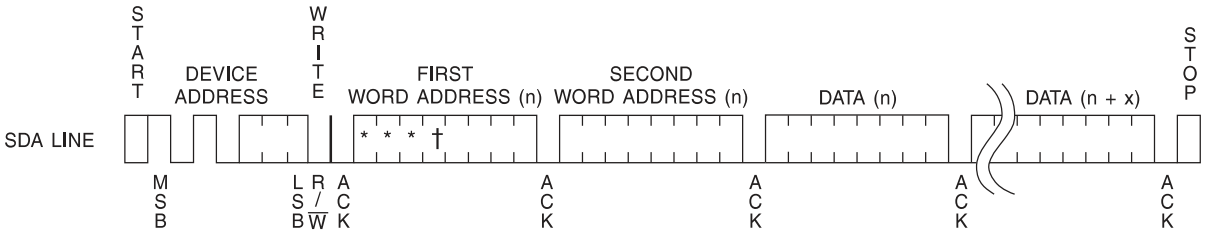


Figure 9. Page Write



Notes: 1. * = *DON'T CARE* bits
2. † = *DON'T CARE* bits for the 32K

Figure 10. Current Address Read

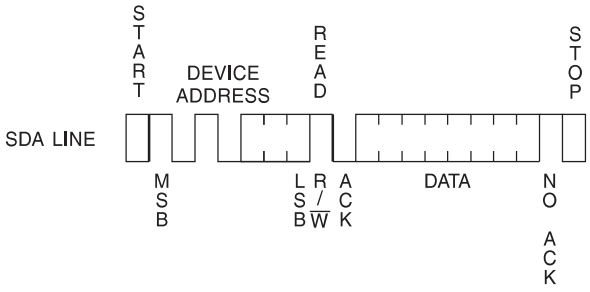
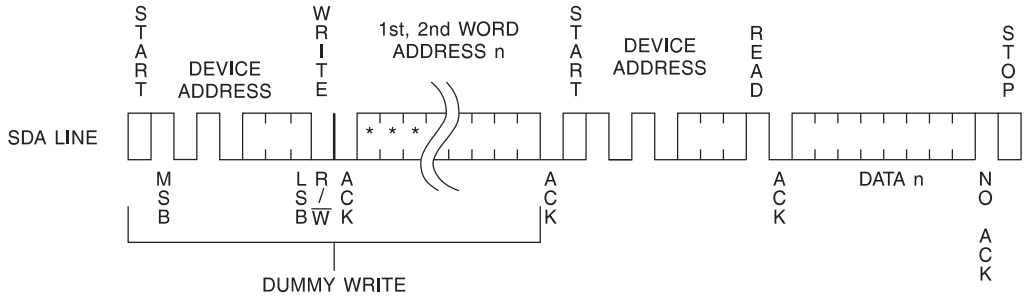
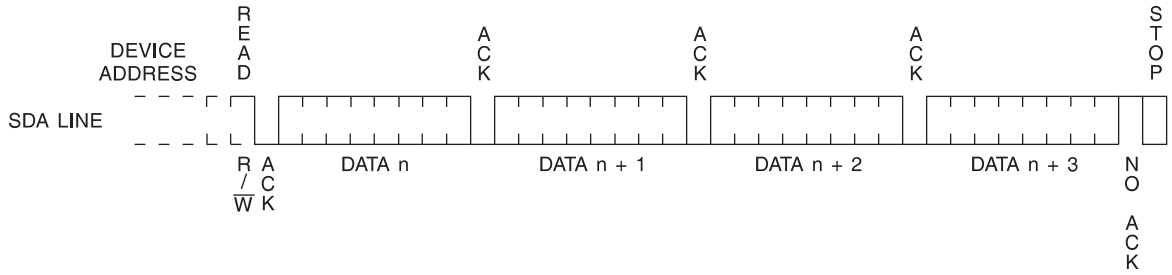


Figure 11. Random Read



Note: 1. * = *DON'T CARE* bits

Figure 12. Sequential Read



AT24C32A Ordering Information[1]

Ordering Code	Package	Operation Range
AT24C32AN-10SQ-2.7[2][3] AT24C32A-10TQ-2.7[2][3]	8S1 8A2	Lead-free/Halogen-free/ Automotive (–40·C to 125·C)

Notes:
1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in the AC and DC Characteristics tables.
2. “Q” designates Green package and RoHS Compliant.
3. AT24C32A not recommended for new design; replaced by AT24C32D Automotive.

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
Options	
–2.7	Low Voltage (2.7V to 5.5V)

AT24C64A Ordering Information[1]

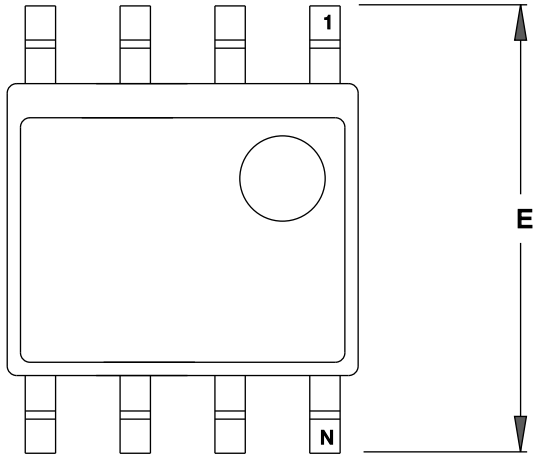
Ordering Code	Package	Operation Range
AT24C64AN-10SQ-2.7[2] AT24C64A-10TQ-2.7[2]	8S1 8A2	Lead-free/Halogen-free/ Automotive (–40·C to 125·C)

Notes: 1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in the AC and DC Characteristics tables.
2. "Q" designates Green package and RoHS Compliant.

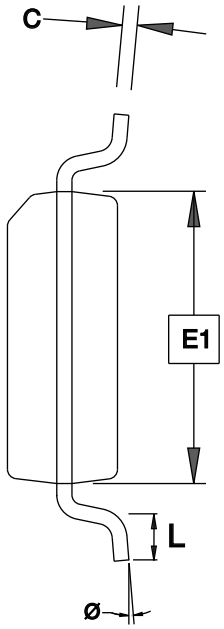
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
Options	
–2.7	Low Voltage (2.7V to 5.5V)

Package Drawings

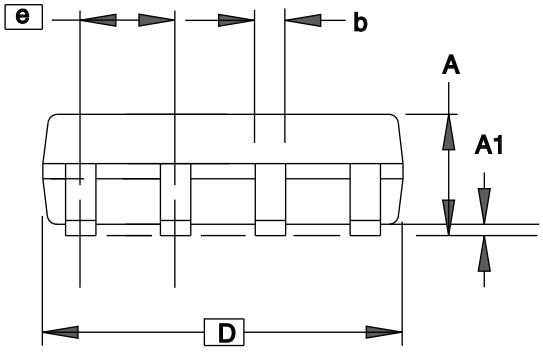
8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

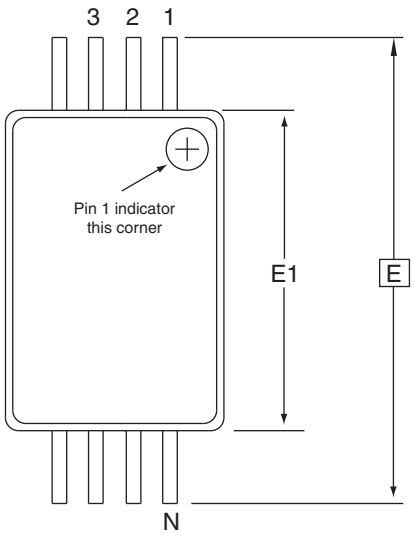
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
θ	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

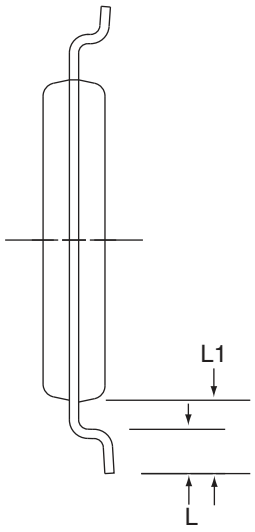
3/17/05

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	8S1	C

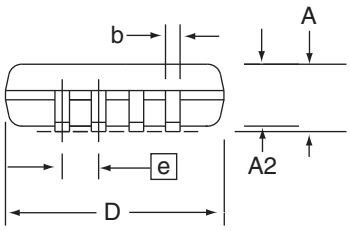
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B

Revision History

Revision History

Revision	Date	Comments
5120D	8/2013	AT24C64A not recommended for new design; replaced by AT24C64D Automotive.
5120D	8/2012	AT24C32A not recommended for new design; replaced by AT24C32D Automotive.
5120D	6/2008	Implemented revision history.

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