HARRIS

2N6792

August 1991

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

Features

- 2A, 400V
- $r_{DS(on)} = 1.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

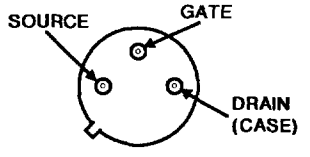
Description

The 2N6792 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6792 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

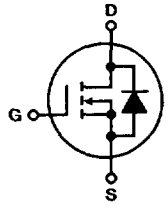
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6792	UNITS
Drain-Source Voltage	V_{DS}	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400*	V
Continuous Drain Current			
T_C = +25°C	I_D	2*	A
T_C = +100°C	I_D	1.25*	A
Pulsed Drain Current	I_{DM}	10*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	2*	A
Pulse Source Current	I_{SM}	10*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	20*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.16*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	10	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **1901.1**

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	400*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 400V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 320V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage [a]	–	–	3.6*	V	V_{GS} = 10V, I_D = 2.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance [a]	–	1.50	1.80*	Ω	V_{GS} = 10V, I_D = 1.25A, T_A = 25°C
		–	–	4.00*	Ω	V_{GS} = 10V, I_D = 1.25A, T_A = 125°C
V_{SD}	Diode Forward Voltage [a]	0.6*	–	1.4*	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance [a]	1.0*	2.0	3.0*	S(℧)	V_{DS} = 5V, I_D = 1.25A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	40*	100	200*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	20	40*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 175V, I_D = 1.25A, Z_o = 50Ω
t_r	Rise Time	–	–	35*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	60*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	35*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 200V, I_D = 100 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 10V, I_D = 2.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	450	ns	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.1	μC	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

a Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

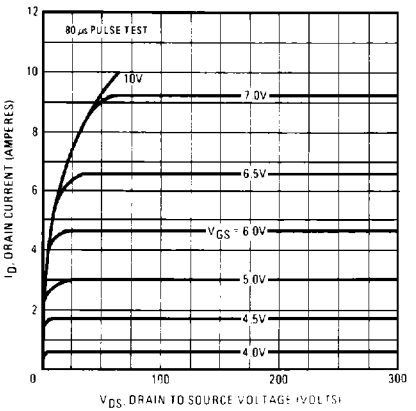


Fig. 1 - Typical output characteristics.

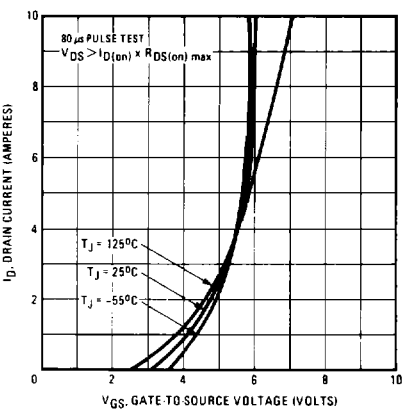


Fig. 2 - Typical transfer characteristics.

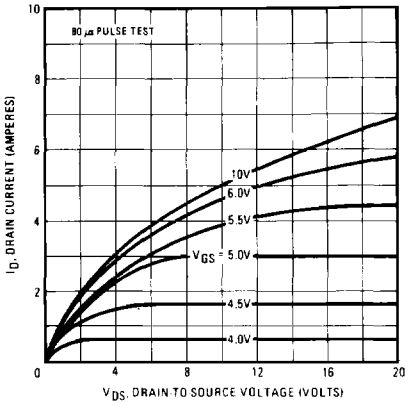


Fig. 3 - Typical saturation characteristics.

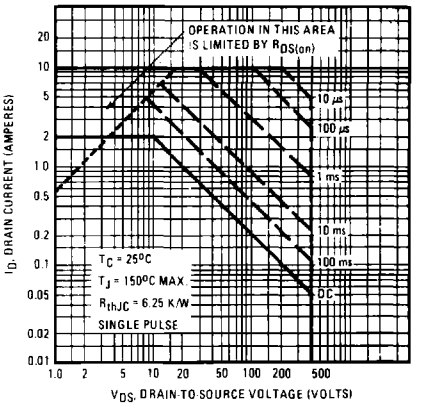


Fig. 4 - Maximum safe operating area.

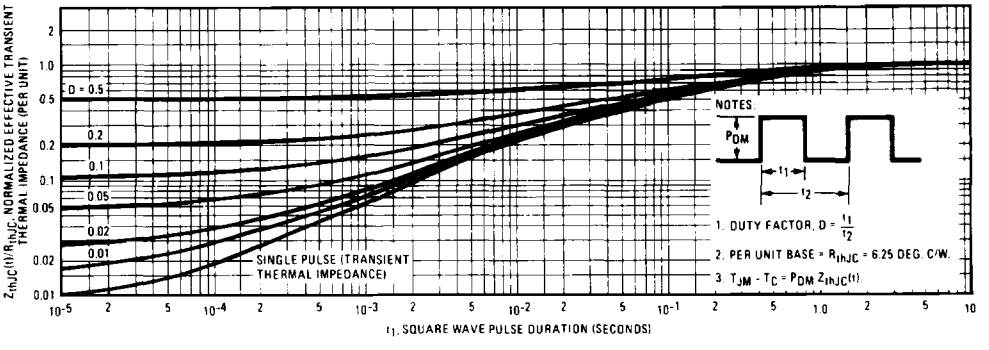


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

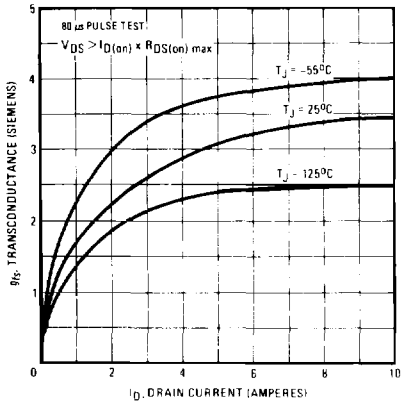


Fig. 6 - Typical transconductance versus drain current.

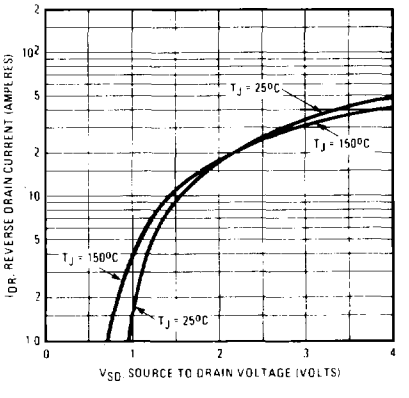


Fig. 7 - Typical source-drain diode forward voltage.

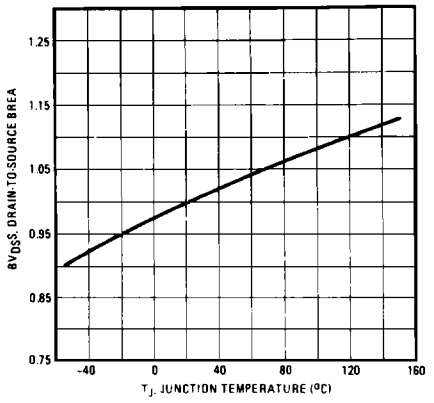


Fig. 8 - Breakdown voltage versus temperature.

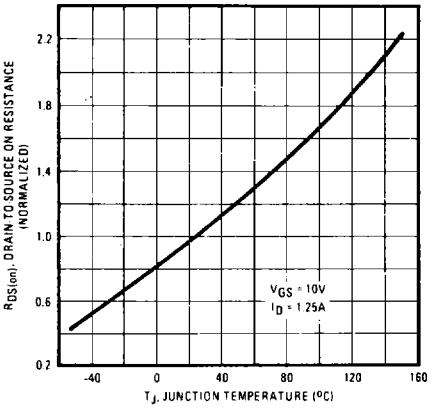


Fig. 9 - Typical normalized on-resistance versus. temperature.

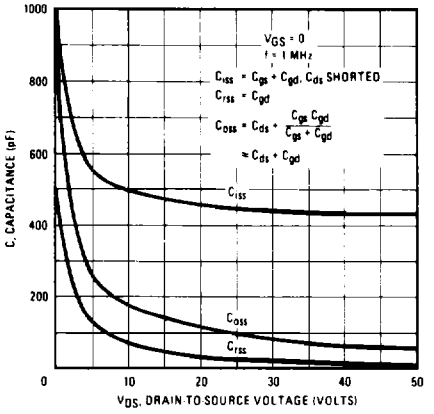


Fig. 10 - Typical capacitance versus drain-to-source. voltage.

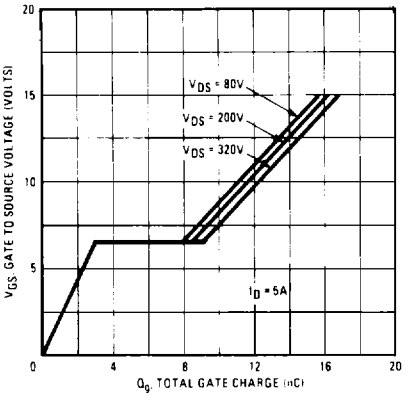


Fig. 11 - Typical gate charge versus gate-to-source. voltage.

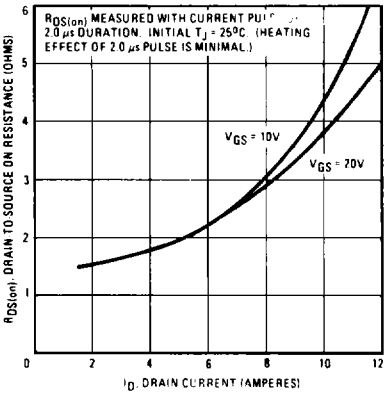


Fig. 12 - Typical on-resistance versus drain current.

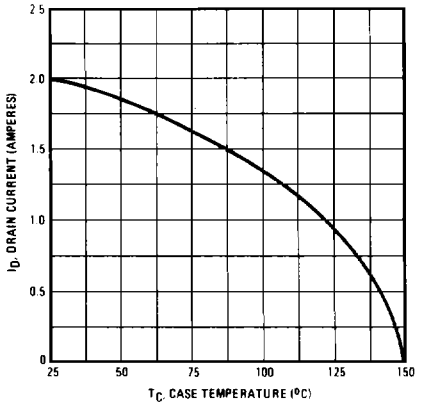


Fig. 13 - Maximum drain current versus case. temperature.

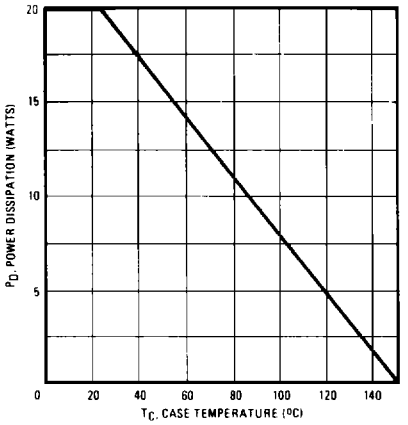
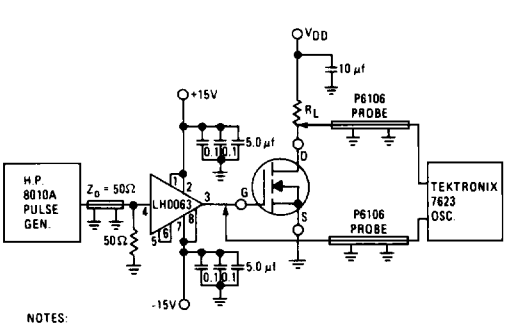
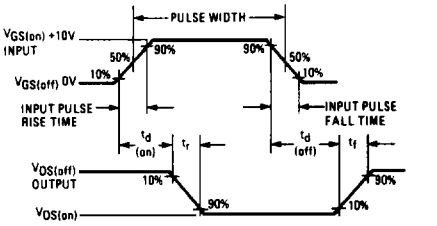


Fig. 14 - Power versus temperature derating curve.

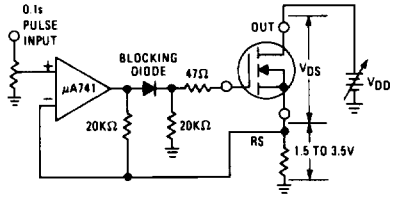


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D = R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating area test circuit.