

10A, 30V, 0.0135 Ohm, Single N-Channel, Logic Level Power MOSFET

This power MOSFET is manufactured using an innovative process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Ordering Information

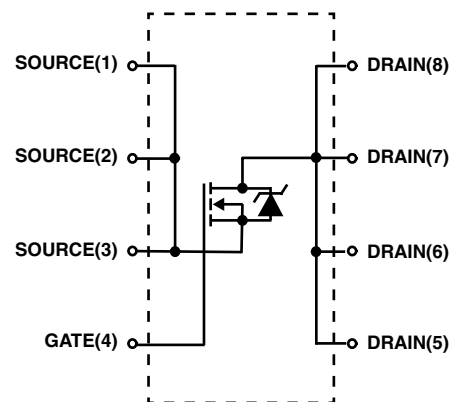
PART NUMBER	PACKAGE	BRAND
HP4410DY	SO-8	P4410DY

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HP4410DYT.

Features

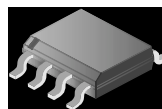
- Logic Level Gate Drive
- 10A, 30V
- $r_{DS(ON)} = 0.0135\Omega$ at $I_D = 10A, V_{GS} = 10V$
- $r_{DS(ON)} = 0.020\Omega$ at $I_D = 8A, V_{GS} = 4.5V$
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

SO-8



HP4410DY

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

	HP4410DY	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30 V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	30 V
Gate to Source Voltage	V_{GS}	± 16 V
Drain Current		
Continuous	I_D	10 A
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	50 A
Power Dissipation	P_D	2.5 W
Derate Above 25°C		0.02 W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_A = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 9)	1	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}, T_A = 55^\circ\text{C}$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 16\text{V}$	-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 8\text{A}, V_{GS} = 4.5\text{V}$ (Figures 6, 8)	-	0.015	0.020	Ω
		$I_D = 10\text{A}, V_{GS} = 10\text{V}$ (Figures 6, 8)	-	0.011	0.0135	Ω
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 25\text{V}, I_D \cong 1\text{A},$ $R_L = 25\Omega, V_{GEN} = 10\text{V},$ $R_{GS} = 6\Omega$	-	15	30	ns
Rise Time	t_r		-	9	20	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	100	ns
Fall Time	t_f		-	20	80	ns
Total Gate Charge	$Q_{g(TOT)}$		$V_{DS} = 15\text{V}, V_{GS} = 10\text{V}, I_D \cong 10\text{A}$	-	35	60
Gate to Source Charge	Q_{gs}		-	7.5	-	nC
Gate to Drain Charge	Q_{gd}		-	5.8	-	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ (Figure 4)	-	1600	-	pF
Output Capacitance	C_{OSS}		-	685	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	115	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pulse Width < 10s (Figure 11) Device Mounted on FR-4 Material	-	-	50	$^\circ\text{C}/\text{W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 2.3\text{A}$ (Figure 7)	-	0.75	1.1	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 2.3\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	50	80	ns

Typical Performance Curves Unless Otherwise Specified

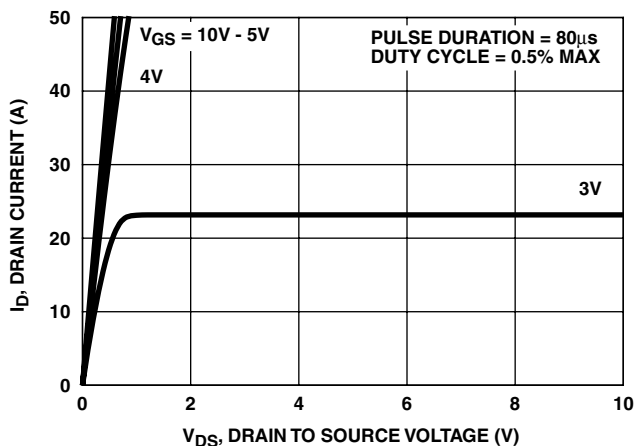


FIGURE 1. OUTPUT CHARACTERISTICS

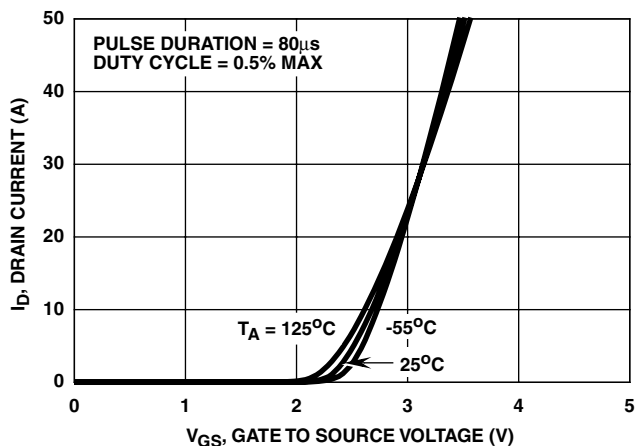


FIGURE 2. TRANSFER CHARACTERISTICS

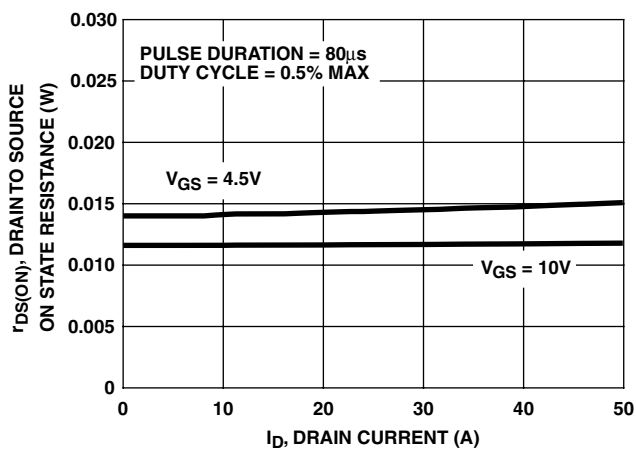


FIGURE 3. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

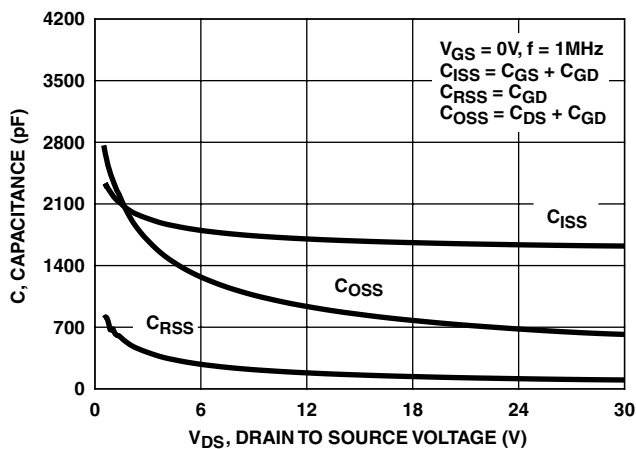


FIGURE 4. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

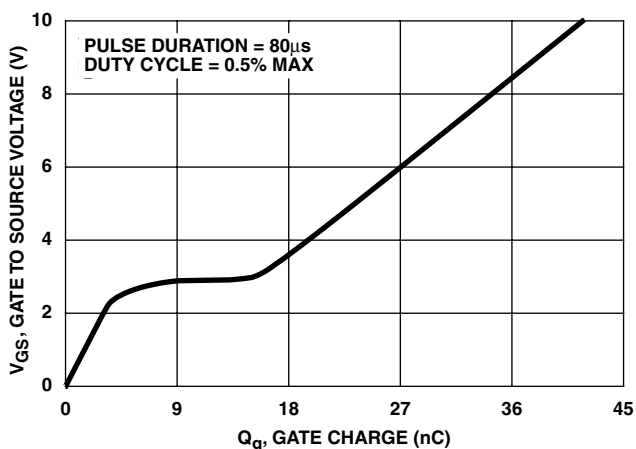


FIGURE 5. GATE TO SOURCE VOLTAGE vs GATE CHARGE

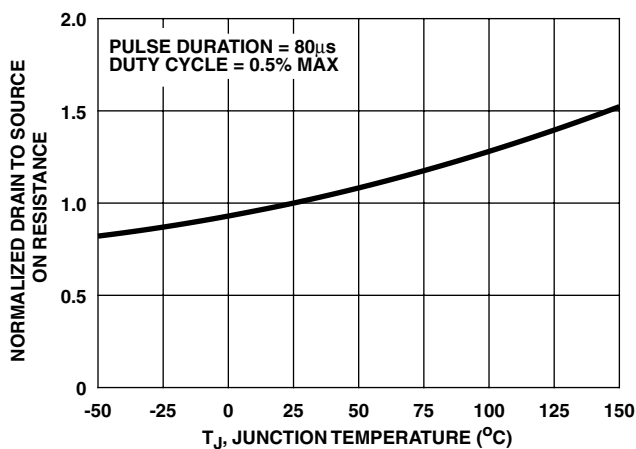


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

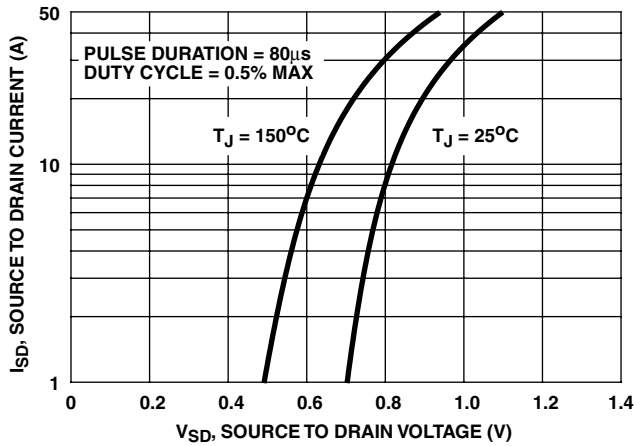


FIGURE 7. SOURCE TO DRAIN DIODE VOLTAGE

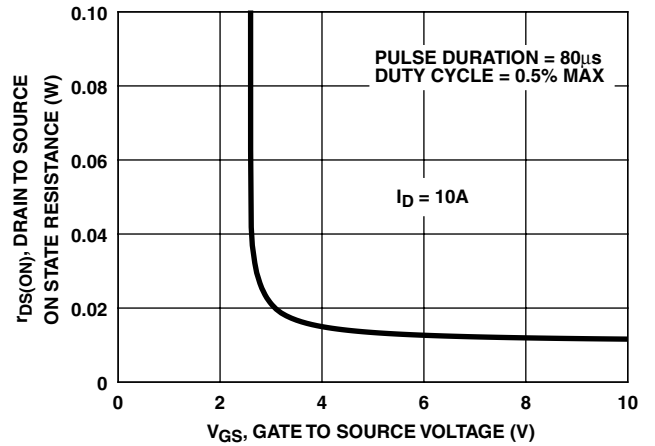


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE TO SOURCE VOLTAGE

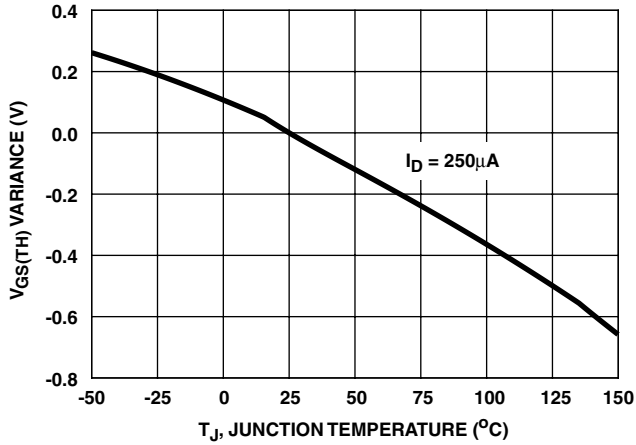


FIGURE 9. GATE THRESHOLD VOLTAGE VARIANCE vs JUNCTION TEMPERATURE

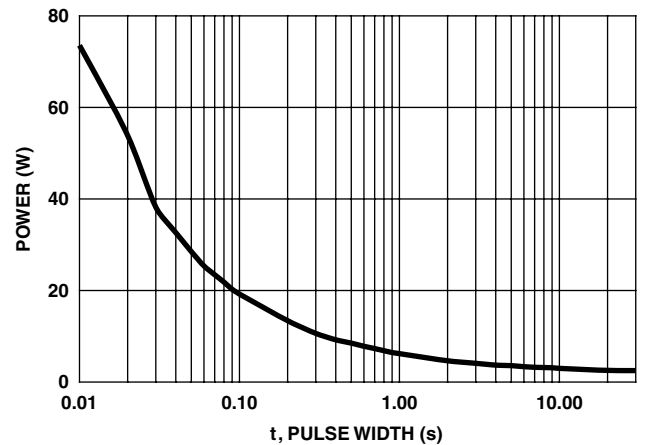


FIGURE 10. SINGLE PULSE POWER CAPABILITY vs PULSE WIDTH

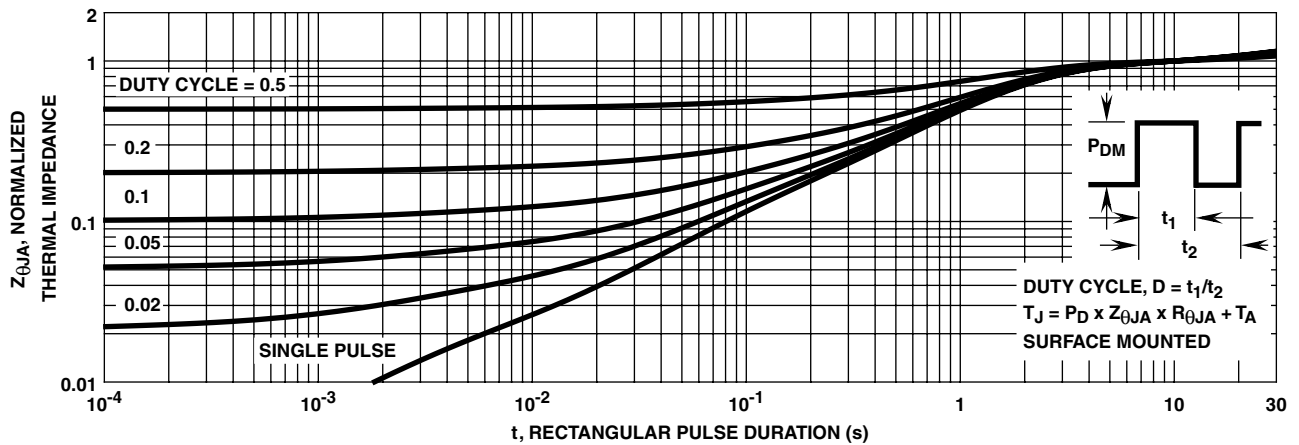


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

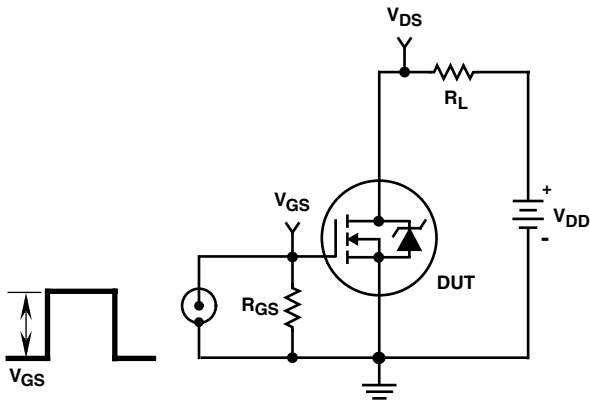


FIGURE 12. SWITCHING TIME TEST CIRCUIT

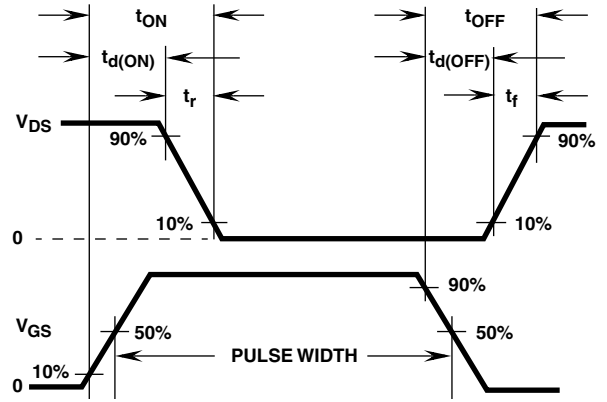


FIGURE 13. SWITCHING TIME WAVEFORM

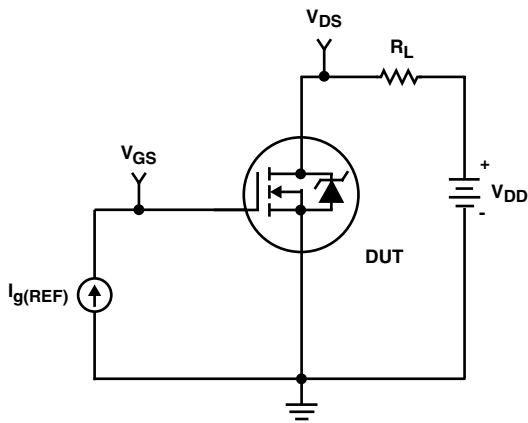


FIGURE 14. GATE CHARGE TEST CIRCUIT

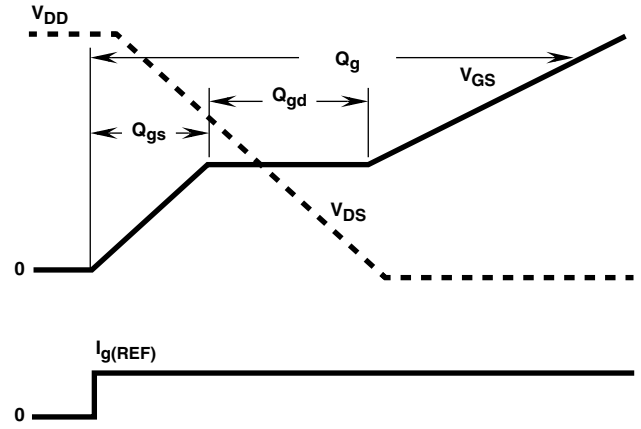


FIGURE 15. GATE CHARGE WsAVEFORMS

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE _x ™	FAST [®]	OPTOLOGIC™	SMART START™	VCX™
Bottomless™	FAST _r ™	OPTOPLANAR™	STAR*POWER™	
CoolFET™	FRFET™	PACMAN™	Stealth™	
CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOMET™	HiSeC™	PowerTrench [®]	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E ² CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER [®]	UltraFET [®]	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.