16-BIT, 1.0 GSPS Digital-to-Analog Converter (DAC)

Check for Samples: DAC5681

FEATURES

- **16-Bit Digital-to-Analog Converter (DAC)**
- **1.0 GSPS Update Rate**
- **16-Bit Wideband Input LVDS Data Bus**
  - **8 Sample Input FIFO**
  - **On-Chip Delay Lock Loop**
- **High Performance**
  - **73 dBc ACLR WCDMA TM1 at 180 MHz**
- **On Chip 1.2 V Reference**
- **Differential Scalable Output: 2 to 20 mA**
- **Package: 64-Pin 9 × 9 mm QFN**

APPLICATIONS

- **Cellular Base Stations**
- **Broadband Wireless Access (BWA)**
- **WiMAX 802.16**
- **Fixed Wireless Backhaul**
- **Cable Modem Termination System (CMTS)**
- **Medical / Test Instrumentation**
- **Radar Systems**

DESCRIPTION

The DAC5681 is a 16-bit 1.0 GSPS digital-to-analog converter (DAC) with wideband LVDS data input and internal voltage reference. The DAC5681 offers superior linearity and noise performance.

The DAC5681 integrates a wideband LVDS port with on-chip termination, providing full 1.0 GSPS data transfer into the DAC and lower EMI than traditional CMOS data interfaces. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock.

The current-steering architecture of the DAC5681 consists of a segmented array of current sinking switches directing up to 20mA of full-scale current to complementary output nodes. An accurate on-chip voltage reference is temperature-compensated and delivers a stable 1.2-V reference voltage. Optionally, an external reference may be used.

The DAC5681 is characterized for operation over the industrial temperature range of –40°C to 85°C and is available in a 64-pin QFN package. The device is pin upgradeable to the other members of the family: the DAC5681Z and DAC5682Z. The single-channel DAC5681Z and dual-channel DAC5682Z both provide optional 2x/4x interpolation and a clock multiplying PLL.

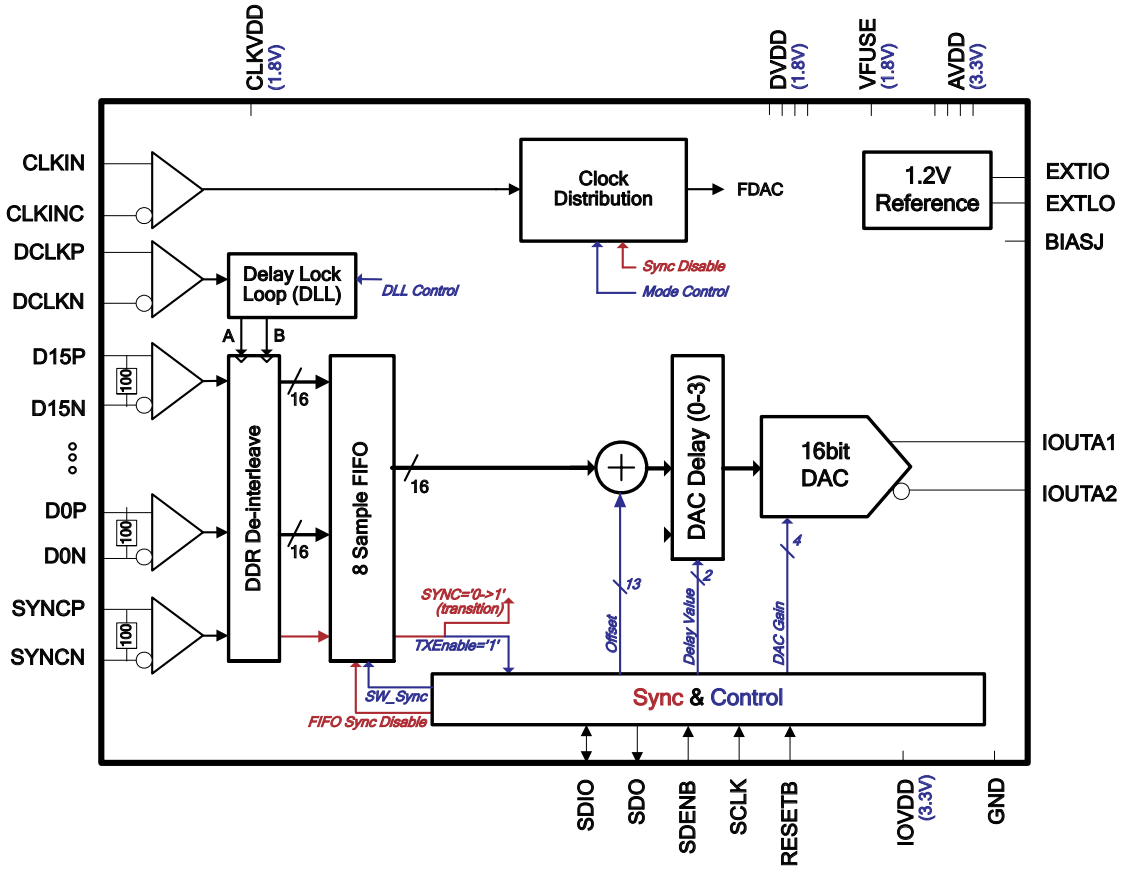
ORDERING INFORMATION

T_A	ORDER CODE	PACKAGE DRAWING/TYPE (1) (2) (3)	TRANSPORT MEDIA	QUANTITY
–40°C to 85°C	DAC5681IRGCT	RGC / 64QFN Quad Flatpack No-Lead	Tape and Reel	250
	DAC5681IRGCR		Tape and Reel	2000

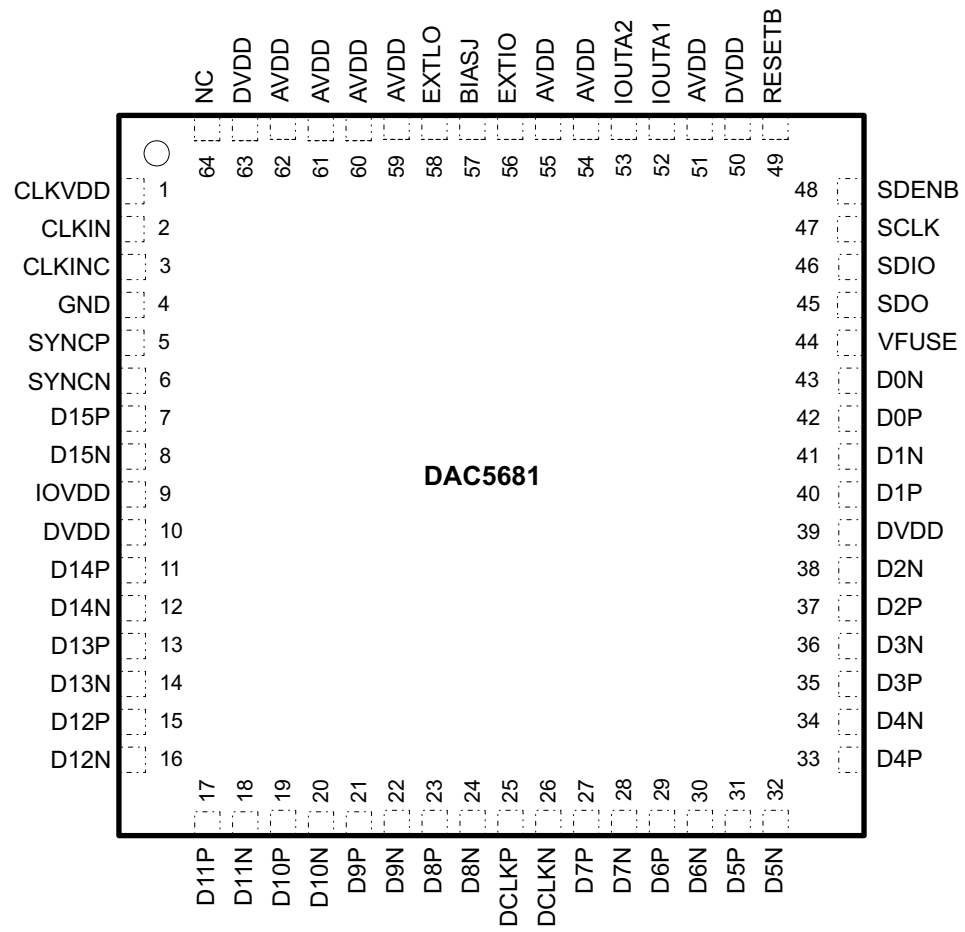
(1) Thermal Pad Size: 7,4 mm × 7,4 mm
(2) MSL Peak Temperature: Level-3-260C-168 HR
(3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



DAC5681
RGC PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AVDD	51, 54, 55, 59–62	I	Analog supply voltage. (3.3V)
BIASJ	57	O	Full-scale output current bias. For 20mA full-scale output current, connect a 960 Ω resistor to GND.
CLKIN	2	I	Positive external clock input with a self-bias of approximately CLKVDD/2.
CLKINC	3	I	Complementary external clock input. (See the CLKIN description)
CLKVDD	1	I	Internal clock buffer supply voltage. (1.8 V)
D[15..0]P	7, 11, 13, 15, 17, 19, 21, 23, 27, 29, 31, 33, 35, 37, 40, 42	I	LVDS positive input data bits 0 through 15. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Order of bus can be reversed via **rev_bus** bit in CONFIG5 register. Data format relative to DCLKP/N clock is Double Data Rate (DDR) with two data samples input per DCLKP/N clock. In dual-channel mode, data for the A-channel is input while DCLKP is high. D15P is most significant data bit (MSB) – pin 7 D0P is least significant data bit (LSB) – pin 42
D[15..0]N	8, 12, 14, 16, 18, 20, 22, 24, 28, 30, 32, 34, 36, 38, 41, 43	I	LVDS negative input data bits 0 through 15. (See D[15:0]P description above) D15N is most significant data bit (MSB) – pin 8 D0N is least significant data bit (LSB) – pin 43

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DCLKP	25	I	LVDS positive input clock. Unlike the other LVDS inputs, the DCLKP/N pair is self-biased to approximately DVDD/2 and does **not** have an internal termination resistor in order to optimize operation of the DLL circuit. See the “DLL Operation” section. For proper external termination, connect a 100 Ω resistor across LVDS clock source lines followed by series 0.01 µF capacitors connected to each of DCLKP and DCLKN pins (see Figure 17). For best performance, the resistor and capacitors should be placed as close as possible to these pins.
DCLKN	26	I	LVDS negative input clock. (See the DCLKP description)
DVDD	10, 39, 50, 63	I	Digital supply voltage. (1.8 V)
EXTIO	56	I/O	Used as external reference input when internal reference is disabled (i.e., EXTLO connected to AVDD). Used as 1.2V internal reference output when EXTLO = GND, requires a 0.1 µF decoupling capacitor to AGND when used as reference output.
EXTLO	58	O	Connect to GND for internal reference, or AVDD for external reference.
GND	4, Thermal Pad	I	Pin 4 and the Thermal Pad located on the bottom of the QFN package is ground for AVDD, DVDD and IOVDD supplies.
IOUTA1	52	O	DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current sink and the least positive voltage on the IOUTA1 pin. Similarly, a 0xFFFF data input results in a 0 mA current sink and the most positive voltage on the IOUTA1 pin.
IOUTA2	53	O	DAC complementary current output. The IOUTA2 has the opposite behavior of the IOUTA1 described above. An input data value of 0x0000 results in a 0mA sink and the most positive voltage on the IOUTA2 pin.
IOVDD	9	I	Digital I/O supply voltage (3.3V) for pins RESETB, SCLK, SDENB, SDIO, SDO.
NC	64	I	No Connect. Leave open for proper operation.
RESETB	49	I	Resets the chip when low. Internal pull-up.
SCLK	47	I	Serial interface clock. Internal pull-down.
SDENB	48	I	Active low serial data enable, always an input to the DAC5681. Internal pull-up.
SDIO	46	I/O	Bi-directional serial interface data in 3-pin mode (default). In 4-pin interface mode (CONFIG5 **sif4**), the SDIO pin is an input only. Internal pull-down.
SDO	45	O	Uni-directional serial interface data in 4-pin mode (CONFIG5 **sif4**). The SDO pin is in high-impedance state in 3-pin interface mode (default), but can optionally be used as a status output pin via CONFIG14 **SDO_func_sel(2:0)**. Internal pull-down.
SYNCP	5	I	LVDS SYNC positive input data. The SYNCP/N LVDS pair has an internal 100 Ω termination resistor. By default, the **SYNCP/N input must be logic ‘1’ to enable a DAC analog output**. See the *LVDS SYNCP/N Operation* paragraph for a detailed description.
SYNCN	6	I	LVDS SYNC negative input data.
VFUSE	44	I	Digital supply voltage. (1.8V) **Connect to DVDD pins for normal operation**. This supply pin is also used for factory fuse programming.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Supply voltage range	DVDD(2)	–0.5 to 2.3	V
	VFUSE(2)	–0.5 to 2.3	V
	CLKVDD(2)	–0.5 to 2.3	V
	AVDD(2)	–0.5 to 4	V
	IOVDD(2)	–0.5 to 4	V
Terminal voltage range	AVDD to DVDD	–2 to 2.6	V
	CLKVDD to DVDD	–0.5 to 0.5	V
	IOVDD to AVDD	–0.5 to 0.5	V
	D[15..0]P ,D[15..0]N, SYNCP, SYNCN (2)	–0.5 to DVDD + 0.5	V
	DCLKP, DCLKN(2)	–0.3 to 2.1	V
	CLKIN, CLKINC(2)	–0.5 to CLKVDD + 0.5	V
	SDO, SDIO, SCLK, SDENB, RESETB (2)	–0.5 to IOVDD + 0.5	V
	IOUTA1, IOUTA2 (2)	–0.5 to AVDD + 0.5	V
	EXTIO, EXTLO, BIASJ(2)	–0.5 to AVDD + 0.5	V
Peak input current (any input)		20	mA
Peak total input current (all inputs)		–30	mA
Operating free-air temperature range, T_A: DAC5681		–40 To 85	°C
Storage temperature range		–65 To 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to GND.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL CONDUCTIVITY		64ld QFN	UNIT
T_J	Maximum junction temperature (1)	125	°C
θ_{JA}	Theta junction-to-ambient (still air)	20	°C/W
	Theta junction-to-ambient (150 lfm)	16	
θ_{JC}	Theta junction-to-case	7	°C/W
θ_{JP}	Theta junction-to-pad	0.2	°C/W

(1) Air flow or heat sinking reduces θ_{JA} and may be required for sustained operation at 85° under maximum operating conditions.

ELECTRICAL CHARACTERISTICS — DC SPECIFICATION

over operating free-air temperature range , AVDD = 3.3 V, CLKVDD = 1.8 V, IOVDD = 3.3 V, DVDD = 1.8 V, $Iout_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION			16			Bits
DC ACCURACY(1)						
INL	Integral nonlinearity	1 LSB = IOUTFS/2^{16}		±4		LSB
DNL	Differential nonlinearity			±2		
ANALOG OUTPUT						
	Coarse gain linearity			±0.04		LSB
	Offset error	Mid code offset		0.01		%FSR
	Gain error	With external reference		1		%FSR
	Gain error	With internal reference		0.7		%FSR
	Minimum full scale output current(2)			2		mA
	Maximum full scale output current(2)			20		
	Output Compliance range(3)	IOUTFS = 20 mA	AVDD –0.5V		AVDD + 0.5V	V
	Output resistance			300		kΩ
	Output capacitance			5		pF
REFERENCE OUTPUT						
V_{ref}	Reference voltage		1.14	1.2	1.26	V
	Reference output current(4)			100		nA
REFERENCE INPUT						
V_{EXTIO}	Input voltage range		0.1		1.25	V
	Input resistance			1		MΩ
	Small signal bandwidth	CONFIG6: BiasLPF_A = 0		95		kHz
		CONFIG6: BiasLPF_A = 1		472		
	Input capacitance			100		pF
TEMPERATURE COEFFICIENTS						
	Offset drift			±1		ppm of FSR/°C
	Gain drift	With external reference		±15		ppm of FSR/°C
		With internal reference		±30		
	Reference voltage drift			±8		ppm/°C
POWER SUPPLY						
	Analog supply voltage, AVDD		3.0	3.3	3.6	V
	Digital supply voltage, DVDD		1.71	1.8	2.15	V
	Clock supply voltage, CLKVDD		1.71	1.8	2.15	V
	I/O supply voltage, IOVDD		3.0	3.3	3.6	V
$I_{(AVDD)}$	Analog supply current	Mode 1 (below)		67		mA
$I_{(DVDD)}$	Digital supply current			191		mA
$I_{(CLKVDD)}$	Clock supply current			15		mA
$I_{(IOVDD)}$	IO supply current			4		mA

(1) Measured differential across IOUTA1 and IOUTA2 with 25 Ω each to AVDD.
(2) Nominal full-scale current, IoutFS, equals 16 × IBIAS current.
(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5681 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
(4) Use an external buffer amplifier with high impedance input to drive any external load.

ELECTRICAL CHARACTERISTICS — DC SPECIFICATION (continued)

over operating free-air temperature range , AVDD = 3.3 V, CLKVDD = 1.8 V, IOVDD = 3.3 V, DVDD = 1.8 V, $Iout_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(AVDD)}$	Sleep mode, AVDD supply current	Mode 3 (below)		1.5		mA
$I_{(DVDD)}$	Sleep mode, DVDD supply current			91		mA
$I_{(CLKVDD)}$	Sleep mode, CLKVDD supply current			15		mA
$I_{(IOVDD)}$	Sleep mode, IOVDD supply current			1.5		mA
P	AVDD + IOVDD current, 3.3V	Mode 1: CLKIN = 1000 MHz IF = 40 MHz Single Tone, 0 dBFS		71		mA
	DVDD + CLKVDD current, 1.8V			206		mA
	Power Dissipation			605	650	mW
	AVDD + IOVDD current, 3.3V	Mode 2: CLKIN = 500 MHz IF = 40 MHz Single Tone, 0 dBFS		71		mA
	DVDD + CLKVDD current, 1.8V			111		mA
	Power Dissipation			435		mW
	AVDD + IOVDD current, 3.3V	Mode 3: CLKIN = 1000 MHz DAC on SLEEP, Static Data Pattern		3		mA
	DVDD + CLKVDD current, 1.8V			106		mA
	Power Dissipation			200		mW
	AVDD + IOVDD current, 3.3V	Mode 4: CLKIN = OFF DAC on SLEEP, Static Data Pattern		3		mA
	DVDD + CLKVDD current, 1.8V			6		mA
	Power Dissipation			20	30	mW
PSRR	Power supply rejection ratio	DC tested	–0.2		0.2	%FSR/V
T	Operating range		–40		85	°C

ELECTRICAL CHARACTERISTICS — AC SPECIFICATION(1)

Over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA, 4:1 transformer output termination, 50Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
f_{CLK}	Maximum output update rate		1000			MSPS
$t_{s(DAC)}$	Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF		10.4		ns
t_{pd}	Output propagation delay	DAC output is updated on falling edge of DAC clock. Does not include Digital Latency (see below).		2.5		ns
$t_{r(IOUT)}$	Output rise time 10% to 90%			220		ps
$t_{f(IOUT)}$	Output fall time 90% to 10%			220		ps
Digital Latency				76		DAC clock cycles
Power-up Time	DAC Wake-up Time(2)	BiasLPF_A enabled; register 0x06, Bit 3 set to 1.		8		µs
		BiasLPF_A disabled; register 0x06, Bit 3 set to 0.		80		µs
	DAC Sleep Time (3)	BiasLPF_A enabled; register 0x06, Bit 3 set to 1.		8		µs
		BiasLPF_A disabled; register 0x06, Bit 3 set to 0.		80		µs
AC PERFORMANCE						
SFDR	Spurious free dynamic range	CLKIN = 500 MHz, IF = 5.1 MHz, First Nyquist Zone < $f_{DATA}/2$		81		dBc
		CLKIN = 1000 MHz, IF = 5.1 MHz, First Nyquist Zone < $f_{DATA}/2$		80		
		CLKIN = 1000 MHz, IF = 20.1 MHz, First Nyquist Zone < $f_{DATA}/2$		77		
SNR	Signal-to-noise ratio	CLKIN = 500 MHZ, Single tone, 0 dBFS, IF = 20.1 MHz		75		dBc
		CLKIN = 1000 MHZ, Single tone, 0 dBFS, IF = 20.1 MHz		70		
		CLKIN = 1000 MHZ, Single tone, 0 dBFS, IF = 70.1 MHz		66		
		CLKIN = 1000 MHZ, Single tone, 0 dBFS, IF = 180 MHz		60		
		CLKIN = 1000 MHZ, Single tone, 0 dBFS, IF = 300.2 MHz		60		
		CLKIN = 1000 MHZ, Four tone, each -12 dBFS, IF = 24.7, 24.9, 25.1 and 25.3 MHz		73		
IMD3	Third-order two-tone intermodulation (each tone at –6 dBFS)	CLKIN = 1000 MHZ, IF = 20.1 and 21.1 MHz		88		dBc
		CLKIN = 1000 MHZ, IF = 70.1 and 71.1 MHz		75		
		CLKIN = 1000 MHZ, IF = 150.1 and 151.1 MHz		67		
IMD	Four-tone intermodulation (each tone at –12 dBFS)	CLKIN = 1000 MHz, IF = 298.4, 299.2, 300.8 and 301.6 MHz		64		dBc
ACLR(4)	Adjacent channel leakage ratio	Single carrier, baseband, CLKIN = 983.04 MHz	80	83		dBc
		Single carrier, IF = 180 MHz, CLKIN = 983.04 MHz		73		
		Four carrier, IF = 180 MHz, CLKIN = 983.04 MHz		68		
		Four carrier, IF = 275 MHz, CLKIN = 983.04 MHz		66		
	Noise floor(5)	50-MHz offset, 1-MHz BW, Single Carrier, baseband, CLKIN = 983.04		93		dBc
		50-MHz offset, 1-MHz BW, Four Carrier, baseband, CLKIN = 983.04		85		

(1) Measured single-ended into 50 Ω load.
(2) IOUT current settling to 1% of $IOUT_{FS}$. Measured from SDENB rising edge; Register 0x06, toggle Bit 4 from 1 to 0.
(3) IOUT current settling to less than 1% of $IOUT_{FS}$. Measured from SDENB rising edge; Register 0x06, toggle Bit 4 from 0 to 1.
(4) W-CDMA with 3.84 MHz BW, 5-MHz spacing, centered at IF. TESTMODEL 1, 10 ms
(5) Carrier power measured in 3.84 MHz BW.

ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3V, CLKVDD, DVDD = 1.8V.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
LVDS INTERFACE: D[15:0]P/N, SYNCP/N, DCLKP/N (1)								
$V_{A,B+}$	Logic high differential input voltage threshold				175			mV
$V_{A,B-}$	Logic low differential input voltage threshold				–175			mV
V_{COM1}	Input Common Mode	SYNCP/N, D[15:0]P/N only			1.0			V
V_{COM2}	Input Common Mode	DCLKP/N only				DVDD ÷2		V
Z_T	Internal termination	SYNCP/N, D[15:0]P/N only			85	110	135	Ω
C_L	LVDS Input capacitance					2		pF
t_S, t_H	DCLK to Data	DCLKP/N: 0 to 125MHz (see Figure 20) DLL Disabled, CONFIG5 **DLL_bypass** = 1, CONFIG10 = '00000000'		Setup_min		1100		ps
				Hold_min		–600		
$t_{SKEW(A)}$, $t_{SKEW(B)}$	DCLK to Data Skew(2)	DLL Enabled, CONFIG5 **DLL_bypass** = 0, DDR format	DCLKP/N = 150 MHz	Positive		1000		ps
				Negative		–1800		
			DCLKP/N = 200 MHz	Positive		800		
				Negative		–1300		
			DCLKP/N = 250 MHz	Positive		600		
				Negative		–1000		
			DCLKP/N = 300 MHz	Positive		450		
				Negative		–800		
			DCLKP/N = 350 MHz	Positive		400		
				Negative		–700		
			DCLKP/N = 400 MHz	Positive		300		
				Negative		–600		
			DCLKP/N = 450 MHz	Positive		300		
				Negative		–500		
			DCLKP/N = 500 MHz	Positive		350		
				Negative		–300		
f_{DATA}	Input data rate supported	DLL Disabled, CONFIG5 **DLL_bypass** = 1, DDR format, DCLKP frequency: <125 MHz					250	MSPS
		DLL Enabled, CONFIG5 **DLL_bypass** = 0, DDR format, DCLKP frequency: 125 to 500 MHz			250		1000	
	DLL Operating Frequency (DCLKP/N Frequency)	DLL Enabled, CONFIG5 **DLL_bypass** = 0, DDR format	CONFIG10 = '11001101' = 0xCD			125-150		MHz
			CONFIG10 = '11001110' = 0xCE			150-175		
			CONFIG10 = '11001111' = 0xCF			175-200		
			CONFIG10 = '11001000' = 0xC8			200-325		
			CONFIG10 = '11000000' = 0xC0			325-500		

(1) See LVDS INPUTS section for terminology.
(2) Positive skew: Clock ahead of data.
Negative skew: Data ahead of clock.

ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS) (continued)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3V, CLKVDD, DVDD = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS INTERFACE: SDO, SDIO, SCLK, SDENB, RESETB						
V_{IH}	High-level input voltage		2	3		V
V_{IL}	Low-level input voltage		0	0	0.8	V
I_{IH}	High-level input current			±20		µA
I_{IL}	Low-level input current			±20		µA
CI	CMOS Input capacitance			5		pF
V_{OH}	SDO, SDIO	I_{load} = –100 µA		IOVDD –0.2		V
		I_{load} = –2mA		0.8 x IOVDD		V
V_{OL}	SDO, SDIO	I_{load} = 100 µA		0.2		V
		I_{load} = 2 mA		0.5		V
$t_{s(SDENB)}$	Setup time, SDENB to rising edge of SCLK		20			ns
$t_{s(SDIO)}$	Setup time, SDIO valid to rising edge of SCLK		10			ns
$t_{h(SDIO)}$	Hold time, SDIO valid to rising edge of SCLK		5			ns
$t_{(SCLK)}$	Period of SCLK		100			ns
$t_{(SCLKH)}$	High time of SCLK		40			ns
$t_{(SCLKL)}$	Low time of SCLK		40			ns
$t_{d(Data)}$	Data output delay after falling edge of SCLK			10		ns
t_{RESET}	Minimum RESETB pulse width			25		ns
CLOCK INPUT (CLKIN/CLKINC)						
	Duty cycle			50%		
	Differential voltage(3)		0.4	1		V
	CLKIN/CLKINC input common mode			CLKVDD ÷2		V

(3) Driving the clock input with a differential voltage lower than 1V will result in degraded performance.

TYPICAL CHARACTERISTICS

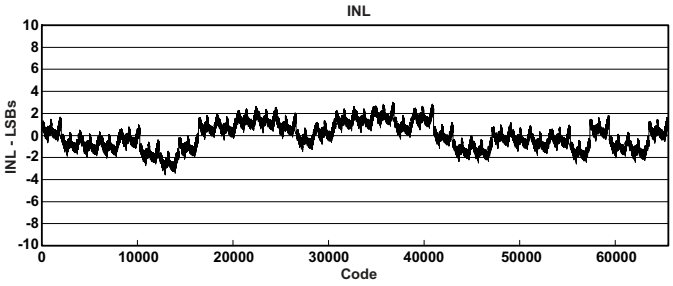


Figure 1. Integral Nonlinearity

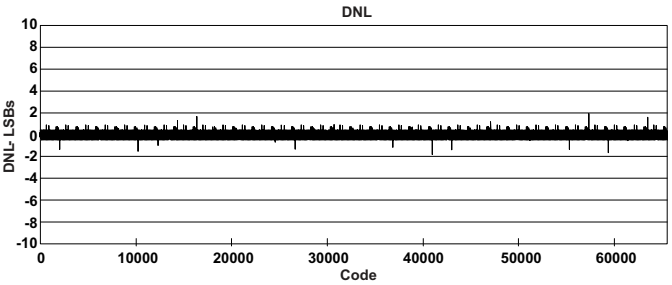


Figure 2. Differential Nonlinearity

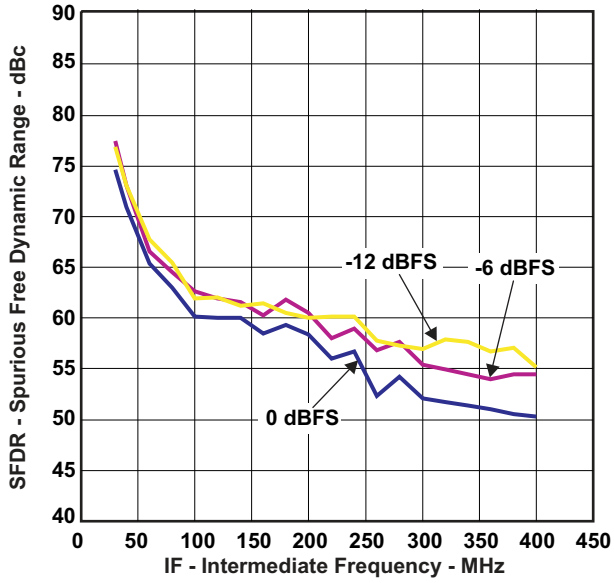


Figure 3. SFDR vs IF

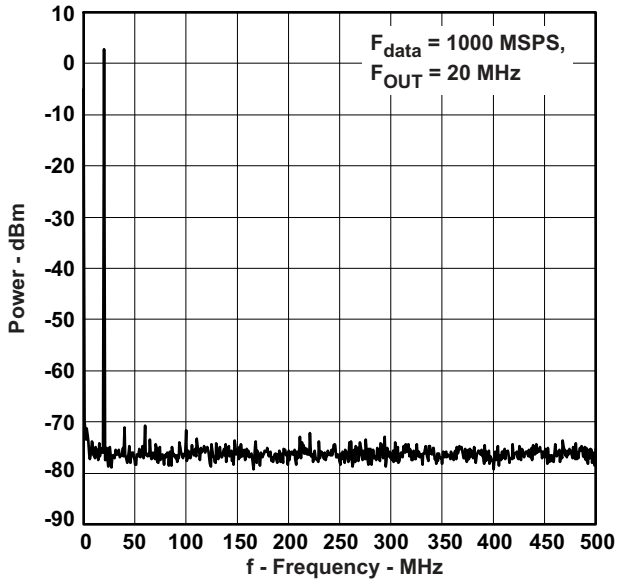


Figure 4. Single-Tone Spectral Plot

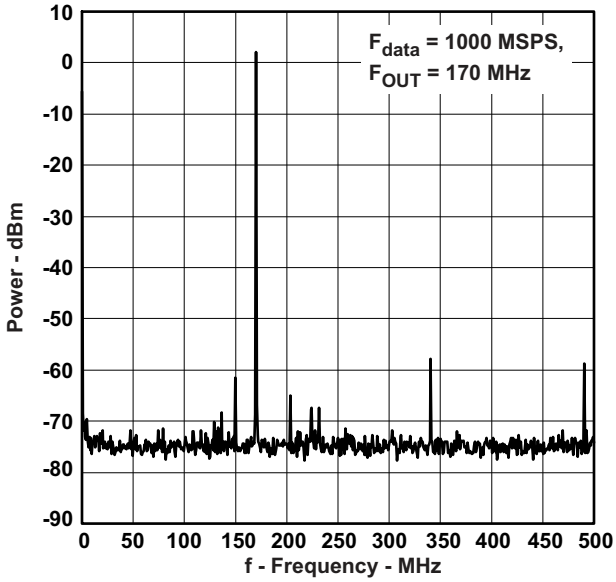


Figure 5. Single-Tone Spectral Plot

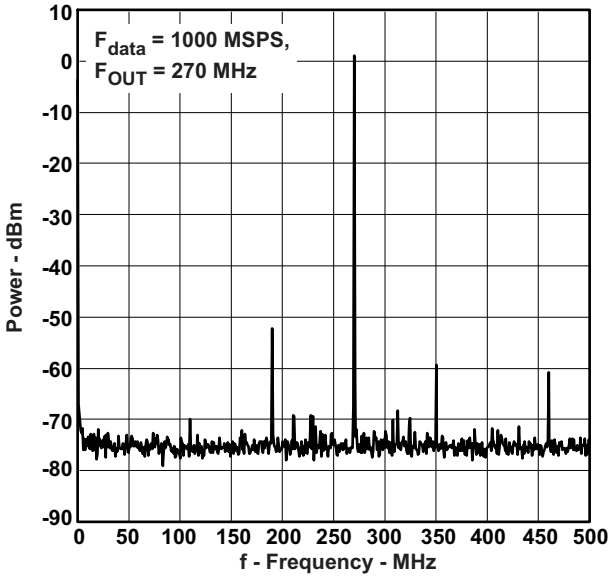


Figure 6. Single-Tone Spectral Plot

TYPICAL CHARACTERISTICS (continued)

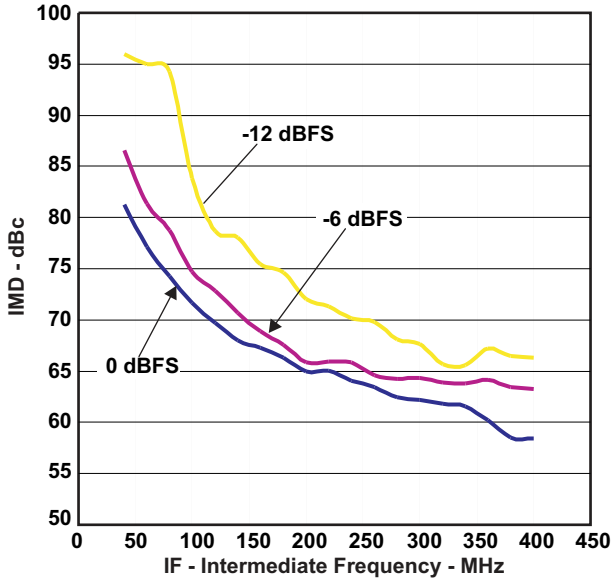


Figure 7. Two-Tone IMD vs Output Frequency

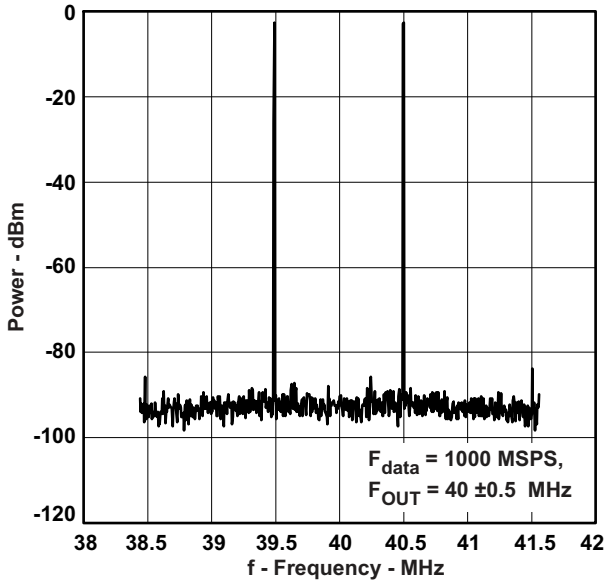


Figure 8. Two-Tone IMD Spectral Plot

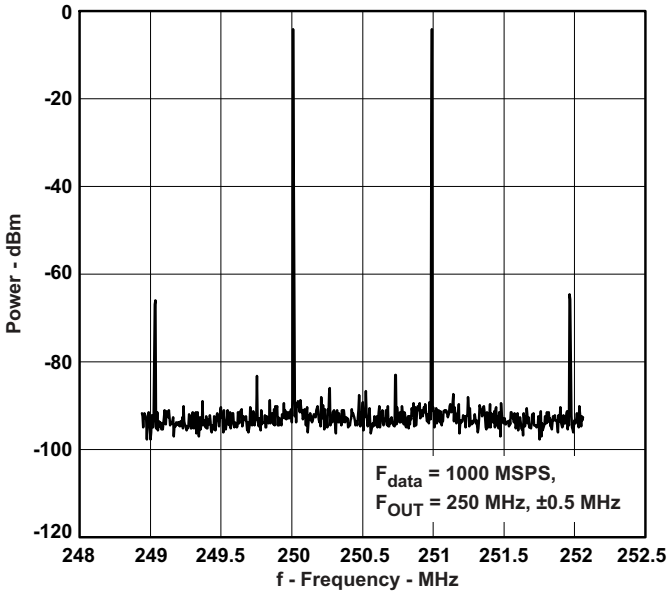


Figure 9. Two-Tone IMD Spectral Plot

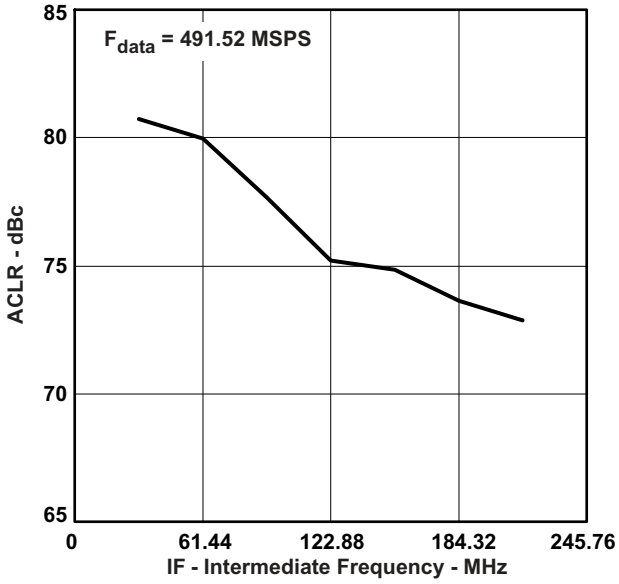


Figure 10. Single Carrier W-CDMA Test Model 1 - ACLR vs IF

TYPICAL CHARACTERISTICS (continued)

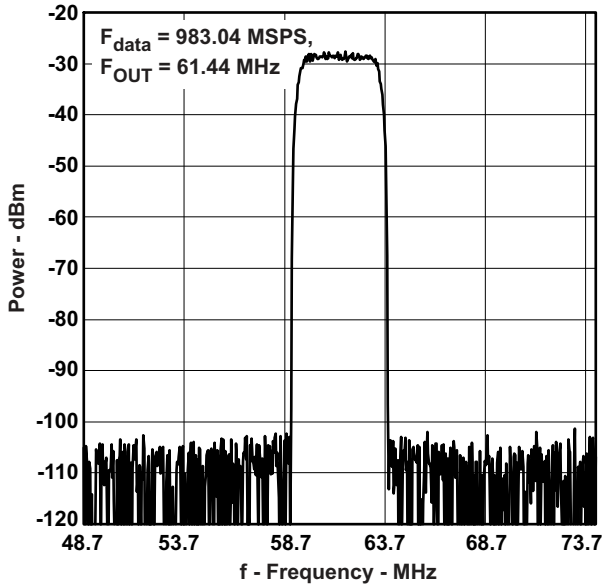


Figure 11. Single Carrier W-CDMA Test Model 1
Carrier Power: -8.2 dBm, ACLR 79.7 dB

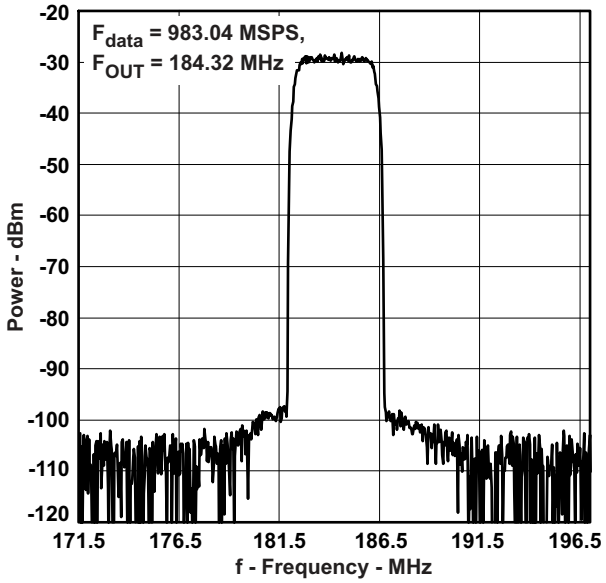


Figure 12. Single Carrier W-CDMA Test Model 1
Carrier Power: -9 dBm, ACLR 73.3 dB

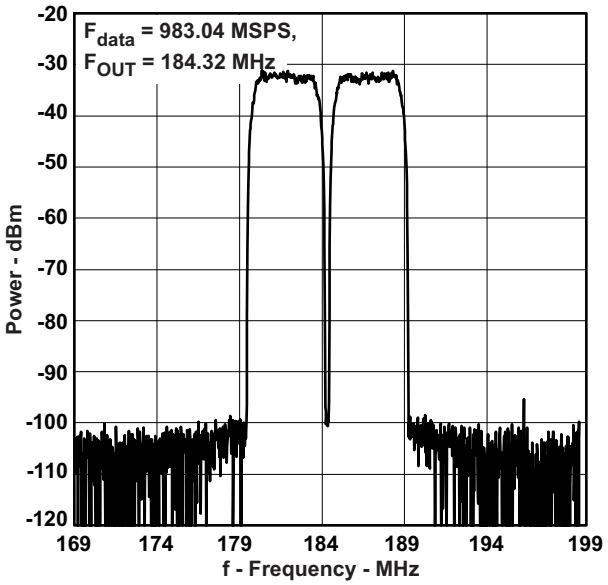


Figure 13. Two Carrier W-CDMA Test Model 1
Carrier Power: -12 dBm, ACLR 70.6 dB

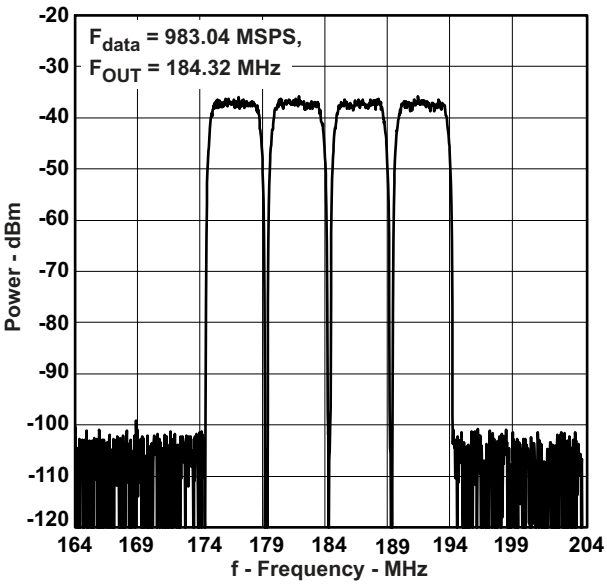


Figure 14. Four Carrier W-CDMA Test Model 1
Carrier Power: -16.8 dBm, ACLR 68.3 dB

TYPICAL CHARACTERISTICS (continued)

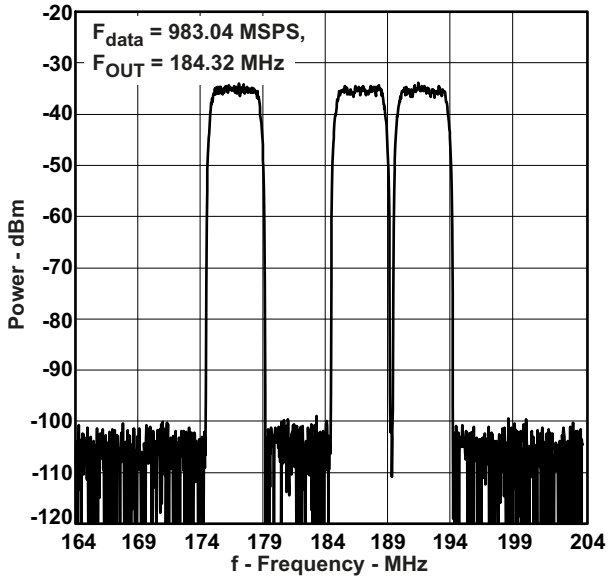


Figure 15. Three Carrier W-CDMA Test Model 1 with GAP Carrier Power: -14.8 dBm, ACLR 70.1 dB

TEST METHODOLOGY

Typical AC specifications were characterized with the DAC5681EVM using the test configuration shown in Figure 16. A sinusoidal master clock frequency is generated by an HP8665B signal generator and into a splitter. One output drives an Agilent 8133A pulse generator, and the other drives the CDCM7005 clock driver. The 8133A converts the sinusoidal frequency into a square wave output clock and drives an Agilent ParBERT 81250A pattern-generator clock. On the EVM, the DAC5681 CLKIN/C input clock is driven by an CDCM7005 clock distribution chip that is configured to simply buffer the external 8665B clock.

The DAC5681 output is characterized with a Rohde and Schwarz FSU spectrum analyzer. For WCDMA signal characterization, it is important to use a spectrum analyzer with high IP3 and noise subtraction capability so that the spectrum analyzer does not limit the ACPR measurement.

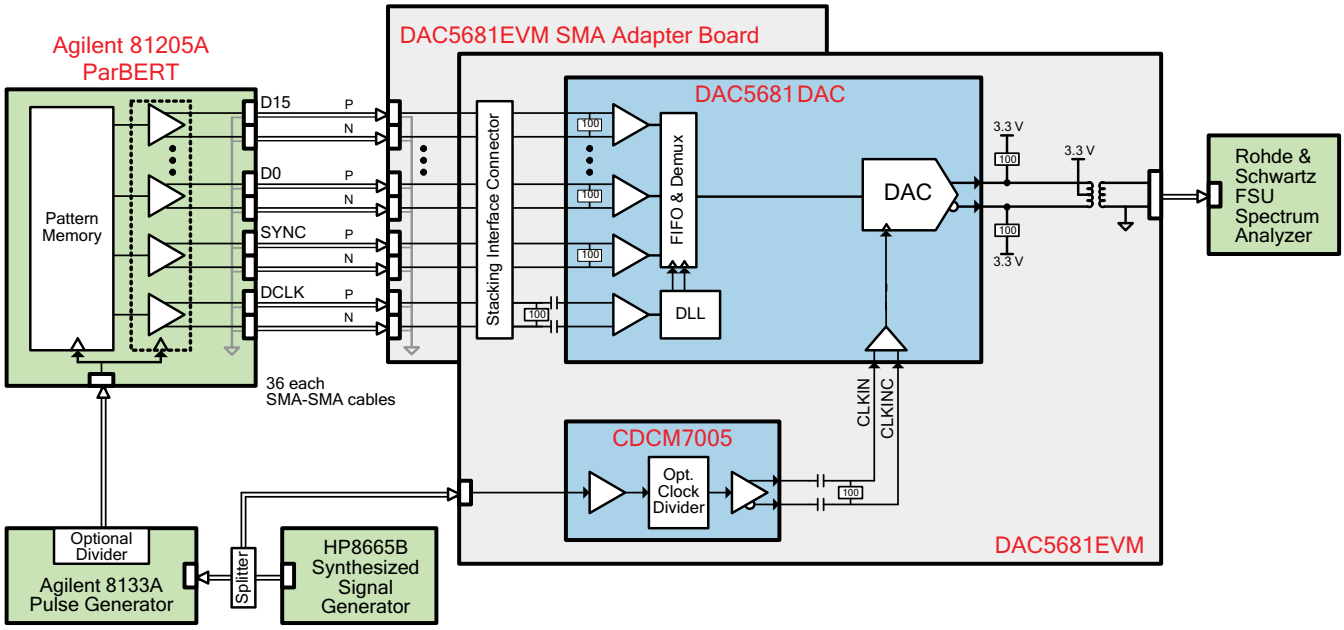


Figure 16. DAC5681 Test Configuration

DEFINITION OF SPECIFICATIONS

Adjacent Carrier Leakage Ratio (ACLR): Defined for a 3.84Mcps 3GPP W-CDMA input signal measured in a 3.84MHz bandwidth at a 5MHz offset from the carrier with a 12dB peak-to-average ratio.

Analog and Digital Power Supply Rejection Ratio (APSSR, DPSSR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3, IMD): The two-tone IMD3 or four-tone IMD is defined as the ratio (in dBc) of the worst 3rd-order (or higher) intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio of the differential output current (IOUT1–IOUT2) and the mid-scale output current.

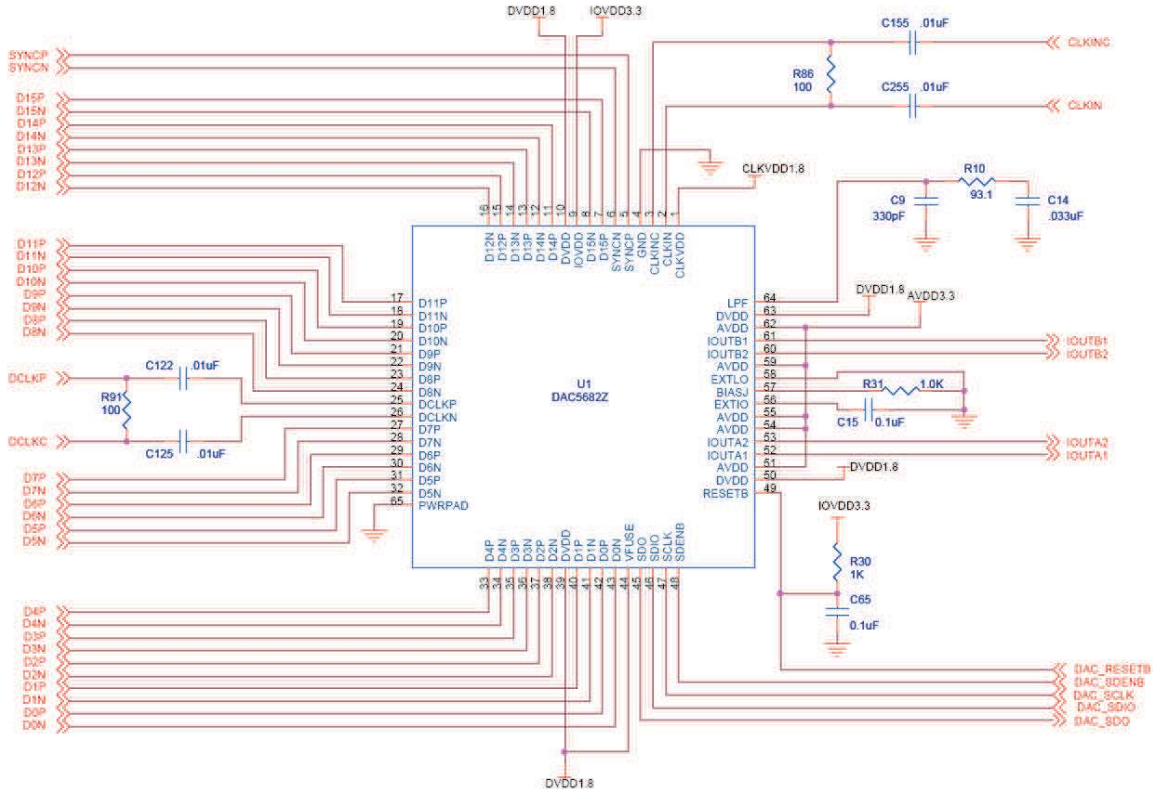
Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

Spurious Free Dynamic Range (SFDR): Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

Signal to Noise Ratio (SNR): Defined as the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

TYPICAL APPLICATION SCHEMATIC



(1) Power supply decoupling capacitors not shown.

(2) Internal Reference configuration shown.

Figure 17. Schematic

DETAILED DESCRIPTION

Table 1. Register Map

Name	Address	Default	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0
STATUS0	0x00	0x1F	Reserved	DLL_lock	Unused	device_ID(2:0)			version(1:0)	
CONFIG1	0x01	0x10	DAC_delay(1:0)		Unused	Reserved	SLFTST _ena	FIFO_offset(2:0)		
CONFIG2	0x02	0xC0	Twos_ comp	Reserved	Reserved	Unused	Reserved			
CONFIG3	0x03	0x70	DAC_offset _ena	SLFTST_err _mask	FIFO_err_ mask	Pattern_err _mask	Reserved	Reserved	SW_sync	SW_sync _sel
STATUS4	0x04	0x00	Unused	SLFTST_err	FIFO_err	Pattern_ err	Unused	Unused	Unused	Unused
CONFIG5	0x05	0x00	SIF4	rev_bus	clkdiv_ sync_dis	Reserved	Reserved	DLL_ bypass	Reserved	Reserved
CONFIG6	0x06	0x0C	Reserved	Unused	Reserved	Sleep_A	BiasLPF_A	Reserved	Reserved	DLL_ sleep
CONFIG7	0x07	0xFF	DACA_gain(3:0)				Reserved			
CONFIG8	0x08	0x00	Reserved					DLL_ restart	Reserved	
CONFIG9	0x09	0x00	Reserved							
CONFIG10	0x0A	0x00	DLL_delay(3:0)				DLL_invclk	DLL_ifixed(2:0)		
CONFIG11	0x0B	0x00	Reserved							
CONFIG12	0x0C	0x00	Reserved		Offset_sync	OffsetA(12:8)				
CONFIG13	0x0D	0x00	OffsetA(7:0)							
CONFIG14	0x0E	0x00	SDO_func_sel(2:0)			Reserved				
CONFIG15	0x0F	0x00	Reserved							

Register name: STATUS0 – Address: 0x00, Default = 0x1F

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	DLL_lock	Unused	device_ID(2:0)			version(1:0)	
0	0	0	1	1	1	1	1

Reserved (Bit 7): Set to '0' by default.

DLL_lock: Asserted when the internal DLL is locked. Once the DLL is locked, this bit should remain a '1' unless the DCLK input clock is removed or abruptly changes frequency causing the DLL to fall out of lock. (**Read Only**)

device_ID(2:0): Returns '111' for DAC5681 Device_ID code. (**ReadOnly**)

version(1:0): A hardwired register that contains the register set version of the chip. (**ReadOnly**)

version (1:0)	**Identification**
'01'	PG1.0 Initial Register Set
'10'	PG1.1 Register Set
'11'	Production Register Set

Register name: CONFIG1 – Address: 0x01, Default = 0x10

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC_delay(1:0)		Unused	Reserved	SLFTST_ena	FIFO_offset(2:0)		
0	0	0	1	0	0	0	0

DAC_delay(1:0): DAC data delay adjustment. (0–3 periods of the DAC clock) This can be used to adjust system level output timing. The same delay is applied to DACA data paths.

Reserved (Bit 4): Set to '1' for proper operation.

SLFTST_ena: When set, a Digital Self Test (SLFTST) of the core logic is enabled. Refer to *Digital Self Test Mode* section for details on SLFTST operation.

FIFO_offset(2:0): Programs the FIFO's output pointer location, allowing the input pointer to be shifted –4 to +3 positions upon SYNC. Default offset is 0 and is updated upon each sync event.

FIFO_offset(2:0)	Offset
011	+3
010	+2
001	+1
000	0
111	–1
110	–2
101	–3
100	–4

Register name: CONFIG2 – Address: 0x02, Default = 0xC0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Twos_comp	Reserved	Reserved	Unused	Reserved			
1	1	0	0	0	0	0	0

Twos_comp: When set (default) the input data format is expected to be 2s complement, otherwise offset binary format is expected.

Reserved (Bit 6): Set to '1' for proper operation.

Reserved (Bit 5): Set to '0' for proper operation.

Reserved (3:0): Set to '0000' for proper operation.

Register name: CONFIG3 – Address: 0x03, Default = 0x70

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC_offset _ena	SLFTST_err _mask	FIFO_err_ mask	Pattern_err_ mask	Reserved	Reserved	SW_sync	SW_sync_sel
0	1	1	1	0	0	0	0

DAC_offset_ena: When set, the values of **OffsetA(12:0)** in CONFIG12 through CONFIG13 registers are summed into the DAC-A data path. This provides a system-level offset adjustment capability that is independent of the input data.

SLFTST_err_mask: When set, masks out the **SLFTST_err** bit in STATUS4 register. Refer to *Digital Self Test Mode* section for details on SLFTST operation.

FIFO_err_mask: When set, masks out the **FIFO_err** bit in STATUS4 register.

Pattern_err_mask: When set, masks out the **Pattern err** bit in STATUS4 register.

Reserved (Bit 3): Set to '0' for proper operation.

Reserved (Bit 2): Set to '0' for proper operation.

SW_sync: This bit can be used as a substitute for the LVDS external SYNC input pins for both synchronization and transmit enable control.

SW_sync_sel: When set, the SW_sync bit is used as the only synchronization input and the LVDS external SYNC input pins are ignored.

Register name: STATUS4 – Address: 0x04, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	SLFTST_err	FIFO_err	Pattern_err	Unused	Unused	Unused	Unused
0	0	0	0	0	0	0	0

SLFTST_err: Asserted when the Digital Self Test (SLFTST) fails. To clear the error, write a '0' to this register bit. This bit is also output on the SDO pin when the Self Test is enabled via **SLFTST_ena** control bit in CONFIG1. Refer to *Digital Self Test Mode* section for details on SLFTST operation.

FIFO_err: Asserted when the FIFO pointers over run each other causing a sample to be missed. To clear the error, write a '0' to this register bit.

Pattern_err: A digital checkerboard pattern compare function is provided for board level confidence testing and DLL limit checks. If the **Pattern_err_mask** bit via CONFIG3 is cleared, logic is enabled to continuously monitor input FIFO data. Any received data pattern other than 0xAAAA or 0x5555 causes this bit to be set. To clear the error, flush out the previous pattern error by inputting at least 8 samples of the 0xAAAA and/or 0x5555, then write a '0' to this register bit.

Register name: CONFIG5 – Address: 0x05, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIF4	rev_bus	clkdiv_sync _dis	Reserved	Reserved	DLL_bypass	Reserved	Reserved
0	0	0	0	0	0	0	0

SIF4: When set, the serial interface is in 4 pin mode, otherwise it is in 3 pin mode. Refer to **SDO_func_sel (2:0)** bits in CONFIG14 register for options available to output status indicator data on the SDO pin.

rev_bus: Reverses the LVDS input data bus so that the MSB to LSB order is swapped. This function is provided to ease board level layout and avoid wire crossovers in case the LVDS data source output bus is mirrored with respect to the DAC's input data bus.

clkdiv_sync_dis: Disables the clock divider sync when this bit is set.

Reserved (Bit 4): Set to 0 for proper operation.

Reserved (Bit 3): Set to '0' for proper operation.

DLL_bypass: When set, the DLL is bypassed and the LVDS data source is responsible for providing correct setup and hold timing.

Reserved (Bit 1): Set to '0' for proper operation.

Reserved (Bit 0): Set to '0' for proper operation.

Register name: CONFIG6 – Address: 0x06, Default = 0x0C

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Unused	Reserved	Sleep_A	BiasLPF_A	Reserved	Reserved	DLL_sleep
0	0	0	0	1	1	0	0

Reserved (Bit 7): Set to '0' for porper operation.

Reserved (Bit 5): Set to '0' for proper operation.

Sleep_A: When set, DACA is put into sleep mode.

BiasLPF_A: Enables a 95 kHz low pass filter corner on the DACA current source bias when cleared. If this bit is set, a 472 kHz filter corner is used.

Reserved (Bit 2): Set to '1' for proper operation.

Reserved (Bit 1): Set to '0' for proper operation.

DLL_sleep: When set, the DLL is put into sleep mode.

Register name: CONFIG7 – Address: 0x07, Default = 0xFF

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DACA_gain(3:0)				Reserved			
1	1	1	1	1	1	1	1

DACA_gain(3:0): Scales DACA output current in 16 equal steps.

$$\frac{VEXTIO}{R_{bias}} \times (DACA\_gain + 1)$$

Reserved (3:0): Set to '1111' for proper operation.

Register name: CONFIG8 – Address: 0x08, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					DLL_restart	Reserved	
0	0	0	0	0	0	0	0

Reserved (7:3): Set to ‘00000’ for proper operation.

DLL_restart: This bit is used to restart the DLL. When this bit is set, the internal DLL loop filter is reset to zero volts, and the DLL delay line is held at the center of its bias range. When cleared, the DLL will acquire lock to the DCLK signal. A DLL restart is accomplished by setting this bit with a serial interface write, and then clearing this bit with another serial interface write. Any interruption in the DCLK signal or changes to the DLL programming in the CONFIG10 register must be followed by this DLL restart sequence. Also, when this bit is set, the **DLL_lock** indicator in the STATUS0 register is cleared.

Reserved (1:0): Set to ‘00’ for proper operation

Register name: CONFIG9 – Address: 0x09, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							
0	0	0	0	0	0	0	0

Reserved (7:0): Set to '0x00' for proper operation

Register name: CONFIG10 – Address: 0x0A, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLL_delay(3:0)				DLL_invclk	DLL_ifixed(2:0)		
0	0	0	0	0	0	0	0

DLL_delay(3:0): The DCLKP/N LVDS input data clock has a DLL to automatically skew the clock to LVDS data timing relationship, providing proper setup and hold times. **DLL_delay(3:0)** is used to manually adjust the DLL delay ± from the fixed delay set by **DLL_ifixed(2:0)**. Adjustment amounts are approximate.

DLL_delay(3:0)	Delay Adjust (degrees)
1000	50°
1001	55°
1010	60°
1011	65°
1100	70°
1101	75°
1110	80°
1111	85°
0000	90° (Default)
0001	95°
0010	100°
0011	105°
0100	110°
0101	115°
0110	120°
0111	125°

DLL_invclk: When set, used to invert an internal DLL clock to force convergence to a different solution. This can be used in the case where the DLL delay adjustment has exceeded the limits of its range.

DLL_ifixed(2:0): Adjusts the DLL delay line bias current. Refer to the Electrical Characteristics table. Used in conjunction with the DLL_invclk bit to select appropriate delay range for a given DCLK frequency:
'011' – maximum bias current and minimum delay range
'000' – mid scale bias current
'101' – minimum bias current and maximum delay range
'100' – do not use.

Register name: CONFIG11 – Address: 0x0B, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							
0	0	0	0	0	0	0	0

Reserved (7:0): Set to '0x00' for proper operation.

Register name: CONFIG12 – Address: 0x0C, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Offset_sync	OffsetA(12:8)				
0	0	0	0	0	0	0	0

Reserved (1:0): Set to ‘00’ for proper operation.

Offset_sync: On a change from ‘0’ to ‘1’ the values of the OffsetA(12:0) and OffsetB(12:0) control registers are transferred to the registers used in the DAC-A and DAC-B offset calculations. This double buffering allows complete control by the user as to when the change in the offset value occurs. This bit does not auto-clear. Prior to updating new offset values, it is recommended that the user clear this bit.

OffsetA(12:8): Upper 5 bits of the offset adjustment value for the A data path. (**SYNCED via Offset_sync**)

Register name: CONFIG13 – Address: 0x0D, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OffsetA(7:0)							
0	0	0	0	0	0	0	0

OffsetA(7:0): Lower 8 bits of the offset adjustment value for the A data path. (**SYNCED via Offset_sync**)

Register name: CONFIG14 – Address: 0x0E, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDO_func_sel(2:0)			Reserved				
0	0	0	0	0	0	0	0

SDO_func_sel(2:0): Selects the signal for output on the SDO pin. When using the 3 pin serial interface mode, this allows the user to multiplex several status indicators onto the SDO pin. In 4 pin serial interface mode, programming this register to view one of the 5 available status indicators will override normal SDO serial interface operation.

SDO_func_sel (2:0)	Output to SDO
000, 110, 111	Normal SDO function
001	Not defined
010	DLL_lock
011	Pattern_err
100	FIFO_err
101	SLFTST_err

Reserved (4:0): Set to '00000' for proper operation.

Register name: CONFIG15 – Address: 0x0F, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							
0	0	0	0	0	0	0	0

Reserved (7:0): Set to '0x00' for proper operation.

SERIAL INTERFACE

The serial port of the DAC5681 is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC5681. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 pin interface by **SIF4** in register **CONFIG5**. In both configurations, **SCLK** is the serial interface input clock and **SDENB** is serial interface enable. For 3 pin configuration, **SDIO** is a bidirectional pin for both data in and data out. For 4 pin configuration, **SDIO** is data in only and **SDO** is data out only. Data is input into the device with the rising edge of **SCLK**.Data is output from the device on the falling edge of **SCLK**.

Each read/write operation is framed by signal **SDENB** (Serial Data Enable Bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write, how many bytes to transfer, and what address to transfer the data. Table 2 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 to 5 comprise the data transfer cycle.

Table 2. Instruction Byte of the Serial Interface

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W	N1	N0	A4	A3	A2	A1	A0

R/W Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC5681 and a low indicates a write operation to DAC5681.

[N1 : N0] Identifies the number of data bytes to be transferred per Table 5 below. Data is transferred MSB first.

Table 3. Number of Transferred Bytes Within One Communication Frame

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

[A4 : A0] Identifies the address of the register to be accessed during the read or write operation. For multi-byte transfers, this address is the starting address. Note that the address is written to the DAC5681 MSB first and counts down for each byte.

Figure 18 shows the serial interface timing diagram for a DAC5681 write operation. **SCLK** is the serial interface clock input to DAC5681. Serial data enable **SDENB** is an active low input to DAC5681. **SDIO** is serial data in. Input data to DAC5681 is clocked on the rising edges of **SCLK**.

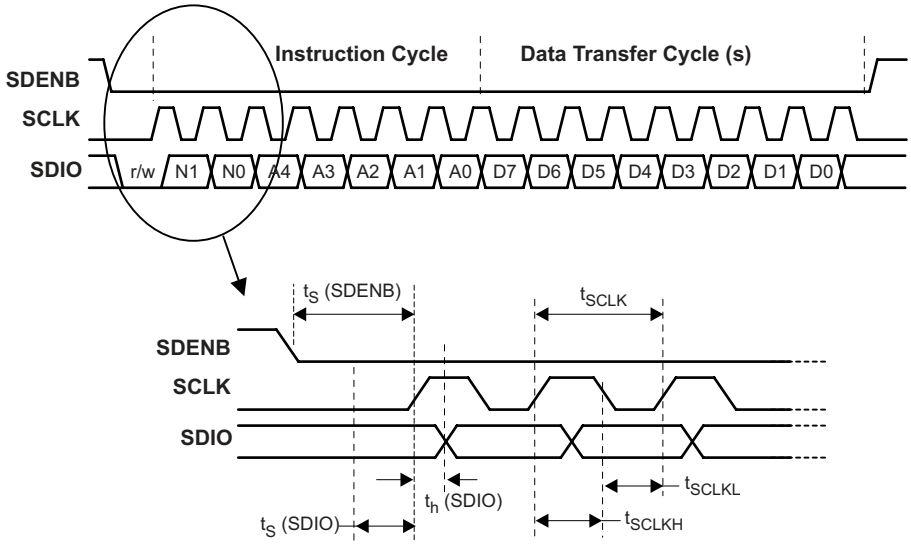


Figure 18. Serial Interface Write Timing Diagram

Figure 19 shows the serial interface timing diagram for a DAC5681 read operation. **SCLK** is the serial interface clock input to DAC5681. Serial data enable **SDENB** is an active low input to DAC5681. **SDIO** is serial data in during the instruction cycle. In 3 pin configuration, **SDIO** is data out from DAC5681 during the data transfer cycle(s), while **SDO** is in a high-impedance state. In 4 pin configuration, **SDO** is data out from DAC5681 during the data transfer cycle(s). At the end of the data transfer, SDO will output low on the final falling edge of SCLK until the rising edge of SDENB when it will 3-state.

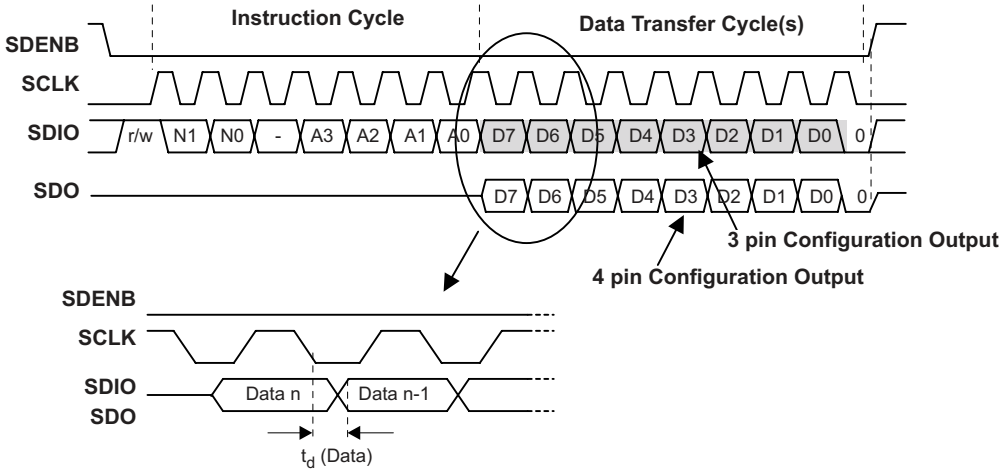


Figure 19. Serial Interface Read Timing Diagram

CLOCK AND DATA MODES

The timing diagram for the DAC5681 is shown in Figure 20. The DAC5681 accepts an external full-rate clock input on the CLKIN/CLKINC pins to drive the DAC and final logic stages. An LVDS half-rate data clock (DCLKP/DCLKN) is provided by the user and is typically generated by a *toggling data bit* to maintain LVDS data to DCLK timing alignment. LVDS data relative to DCLK is input using Double Data Rate (DDR) switching using both rising and falling edges as shown in the both figures below. The CONFIG10 register contains user controlled settings for the DLL to adjust for the DCLK input frequency and various $\mathbf{t_{SKEW}}$ timing offsets between the LVDS data and DCLK. The CDCM7005 and CDCE62005 from Texas Instruments are recommended for providing phase aligned clocks at different frequencies for device-to-device clock distribution and multiple DAC synchronization.

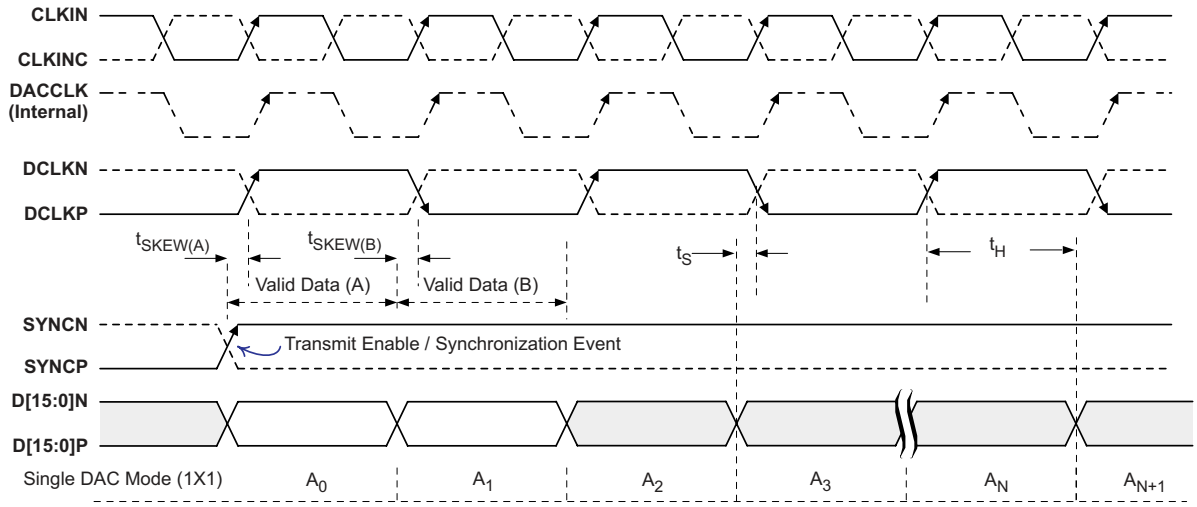


Figure 20. Clock and Data Timing Diagram

CLOCK INPUTS

Figure 21 shows an equivalent circuit for the LVDS data input clock (DCLKP/N).

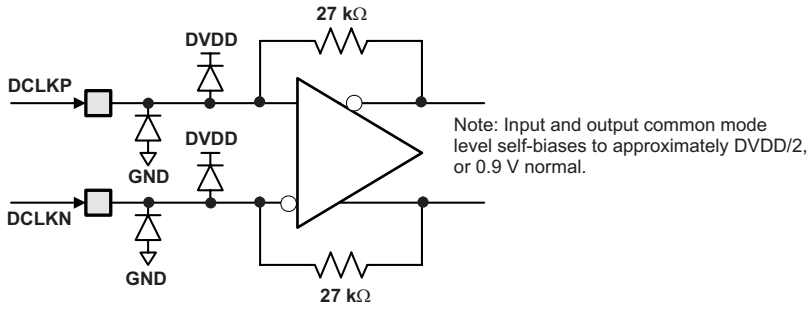


Figure 21. DCLKP/N Equivalent Input Circuit

Figure 22 shows an equivalent circuit for the DAC input clock (CLKIN/C).

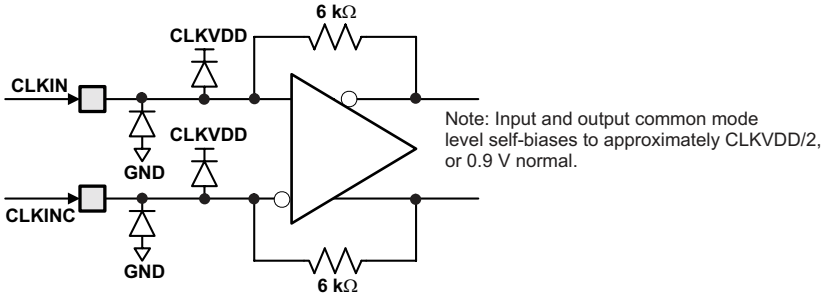


Figure 22. CLKIN/C Equivalent Input Circuit

Figure 23 shows the preferred configuration for driving the CLKIN/CLKINC input clock with a differential ECL/PECL source.

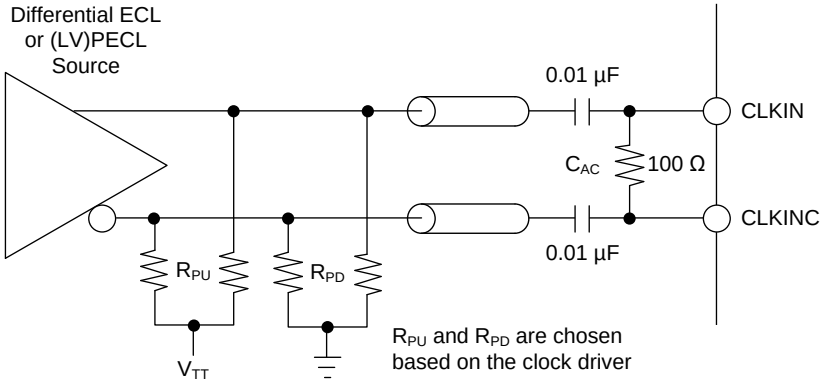


Figure 23. Preferred Clock Input Configuration With a Differential ECL/PECL Clock Source

LVDS DATA INTERFACING

Interfacing very high-speed LVDS data and clocks presents a big challenge to system designers as they have unique constraints and are often implemented with specialized circuits to increase bandwidth. One such specialized LVDS circuit used in many FPGAs and ASICs is a SERializer-DESerializer (SERDES) block. For interfacing to the DAC5681, only the SERializer functionality of the SERDES block is required. SERDES drivers accept lower rate parallel input data and output a serial stream using a shift register at a frequency multiple of the data bit width. For example, a 4-bit SERDES block can accept parallel 4-bit input data at 250 MSPS and output serial data 1000 MSPS.

External clock distribution for FPGA and ASIC SERDES drivers often have a chip-to-chip system constraint of a limited input clock frequency compared to the desired LVDS data rate. In this case, an internal clock multiplying PLL is often used in the FPGA or ASIC to drive the high-rate SERDES outputs. Due to this possible system clocking constraint, the DAC5681 accommodates a scheme where a toggling LVDS SERDES data bit can provide a “data driven” half-rate clock (DCLK) from the data source. A DLL on-board the DAC is used to shift the DCLK edges relative to LVDS data to maintain internal setup and hold timing.

To increase bandwidth of a single 16-bit input bus, the DAC5681 assumes Double Data Rate (DDR) style interfacing of data relative to the half-rate DCLK. Refer to Figure 24 and Figure 25 providing an example implementation using FPGA-based LVDS data and clock interfaces to drive the DAC5681. In this example, an assumed system constraint is that the FPGA can only receive a 250 MHz maximum input clock while the desired DAC clock is 1000 MHz. A clock distribution chip such as the CDCM7005 or the CDCE62005 is useful in this case to provide frequency and phase locked clocks at 250 MHz and 1000 MHz.

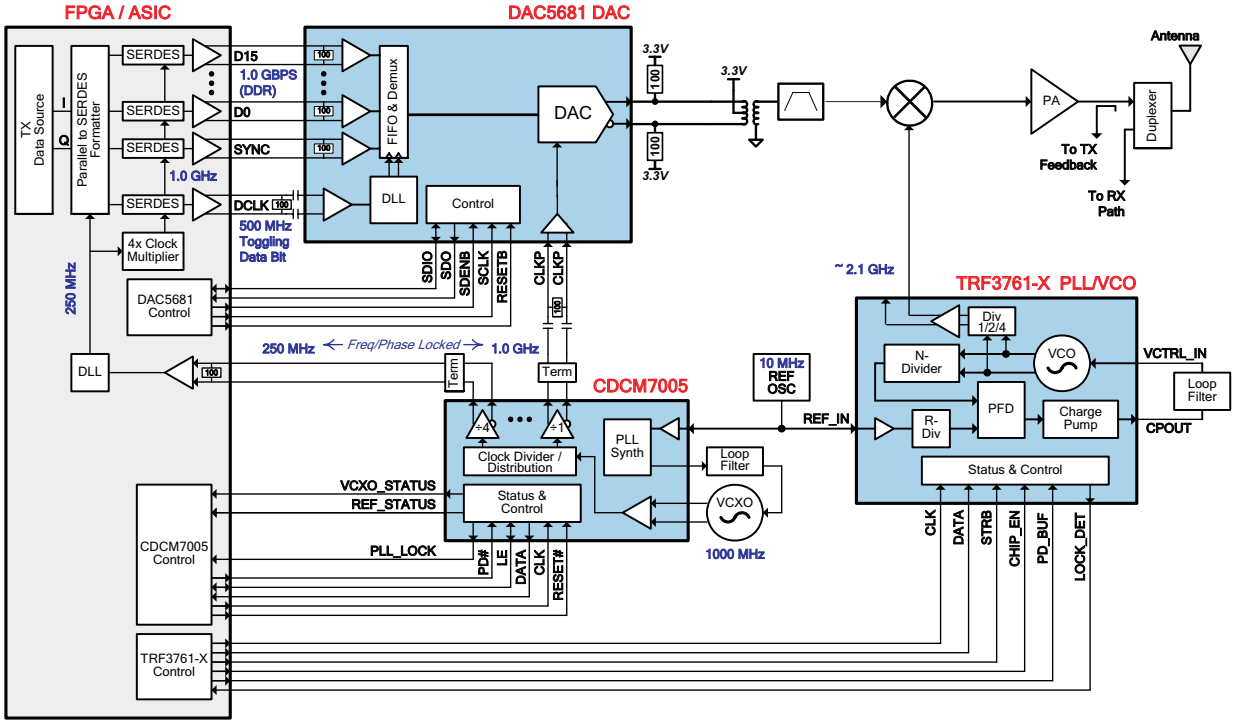


Figure 24. Example Direct Conversion System Diagram

From the example provided by Figure 25, driving LVDS data into the DAC using SERDES blocks requires a parallel load of 4 consecutive data samples to shift registers. Color is used in the figure to indicate how data and clocks flow from the FPGA to the DAC5681. The figure also shows the use of the SYNCP/N input, which along with DCLK, requires 18 individual SERDES data blocks to drive the DAC’s input data FIFO that provides an elastic buffer to the DAC5681 digital processing chain.

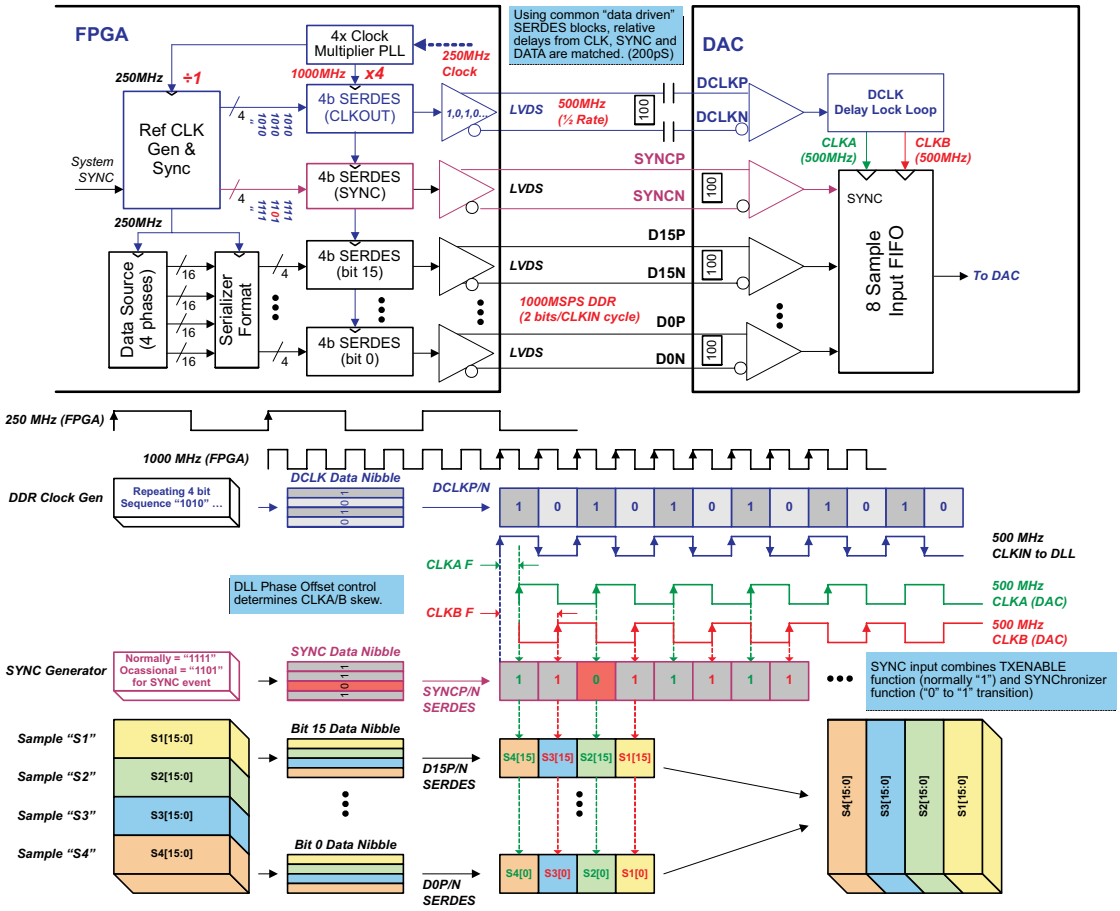


Figure 25. Example FPGA-Based LVDS Data Flow to DAC

LVDS INPUTS

The D[15:0]P/N and SYNCP/N LVDS pairs have the input configuration shown in Figure 26. Figure 27 shows the typical input levels and common-mode voltage used to drive these inputs.

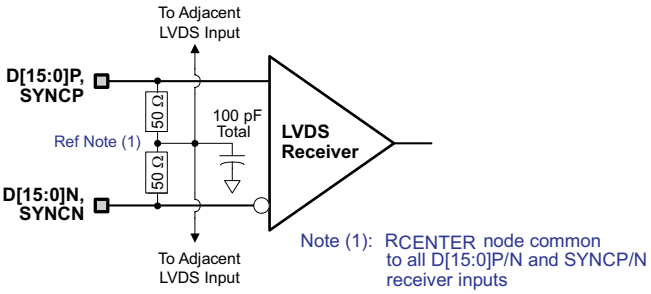


Figure 26. D[15:0]P/N and SYNCP/N LVDS Input Configuration

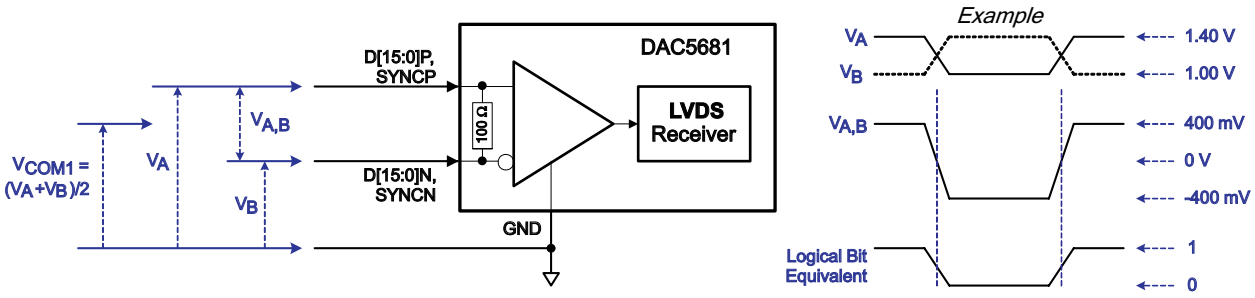


Figure 27. LVDS Data (D[15:0]P/N, SYNCP/N Pairs) Input Levels

Table 4. Example LVDS Data Input Levels

APPLIED VOLTAGES		RESULTING DEFERENTIAL VOLTAGE	RESULTING COMMON-MODE VOLTAGE	LOGICAL BIT BINARY EQUIVALENT
V_A	V_B	$V_{A,B}$	V_{COM1}	
1.4 V	1.0 V	400 mV	1.2 V	1
1.0 V	1.4 V	–400 mV		0
1.2 V	0.8 V	400 mV	1.0 V	1
0.8 V	1.2 V	–400 mV		0

Figure 28 shows the DCLKP/N LVDS clock input levels. Unlike the D[15:0]P/N and SYNCP/N LVDS pairs, the DCLKP/N pair does not have an internal resistor and the common-mode voltage is self-biased to approximately DVDD/2 in order to optimize the operation of the DLL circuit. For proper external termination a 100 Ω resistor needs to be connected across the LVDS clock source lines followed by series 0.01 µF capacitors connected to each of the DCLKP and DCLKN pins. For best performance, the resistor and capacitors should be placed as close as possible to these pins.

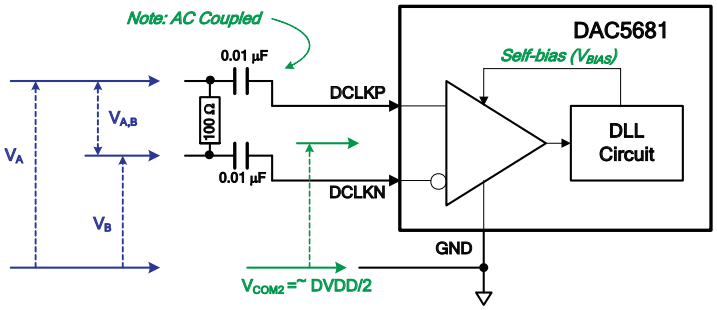


Figure 28. LVDS Clock (DCLKP/N) Input Levels

LVDS SYNCP/N Operation

The SYNCP/N LVDS input control functions as a combination of Transmit Enable (TXENABLE) and Synchronization trigger. If SYNCP is low, the transmit chain is disabled so input data from the FIFO is ignored while zeros are inserted into the data path. If SYNCP is raised from low to high, a synchronization event occurs with behavior defined by individual control bits in registers CONFIG1 and CONFIG5. The SYNCP/N control is sampled and input into the FIFO along with the other LVDS data to maintain timing alignment with the data bus. See Figure 25.

The **software_sync_sel** and **software_sync** controls in CONFIG3 provide a substitute for external SYNCP/N control; however, since the serial interface is used no timing control is provided with respect to the DAC clock.

DLL OPERATION

The DAC5681 provides a digital Delay Lock Loop (DLL) to skew the LVDS data clock (DCLK) relative to the data bits, D[15:0] and SYNC, in order to maintain proper setup and hold timing. Since the DLL operates closed-loop, it requires a stable DCLK to maintain delay lock. Refer to the description of **DLL_ifixed(2:0)** and **DLL_delay(3:0)** control bits in the CONFIG10 register. Prior to initializing the DLL, the **DLL_ifixed** value should be programmed to match the expected DCLK frequency range. To initialize the DLL, refer to the **DLL_Restart** programming bit in the CONFIG8 register. After initialization, the status of the DLL can be verified by reading the **DLL_Lock** bit from STATUS0. See *Startup Sequence* below.

RECOMMENDED STARTUP SEQUENCE

The following startup sequence is recommended to initialize the DAC5681:

1. Supply all 1.8V (CLKVDD, DVDD, VFUSE) voltages simultaneously followed by all 3.3V (AVDD and IOVDD) voltages.
2. Provide stable CLKIN/C clock.
3. Toggle RESETB pin for a minimum 25 nSec active low pulse width.
4. Program all desired SIF registers. Set **DLL_Restart** bit during this write cycle. The CONFIG10 register value should match the corresponding DCLKP/N frequency range in the Electrical Characteristics table.
5. Provide stable DCLKP/N clock. (This can also be provided earlier in the sequence)
6. Clear the **DLL_Restart** bit when the DCLKP/N clock is expected to be stable.
7. Verify the status of **DLL_Lock** and repeat until set to '1'. **DLL_Lock** can be monitored by reading the STATUS0 register or by monitoring the SDO pin in 3-wire SIF mode. (See description for CONFIG14 **SDO_func_sel**.)
8. Enable transmit of data by asserting the LVDS SYNCP/N input or setting CONFIG3 **SW_sync** bit. (See description for CONFIG3 **SW_sync** and **SW_sync_sel**) The SYNC source must be held at a logic '1' to enable data flow through the DAC. If multiple DAC devices require synchronization, refer to the "Recommended Multi-DAC Synchronization Procedure" below.
9. Provide data flow to LVDS D[15:0]P/N pins. If using the LVDS SYNCP/N input, data can be input simultaneous with the logic '1' transition of SYNCP/N.

RECOMMENDED MULTI-DAC SYNCHRONIZATION PROCEDURE

The DAC5681 provides a mechanism to synchronize multiple DAC devices in a system. The procedure has two steps involving control of the CONFIG5 **clkdiv_sync_dis** as well as external control of the LVDS SYNCP/N input. (All DACs involved need to be configured to accept the external SYNCP/N input and not "software" sync mode).

1. Synchronize Clock Dividers (for each DAC):
   (a) Set CONFIG5 **clkdiv_sync_dis** = 0.
   (b) Toggle SYNCP/N input to all DACs simultaneously (same input to all DACs).
2. Synchronize FIFO pointers (for each DAC):
   (a) Set CONFIG5 **clkdiv_sync_dis** = 1 (Disable clock divider re-sync).
   (b) Wait a minimum of 50 CLKIN cycles from previous SYNCP/N toggle. In practice, the time required to write the above register value will typically occupy more than 50 cycles.
   (c) Assert SYNCP/N input and hold at '1' to all DACs simultaneously. Holding this at '1' is effectively the TXENABLE for the chip so data will be output on the analog pins.
3. After the normal pipeline delay of the device, the outputs of all DACs will be synchronized to within ±1 DAC clock cycle.

CMOS DIGITAL INPUTS

Figure 29 shows a schematic of the equivalent CMOS digital inputs of the DAC5681. SDIO and SCLK have pull-down resistors while RESETB and SDENB have pull-up resistors internal the DAC5681. See the specification table for logic thresholds. The pull-up and pull-down circuitry is approximately equivalent to 100kΩ.

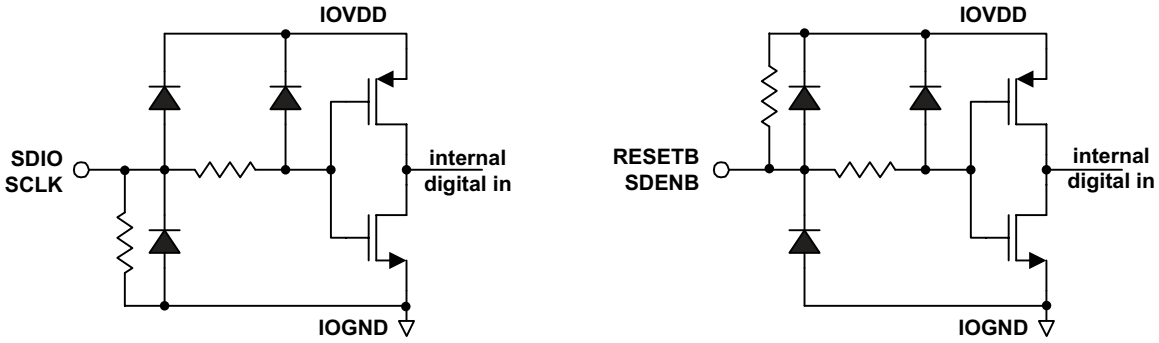


Figure 29. CMOS/TTL Digital Equivalent Input

DIGITAL SELF TEST MODE

The DAC5681 has a Digital Self Test (SLFTST) mode to designed to enable board level testing without requiring specific input data test patterns. The SLFTST mode is enabled via the CONFIG1 **SLFTST_ena** bit and results are only valid when CONFIG3 **SLFTST_err_mask** bit is cleared. An internal Linear Feedback Shift Register (LFSR) is used to generate the input test patterns for the full test cycle while a checksum result is computed on the digital signal chain outputs. The LVDS input data bus is ignored in SLFTST mode. After the test cycle completes, if the checksum result does not match a hardwired comparison value, the STATUS4 **SLFTST_err** bit is set and will remain set until cleared by writing a '0' to the **SLFTST_err** bit. A full self test cycle requires no more than 400,000 CLKIN/C clock cycles to complete and will automatically repeat until the **SLFTEST_ena** bit is cleared.

To initiate the Digital Self Test:

1. Provide a normal CLKIN/C input clock.
2. Provide a RESETB pulse to perform a hardware reset on device.
3. Program the registers with the values shown in Table 5. These register values contain the settings to properly configure the SLFTST including **SLFTST_ena** and **SLFTST_err_mask** bits
4. Provide a '1' on the SYNCP/N input to initiate TXENABLE.
5. Wait at a minimum of 400,000 CLKIN/C cycles for the SLFTST to complete. Example: If CLKIN = 1GHz, then the wait period is 400,000 × 1 / 1GHz = 400 µSec.
6. Read STATUS4 **SLFTST_err** bit. If set, a self test error has occurred. The **SLFTST_err** status may optionally be programmed to output on the SDO pin if using the 3-bit SIF interface. See Table 5 Note (1).
7. (Optional) The SLFTST function automatically repeats until **SLFTST_ena** bit is cleared. To loop the test, write a '0' to STATUS4 **SLFTST_err** to clear previous errors and continue at step 5 above.
8. To continue normal operating mode, provide another RESETB pulse and reprogram registers to the desired normal settings.

Table 5. Digital Self Test (SLFTST) Register Values

REGISTER	ADDRESS (hex)	VALUE (Binary)	VALUE (Hex)
CONFIG1	01	00011000	18
CONFIG2	02	11101010	EA
CONFIG3	03	10110000	B0
STATUS4	04	00000000	00
CONFIG5	05	00000110	06
CONFIG6	06	00001111	0F
CONFIG12	0C	00001010	0A
CONFIG13	0D	01010101	55
CONFIG14(1)	0E	00001010	0A
CONFIG15	0F	10101010	AA
All others	–	Default	Default

(1) If using a 3-bit SIF interface, the SDO pin can be programmed to report **SLFTST_err** status via the **SDO_fun_sel(2:0)** bits. In this case, set CONFIG14 = '10101010' or AA hex.

REFERENCE OPERATION

The DAC5681 uses a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The default full-scale output current equals 16 times this bias current and can thus be expressed as:

$$IOUT_{FS} = 16 \times I_{BIAS} = 16 \times V_{EXTIO} / R_{BIAS}$$

The DAC has a 4-bit coarse gain control via DACA_gain(3:0) in the CONFIG7 register so the $IOUT_{FS}$ can expressed as:

$$IOUTA_{FS} = (DACA\_gain + 1) \times I_{BIAS} = (DACA\_gain + 1) \times V_{EXTIO} / R_{BIAS}$$

where V_{EXTIO} is the voltage at terminal EXTIO. The bandgap reference voltage delivers an accurate voltage of 1.2 V. This reference is active when terminal EXTLO is connected to AGND. An external decoupling capacitor C_{EXT} of 0.1 µF should be connected externally to terminal EXTIO for compensation. The bandgap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the bandgap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by connecting EXTLO to AVDD. Capacitor CEXT may hence be omitted. Terminal EXTIO thus serves as either input or output node.

The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor R_{BIAS} or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 dB.

DAC TRANSFER FUNCTION

The CMOS DAC's consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20 mA. Differential current switches direct the current to either one of the complementary output nodes IOUT1 or IOUT2. Complementary output currents enable differential operation, thus canceling out common mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, even order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip bandgap voltage reference source (+1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a maximum full-scale output current equal to 16 times I_{BIAS}.

The relation between IOUT1 and IOUT2 can be expressed as:

$$IOUT1 = – IOUT_{FS} – IOUT2$$

We will denote current flowing into a node as – current and current flowing out of a node as + current. Since the output stage is a current sink the current can only flow from AVDD into the IOUT1 and IOUT2 pins. The output current flow in each pin driving a resistive load can be expressed as:

$$IOUT1 = IOUT_{FS} \times (65536 – CODE) / 65536$$

$$IOUT2 = IOUT_{FS} \times CODE / 65536$$

where CODE is the decimal representation of the DAC data input word.

For the case where IOUT1 and IOUT2 drive resistor loads R_L directly, this translates into single ended voltages at IOUT1 and IOUT2:

$$VOUT1 = AVDD – | IOUT1 | \times R_L$$

$$VOUT2 = AVDD – | IOUT2 | \times R_L$$

Assuming that the data is full scale (65536 in offset binary notation) and the R_L is 25 Ω, the differential voltage between pins IOUT1 and IOUT2 can be expressed as:

$$VOUT1 = AVDD – | –0 \text{ mA} | \times 25\ \Omega = 3.3 \text{ V}$$

$$VOUT2 = AVDD – | –20 \text{ mA} | \times 25\ \Omega = 2.8 \text{ V}$$

$$VDIFF = VOUT1 – VOUT2 = 0.5 \text{ V}$$

Note that care should be taken not to exceed the compliance voltages at node IOUT1 and IOUT2, which would lead to increased signal distortion.

DAC OUTPUT SINC RESPONSE

Due to the sampled nature of a high-speed DAC, the well known sin(x)/x (or SINC) response can significantly attenuate higher frequency output signals. Figure 30 shows the unitized SINC attenuation roll-off with respect to the final DAC sample rate in 4 Nyquist zones. For example, if the final DAC sample rate F_S = 1.0 GSPS, then a tone at 440MHz is attenuated by 3.0dB. Although the SINC response can create challenges in frequency planning, one side benefit is the natural attenuation of Nyquist images.

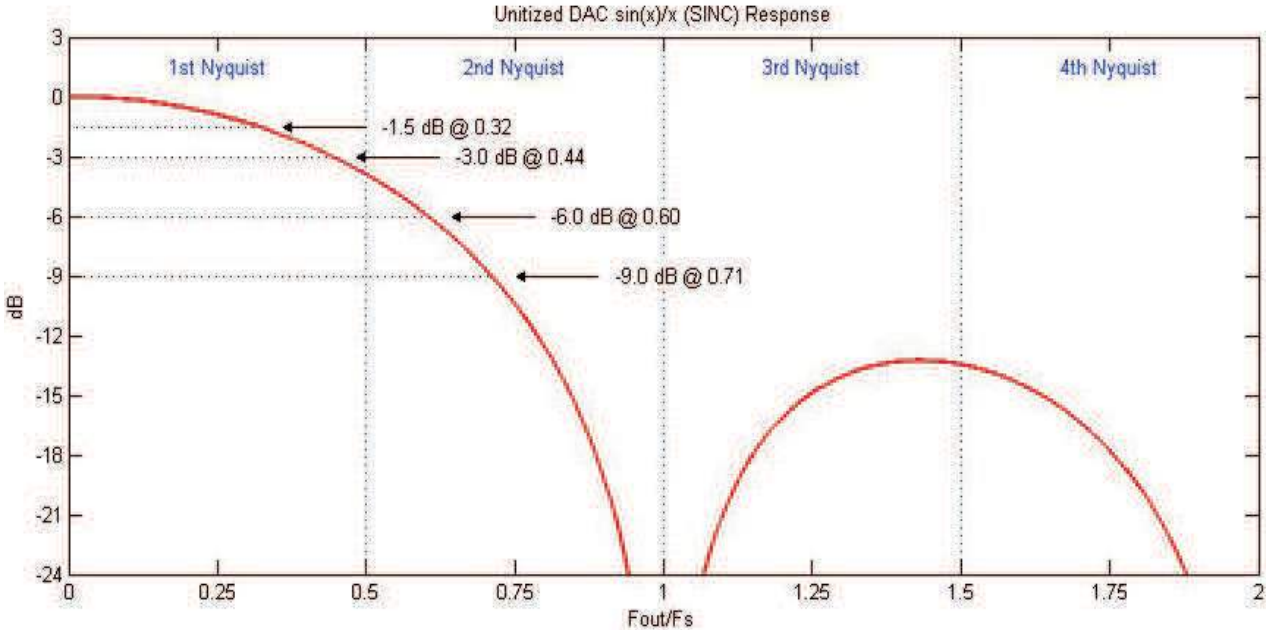


Figure 30. Unitized DAC sin(x)/x (SINC) Response

ANALOG CURRENT OUTPUTS

Figure 31 shows a simplified schematic of the current source array output with corresponding switches in a current sink configuration. Differential switches direct the current into either the positive output node, IOUT1, or its complement, IOUT2, then through the individual NMOS current sources. The output impedance is determined by the stack of the current sources and differential switches, and is typically >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referenced to an external ground. The minimum output compliance at nodes IOUT1 and IOUT2 is limited to AVDD – 0.5 V, determined by the CMOS process. Beyond this value, transistor breakdown may occur resulting in reduced reliability of the DAC5681 device. The maximum output compliance voltage at nodes IOUT1 and IOUT2 equals AVDD + 0.5 V. Exceeding the minimum output compliance voltage adversely affects distortion performance and integral non-linearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 does not exceed 0.5 V.

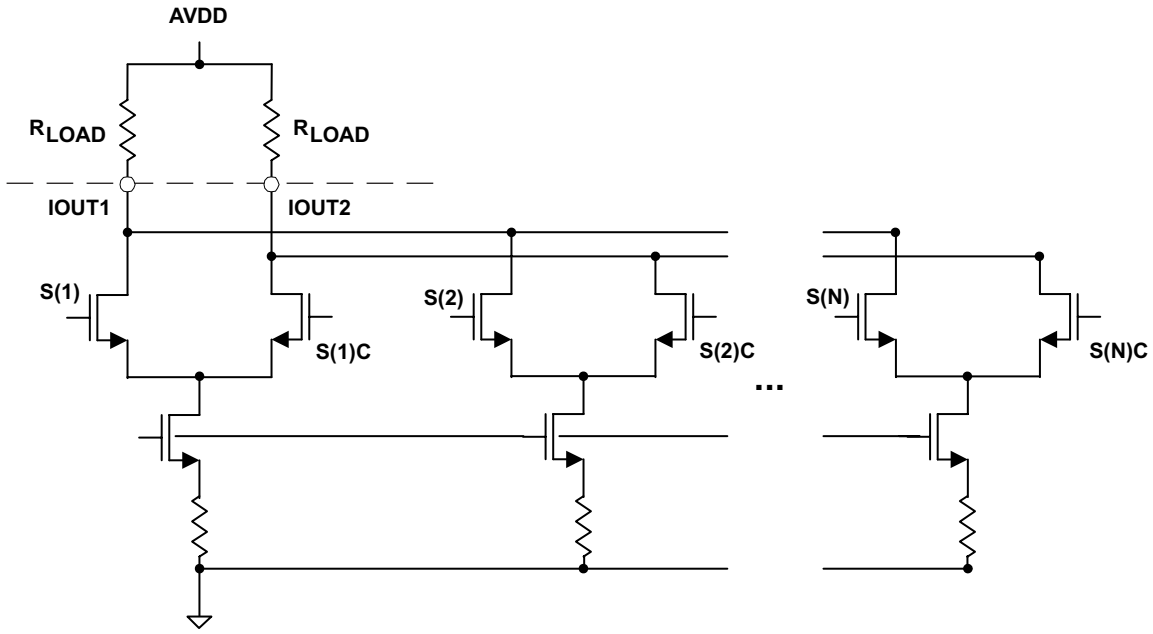


Figure 31. Equivalent Analog Current Output

The DAC5681 can be easily configured to drive a doubly terminated 50Ω cable using a properly selected RF transformer. Figure 32 and Figure 33 show the 50Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratio, respectively. Note that the center tap of the primary input of the transformer has to be connected to AVDD to enable a dc current flow. Applying a 20 mA full-scale output current would lead to a 0.5 V_{PP} for a 1:1 transformer, and a 1 V_{PP} output for a 4:1 transformer. The low dc-impedance between IOUT1 or IOUT2 and the transformer center tap sets the center of the ac-signal at AVDD, so the 1 V_{PP} output for the 4:1 transformer results in an output between AVDD + 0.5 V and AVDD – 0.5 V.

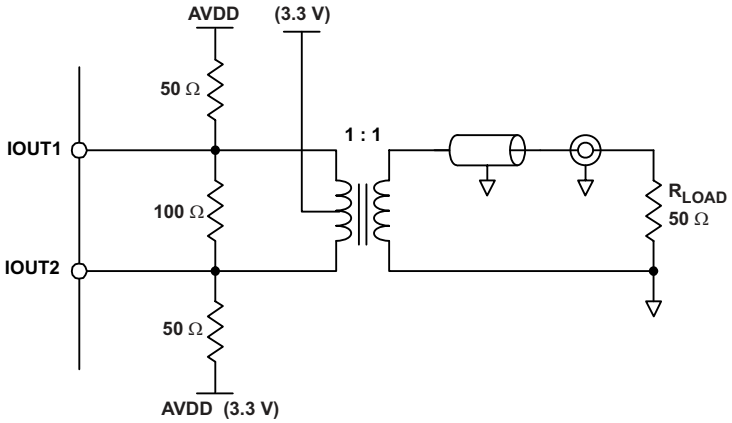


Figure 32. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

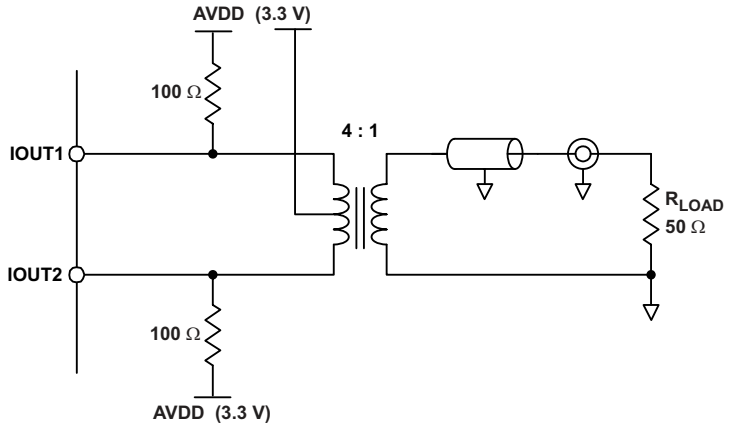


Figure 33. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

APPLICATIONS EXAMPLES

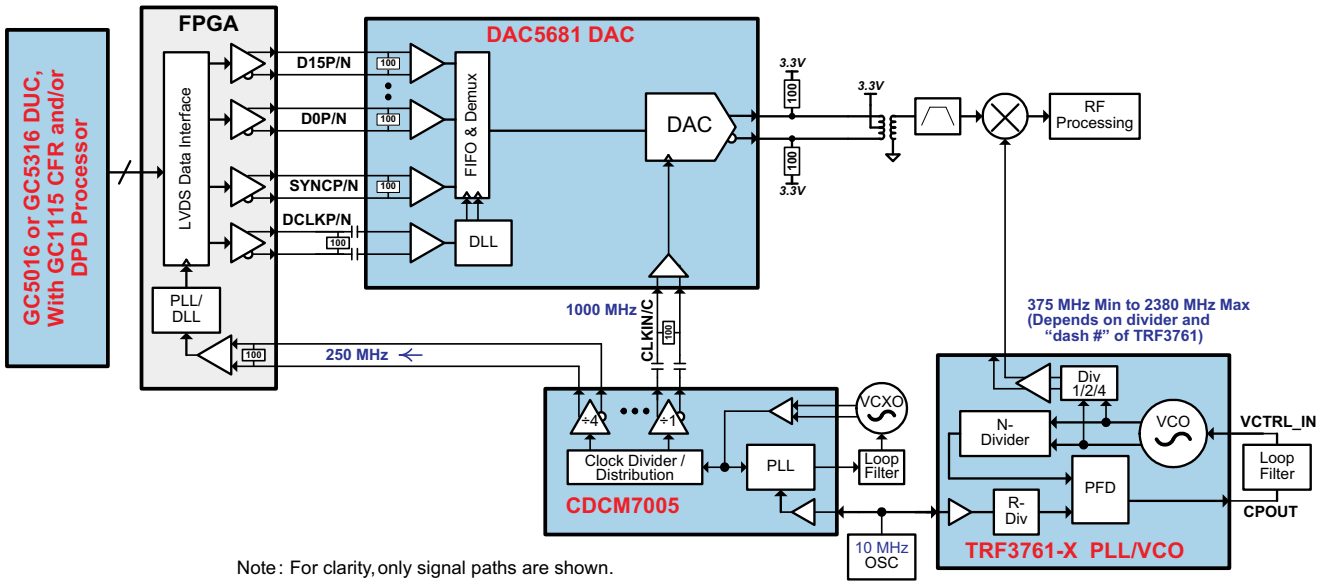
DIGITAL INTERFACE AND CLOCKING CONSIDERATIONS FOR APPLICATION EXAMPLES

The DAC5681's LVDS digital input bus can be driven by an FPGA or digital ASIC. This input signal can be generated directly by the FPGA, or fed by a Texas Instruments Digital Up Converter (DUC) such as the GC5016 or GC5316. Optionally, a GC1115 Crest Factor Reduction (CFR) or Digital Pre-Distortion (DPD) processor may be inserted in the digital signal chain for improving the efficiency of high-power RF amplifiers. For the details on the DAC's high-rate digital interface, refer to the *LVDS Data Interfacing* section.

A low phase noise clock for the DAC at the final sample rate can be generated by a VCXO and a Clock Synchronizer/PLL such as the Texas Instruments CDCM7005 or CDCE62005, which can also provide other system clocks.

DIGITAL IF OUTPUT RADIO

Refer to Figure 34 for an example Digital IF Output Radio. The high data rate of the DAC5681 (up to 1.0GSPS) allows for extremely wide bandwidth signals. The DAC output signal would typically be terminated with a transformer (see the Analog Current Outputs section). An IF filter, either LC or SAW, is used to suppress the DAC Nyquist zone images and other spurious signals before being mixed to RF with a mixer. The TRF3671 Frequency Synthesizer, with integrated VCO, may be used to drive a common LO input of the mixers for frequencies between 375 and 2380 MHz.



Note: For clarity, only signal paths are shown.

Figure 34. System Diagram of a Dual Channel Real IF Output Radio

APPLICATIONS EXAMPLES (continued)

CMTS/VOD TRANSMITTER

The exceptional SNR of the DAC5681 enables a cable modem termination system (CMTS) or video on demand (VOD) QAM transmitter in excess of the stringent DOCSIS specification, with >74 dBc and 75 dBc in the adjacent and alternate channels.

See Figure 34 for an example IF Output Radio – this signal chain is nearly identical to a typical system using the DAC5681 for a cost optimized two QAM transmitter. A GC5016 would accept two separate symbol rate inputs and provide pulse shaping and interpolation to ~ 128 MSPS. The two QAM carriers would be combined into two groups of two QAM carriers with intermediate frequencies of approximately 30 MHz to 40 MHz. The GC5016 would output data to the DAC5681 through an FPGA for CMOS to LVDS translation. The signal is output through a transformer and to an RF upconverter.

HIGH-SPEED ARBITRARY WAVEFORM GENERATOR

The 1GSPS bandwidth input data bus combined with the 16-bit DAC resolution of the DAC5681 allows wideband signal generation for test and measurement applications. The FPGA-based waveform generator can make use of the full Nyquist bandwidth of up to 500MHz.

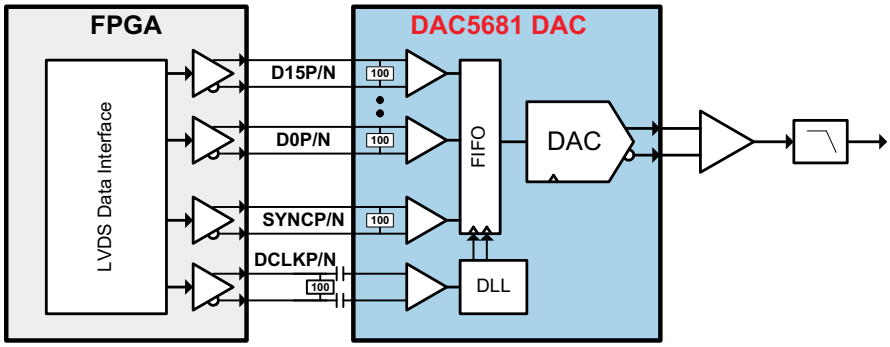


Figure 35. System Diagram of Arbitrary Waveform Generator

REVISION HISTORY

Note: Page numbers of current version may differ from previous versions.

Changes from Original (August 2007) to Revision A **Page**

- Changed $t_{r(IOUT)}$ spec. output rise time 10% to 90% typical value from 2 ns to 220 ps 8
- Changed $t_{f(IOUT)}$ spec. output fall time 10% to 90% typical value from 2 ns to 220 ps 8
- Changed Z_T spec. internal termination from 100 Ω min, 120 Ω max; to 85 Ω min, 135 Ω max 9
- Deleted temperature deratings for f_{DATA} specifications 9
- Added DLL operating frequency range specifications 9
- Changed C_{AC} values from 0.1 to 0.01µF, Figure 23 29

Changes from Revision A (January 2009) to Revision B **Page**

- Changed Table 1 Bit 4 from FIFO_sync_dis to Reserved 18
- Changed Table 1 Bit 7 from Hold_sync _dis to Reserved 18
- Deleted "– unless disabled via **FIFO_sync_dis** in CONFIG5 register" from the Description of CONFIG1 - FIFO_offset(2:0) 19
- Changed "FIFO_sync_dis", to "Reserved" in CONFIG5 table, Bit 4 21
- Changed CONFIG5: FIFO_sync_dis: Description from "....CONFIG1 register" to "Reserved (Bit 4): Set to 0 for poper operation." 21
- Changed CONFIG6, Bit 7 from "Hold_sync _dis" to "Reserved" 22
- Changed CONFIG6 : Hold_sync_dis: Description from "When set.....in CONFIG5." to "Reserved (Bit 7): Set to 0 for proper operation." 22
- Changed LVDS SYNCP/N section text from "....with behavior defined by individual control bits in registers CONFIG1, CONFIG5 and CONFIG6. to "....with behavior defined by individual control bits in registers CONFIG1 and CONFIG5." 32
- Changed text in RECOMMENDED MULTI-DAC SYNCHRONIZATION PROCEDURE section from "The procedure has two steps ..... SYNCP/N input" to "The procedure has two steps involving control of the CONFIG5 **clkdiv_sync_dis** as well as external control of the LVDS SYNCP/N input" 33
- Deleted the sub-step "Set CONFIG5 **FIFO_sync_dis = 0**" in procedural steps for Synchronize Clock Dividers (for each DAC) in RECOMMENDED ....PROCEDURE section. 33
- Deleted the sub-step "Set CONFIG5 **FIFO_sync_dis = 0** (Keep same as step 1)" in procedural steps for Synchronize FIFO pointers (for each DAC) in RECOMMENDED ....PROCEDURE section. 33

Changes from Revision B (April 2011) to Revision C **Page**

- Changed the revision date to C, August 2012 1
- Changed Figure 23 for clarification. 29
- Changed the first paragraph of ANALOG CURRENT OUTPUTS section for clarification. 38

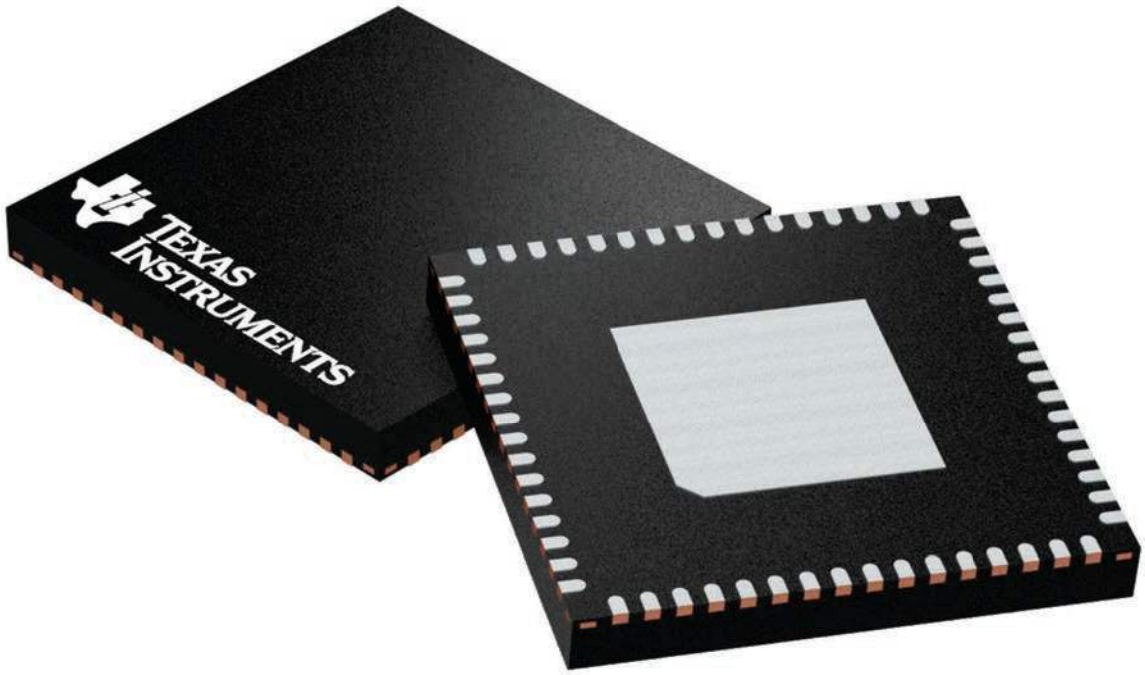
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

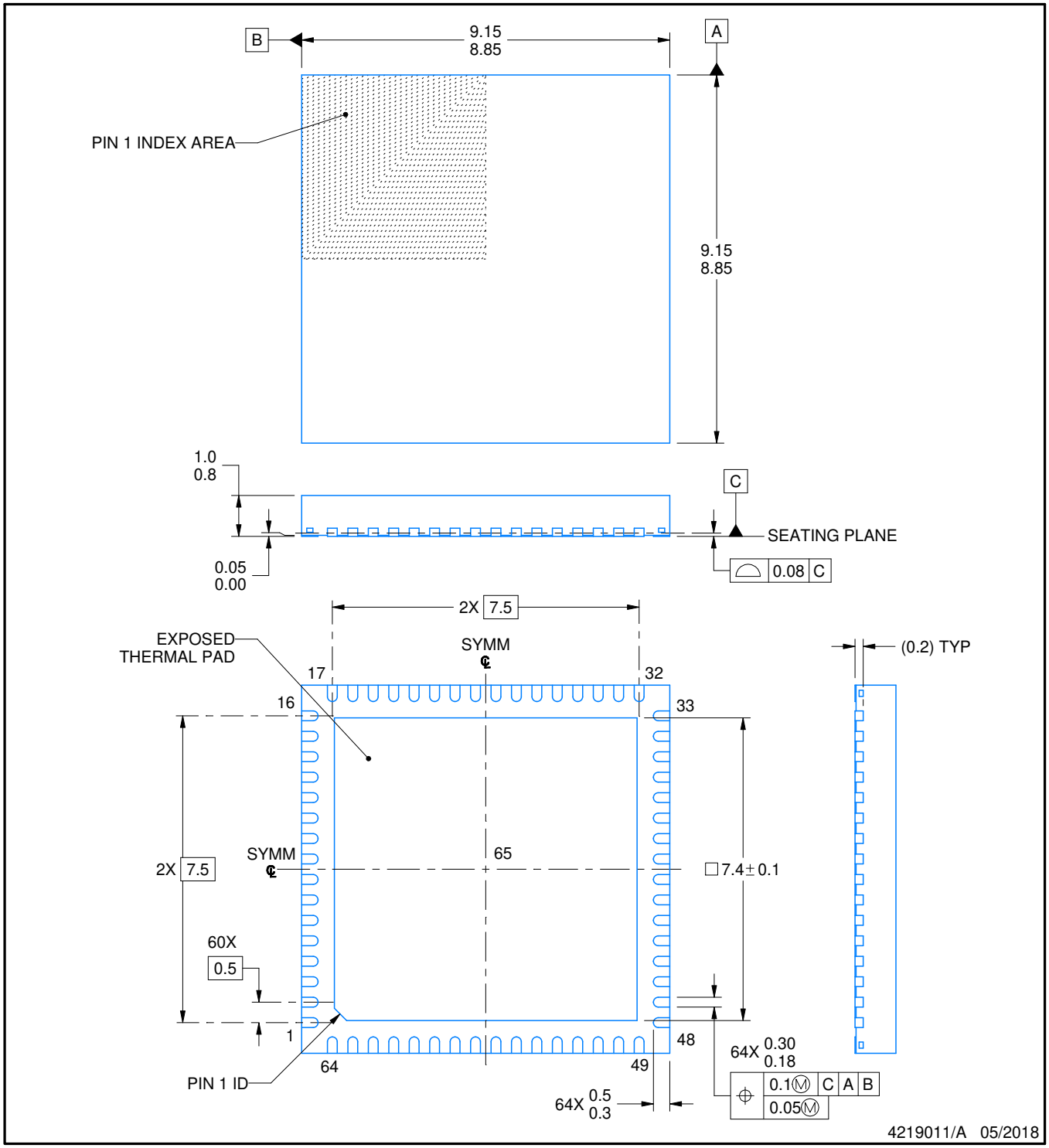
4224597/A

RGC0064H

PACKAGE OUTLINE

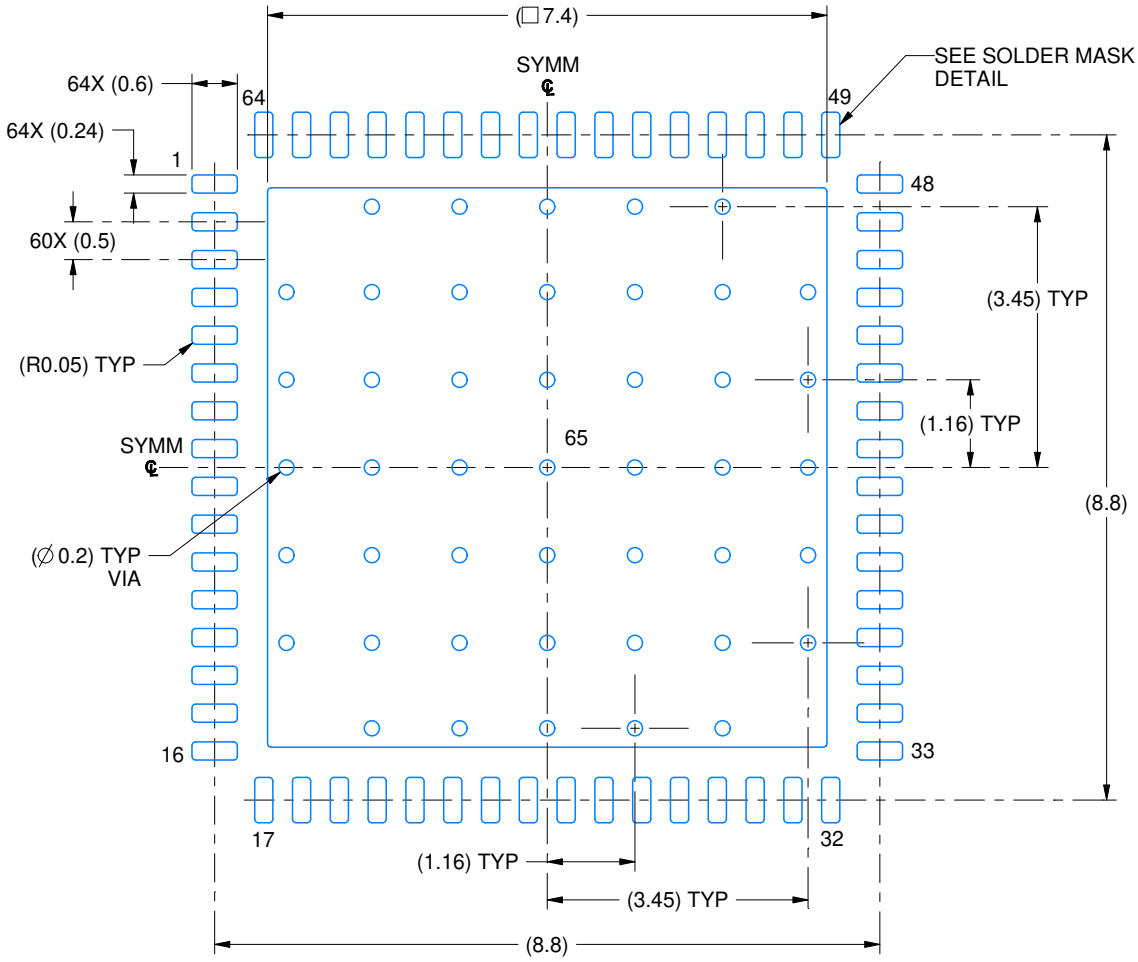
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

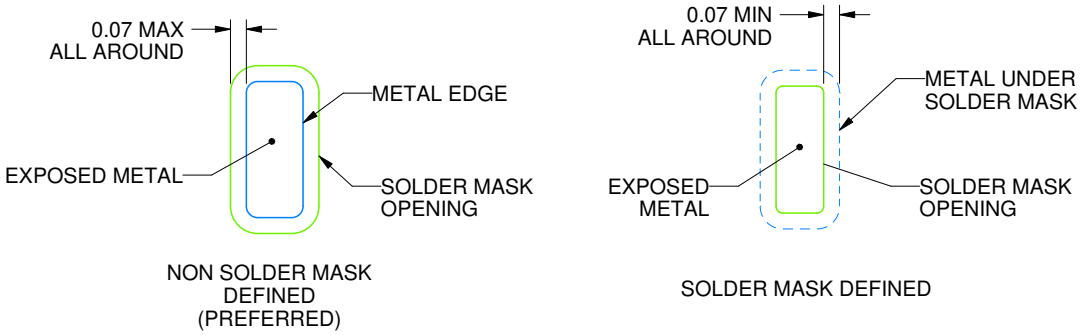


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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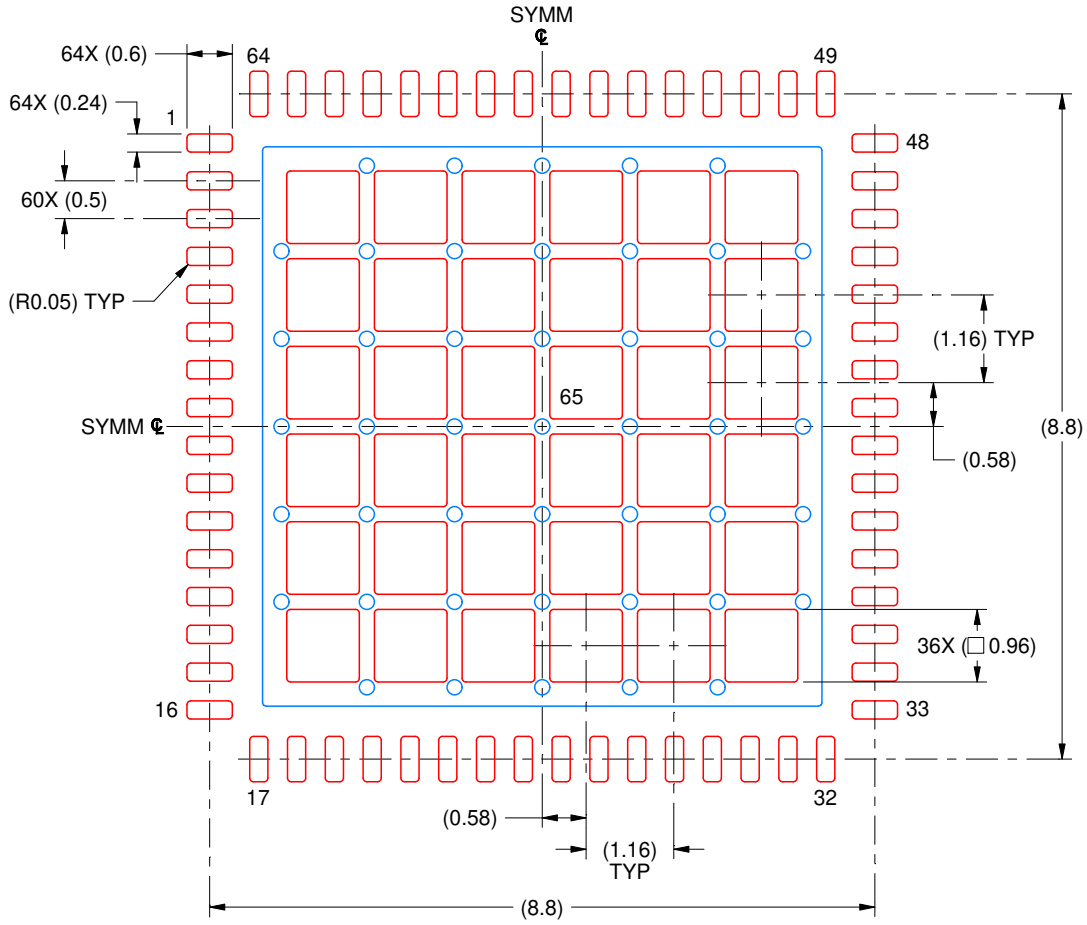
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265