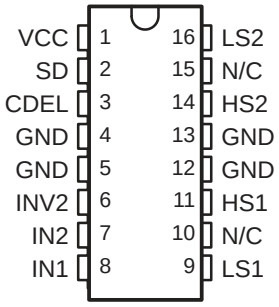
UC27136, UC37136
DUAL OUTPUT SWITCH

SLUS447 - FEBRUARY 2000 - REVISED JULY 2000

- **250-mA Continuous Total Output Drive**
- **Two Output Power Switches, 35-V Maximum Operation**
- **Low-Side or High-Side Switch Configuration**
- **User Programmable Phasing of Output Switch LS2/HS2**
- **Internal Output Voltage Clamp for Driving Inductive Loads**
- **9 V to 35 V Supply Voltage Range**
- **Current Limit Protection**
- **Thermal Shutdown Protection**
- **UVLO With User Programmable Time Delay**

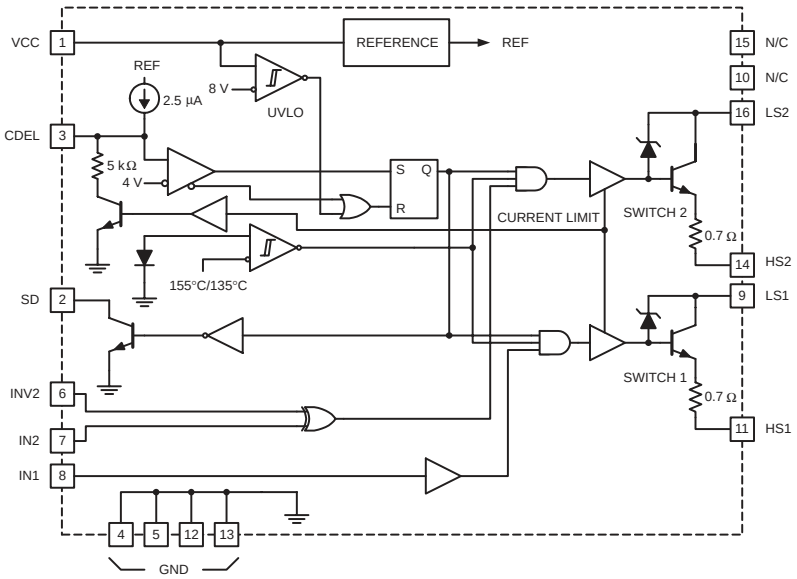
DP, M, OR NP PACKAGES (TOP VIEW)



description

The UCx7136 bipolar dual switch contains all the control and drive circuitry required to drive resistive, capacitive, and inductive loads as in industrial sensor applications. The output drivers are 250-mA NPN power switches that can switch a load between a voltage supply up to 35 V and GND with a continuous output current rating of 250 mA, combined or individually. Internal 46-V Zener clamps are provided to clamp collector-to-emitter NPN power switch voltages to safe levels when driving inductive loads. The two outputs can be configured in any combination of high side (load to GND) or low side (load to VCC). The output of switch 1 is fixed in phase with the CMOS compatible IN1 pin. The CMOS compatible exclusive OR gate inputs, IN2 and INV2, determine the output phase of switch 2. An under voltage lockout (UVLO) function is provided to disable both output NPN power switches until VCC is greater than 8 V. Both output NPN power switches can also be disabled past the UVLO enable trip point by an external user programmable time delay capacitor. An internal current limit function enables a low on/off duty cycle of the NPN power switches should the dc current go beyond 1 A. An internal thermal shutdown function disables the switches if the IC temperature reaches 155°C such as in an overcurrent condition.

schematic



UDG-99016

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply Voltage, VCC . . . . . 35 V
LS1, HS1, LS2, HS2 . . . . . 35 V
LS1-HS1, LS2-HS2 (clamped by internal circuitry) . . . . . 46 V
Output Current, Continuous . . . . . 250 mA (Total)
Output Current, Peak . . . . . 1.3 A
Logic Input Voltage . . . . . 18 V
Storage Temperature, T_J . . . . . –65°C to 150°C
Junction Temperature, T_{stg} . . . . . –55°C to 150°C
Lead Temperature (Soldering, 10 s) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Data Book for thermal limitations and considerations of packages.

AVAILABLE OPTIONS

T_A	PACKAGE DEVICES		
	SOIC Narrow Lead Frame (DP)	Plastic Batwing DIP (NP)	QSOP Lead Frame (M)
–40°C to +85°C	UC27136DP	UC27136NP	N/A
0°C to +70°C	UC37136DP	UC37136NP	UC37136M

electrical characteristics VCC = 25 V, IN1 = IN2 = INV2 = 0 V (for low), IN1 = IN2 = INV2 = 5 V (for high), $T_A = T_J$, CDEL = 10 nF, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall Section					
VCC supply voltage		9		35	V
VCC supply current	VCC current with IN1, IN2, INV2 = 0 V		7.0		mA
Under Voltage Lockout (UVLO) Section					
UVLO threshold		7.5	8	8.5	V
UVLO hysteresis		0.4	0.5	0.6	V
Input Logic Section					
Digital input high level	IN1, IN2, INV2	3.5			V
Digital input low level	IN1, IN2, INV2			1.5	V
Input bias current, low level	IN1, IN2, INV2 = 0 V		–10		µA
Input bias current high level	IN1, IN2, INV2 = 5 V		5		µA
Logic input to output delay				3	µs
Output: High Side Configuration Section					
Rise time (off to on)	R_{LOAD} = 250 Ω, See Figure 1		100		ns
Fall time (on to off)	R_{LOAD} = 250 Ω, See Figure 1		200		ns
Saturation voltage	R_{LOAD} = 100 Ω, T_A = 25°C, See Figure 1			1.15	V
	R_{LOAD} = 100 Ω, T_A = –40°C, See Figure 1			1.3	V
Current limit	R_{LOAD} = 0.25 Ω, T_A = 25°C, See Figure 1		1.1		A
Leakage current	HS1, HS2 = GND, LS1, LS2 = VCC, IN1, IN2, INV2 = 0 V			5	µA
Voltage clamp	Measure ($V_{LS1} – V_{HS1}$) or ($V_{LS2} – V_{HS2}$)		46		V

electrical characteristics VCC = 25 V, IN1 = IN2 = INV2 = 0 V (for low), IN1 = IN2 = INV2 = 5 V (for high), $T_A = T_J$, CDEL = 10 nF, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output: Low Side Configuration Section					
Rise time (on to off)	R_{LOAD} = 250 Ω, See Figure 2		300		ns
Fall Time (off to on)	R_{LOAD} = 250 Ω, See Figure 2		150		ns
Saturation voltage	R_{LOAD} = 100 Ω, T_A = 25°C, See Figure 2			1.15	V
	R_{LOAD} = 100 Ω, T_A = –40°C, See Figure 2			1.3	V
Current limit	R_{LOAD} = 0.25 Ω, T_A = 25°C, See Figure 2		1.1		A
Leakage current	HS1, HS2 = GND, LS1, LS2 = VCC, IN1, IN2, INV2 = 0 V			5	µA
Voltage clamp	Measure (V_{LS1} - V_{HS1}) or (V_{LS2} - V_{HS2})		46		V
Turn On Delay					
CDEL maximum voltage			4.7		V
CDEL threshold			4		V
I_{CDEL}			2.5		µA
Thermal Shutdown (see Note 1)					
Thermal shutdown threshold			155		°C
Hysteresis			20		°C

NOTE 1: Ensured by design. Not production tested.

pin descriptions

CDEL: A capacitor connected to this pin is used to program a turnon delay after the UVLO threshold has been reached. The UVLO function keeps the external capacitor connected to this pin discharged until VCC is greater than 8 V. After the UVLO upper trip point of 8 V has been exceeded, an internal 2.5-µA current source charges the capacitor from GND to 4.7 V. An internal voltage comparator enables the output NPN switches at 4 V, imparting a time delay after UVLO. As an added feature, an external switch can be connected in parallel with the user-programmable time-delay capacitor to disable the output NPN switches and reset the time delay capacitor by external means.

GND: The reference point for the internal reference, all thresholds, and the ground for the remainder of the device.

IN1: The digital-logic input pin that controls the state of the output NPN switch 1. When the IN1 pin is a logic low (0 V to 1.5 V), output switch 1 is off (non-conducting). When the IN1 pin is a logic high (3.5 V to 17.5 V), output switch 1 is on (conducting).

IN2, INV2: The digital logic input pins to the exclusive OR gate that controls the state of the output NPN switch 2. Refer to the truth table for description. A logic low is 0 V to 1.5 V; a logic high is 3.5 V to 17.5 V.

HS1: This pin is the emitter of output NPN switch 1.

HS2: This pin is the emitter of output NPN switch 2.

LS1: This pin is the collector of output NPN switch 1.

LS2: This pin is the collector of output NPN switch 2.

SD: This ground referenced open collector NPN output is asserted in the event of an overcurrent or during the start up delay due to the CDEL pin, non-conducting otherwise. The maximum SD current is 8 mA.

APPLICATION INFORMATION

TRUTHTABLE

INV2	IN2	Switch 2
Low	Low	Off
High	Low	On
Low	High	On
High	High	Off

turn on delay

The NPN output switches remains off until the external capacitor connected to CDEL charges up to the internal threshold voltage of 4 V with a charging current of 2.5 μA. This off condition is independent of the state of the input logic pins IN1, IN2, and INV2. This capacitor charging imparts a delay time on the outputs that is equal to approximately 1.6 ms/nF. As an example, a 0.1-μF capacitor connected to CDEL results in a 160 ms turnon delay after VCC crosses the 8-V UVLO threshold. If VCC drops below the 7.5-V hysteresis threshold, the CDEL capacitor is discharged immediately and both outputs turn off. The CDEL pin can also be externally driven low to restart the turnon delay sequence. The minimum acceptable value for the CDEL capacitor, when driving a capacitive load, is determined by:

$$CDEL_{(MIN)} = \left(\frac{C_{LOAD} \times V_{LOAD}}{2445} \right) \quad (1)$$

Where C_{LOAD} is equal to the output capacitive load and V_{LOAD} is equal to the voltage rail of the output load. The maximum switching frequency to drive a capacitive load, C_{LOAD}, is given by:

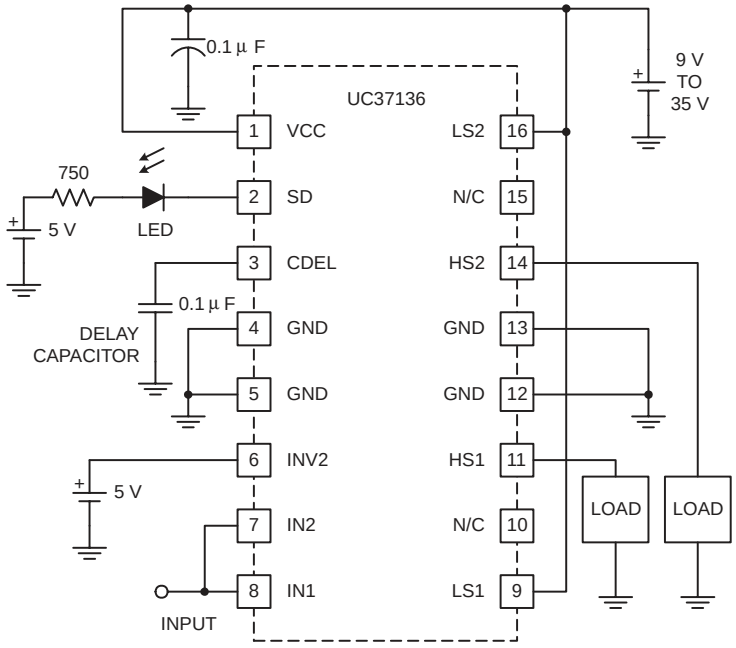
$$f_{(MAX)} = \frac{1}{9.4 \times CDEL \times \left\{ 1 - e^{\left(\frac{-C_{LOAD} \times V_{LOAD}}{5 \times 10^3 \times CDEL} \right)} \right\} + C_{LOAD} \times V_{LOAD}} \quad (2)$$

overcurrent indication

The open collector output SD pin can be used to drive an LED to signal when an overload condition is present. The LED turns on, through an external pullup, when the outputs are shut down due to an overcurrent. The maximum SD current is 8 mA.

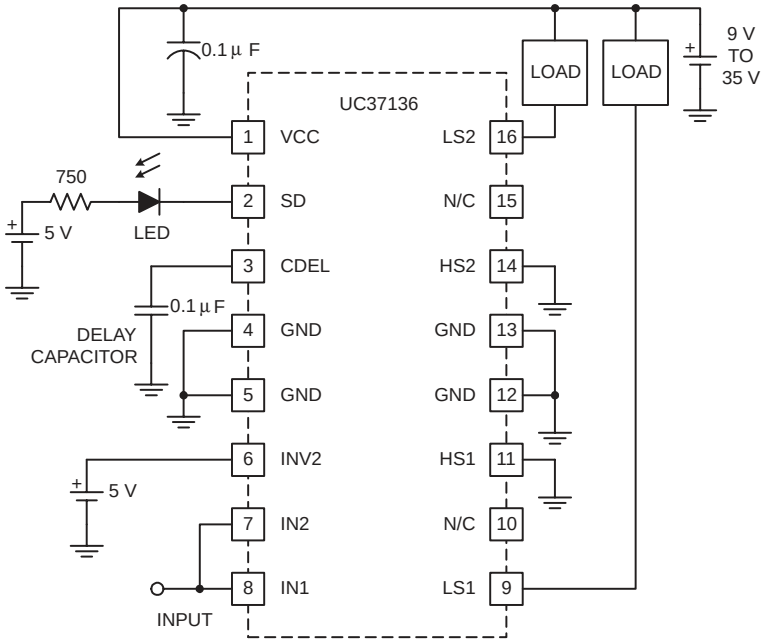
APPLICATION INFORMATION

typical applications



NOTE A: VCC, OUTPUT1 and OUTPUT2 can be connected to separate power supplies within the specified Absolute Maximum Ratings.

Figure 1. Both Switches Configured as High Side, Switch 2 Inverted with Respect to Switch 1

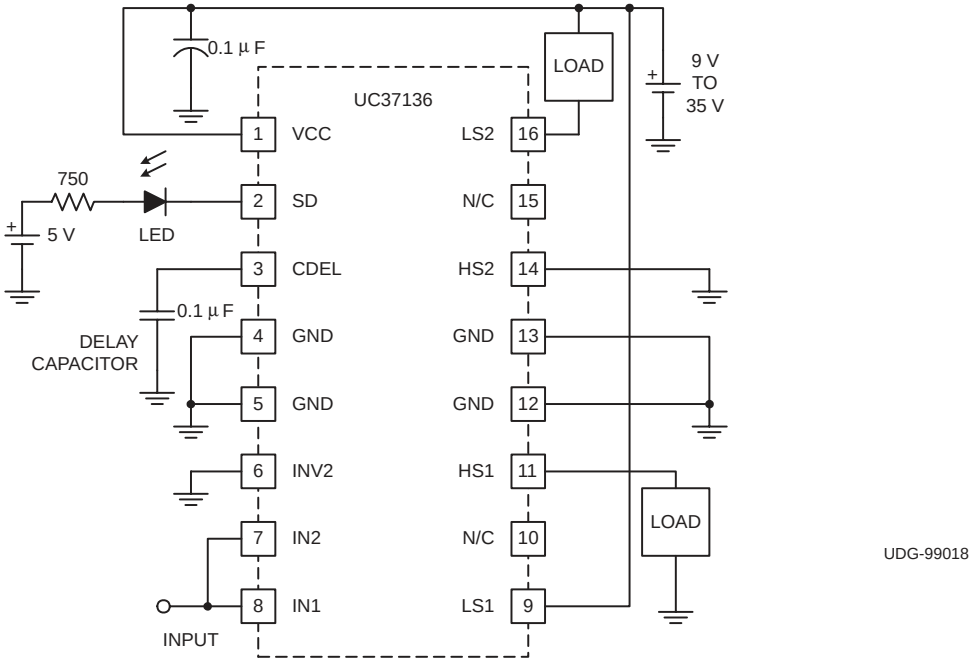


NOTE A: VCC, OUTPUT1 and OUTPUT2 can be connected to separate power supplies within the specified Absolute Maximum Ratings.

Figure 2. Both Switches Configured as Low Side, Switch 2 Inverted with Respect to Switch 1

APPLICATION INFORMATION

typical applications (continued)



NOTE A: VCC, OUTPUT1 and OUTPUT2 can be connected to separate power supplies within the specified Absolute Maximum Ratings.

Figure 3. Switch 1 High Side, Switch 2 Low Side, in Phase with Each Other

PACKAGING INFORMATION

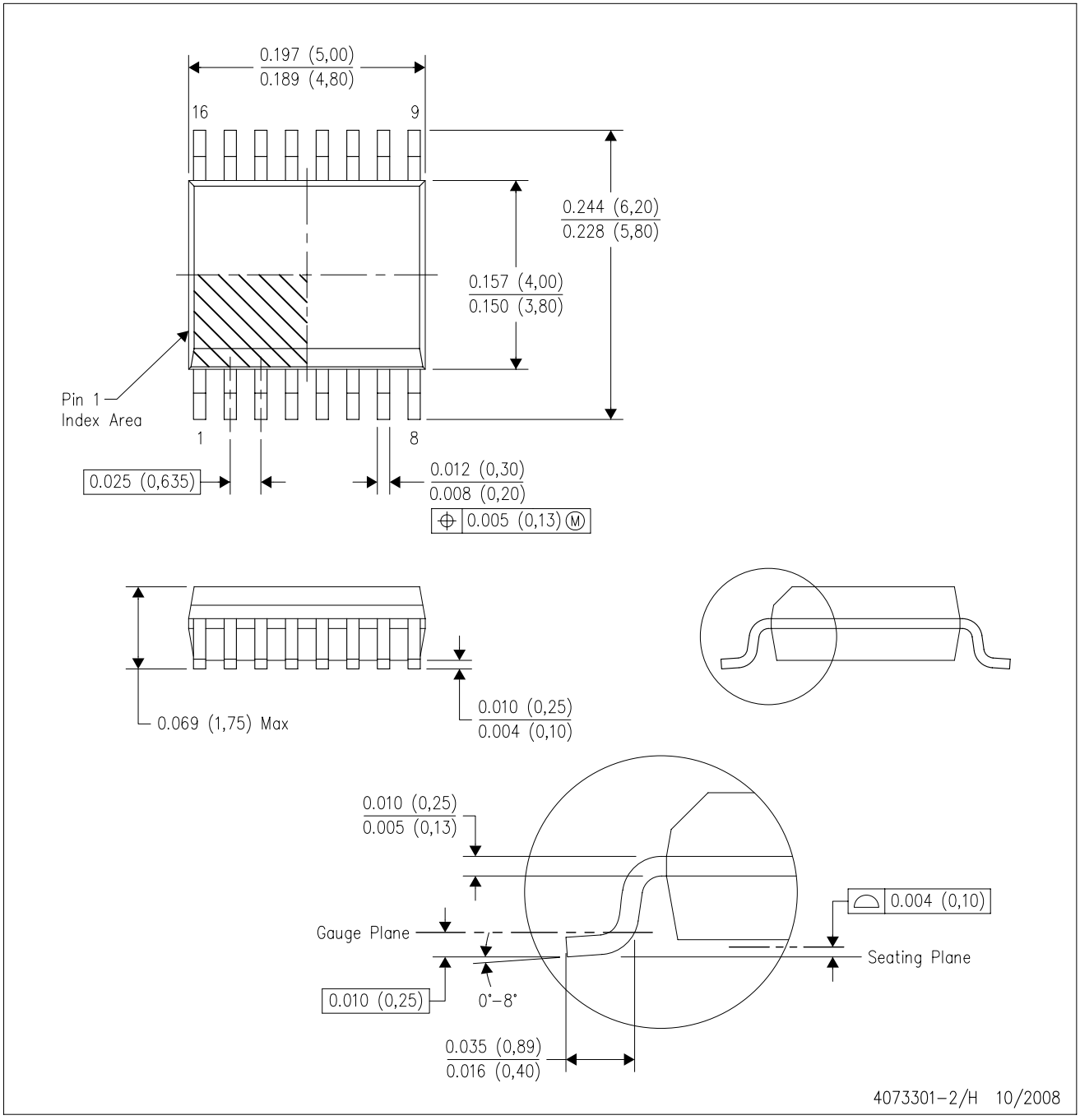
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC37136M	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC37136MG4	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

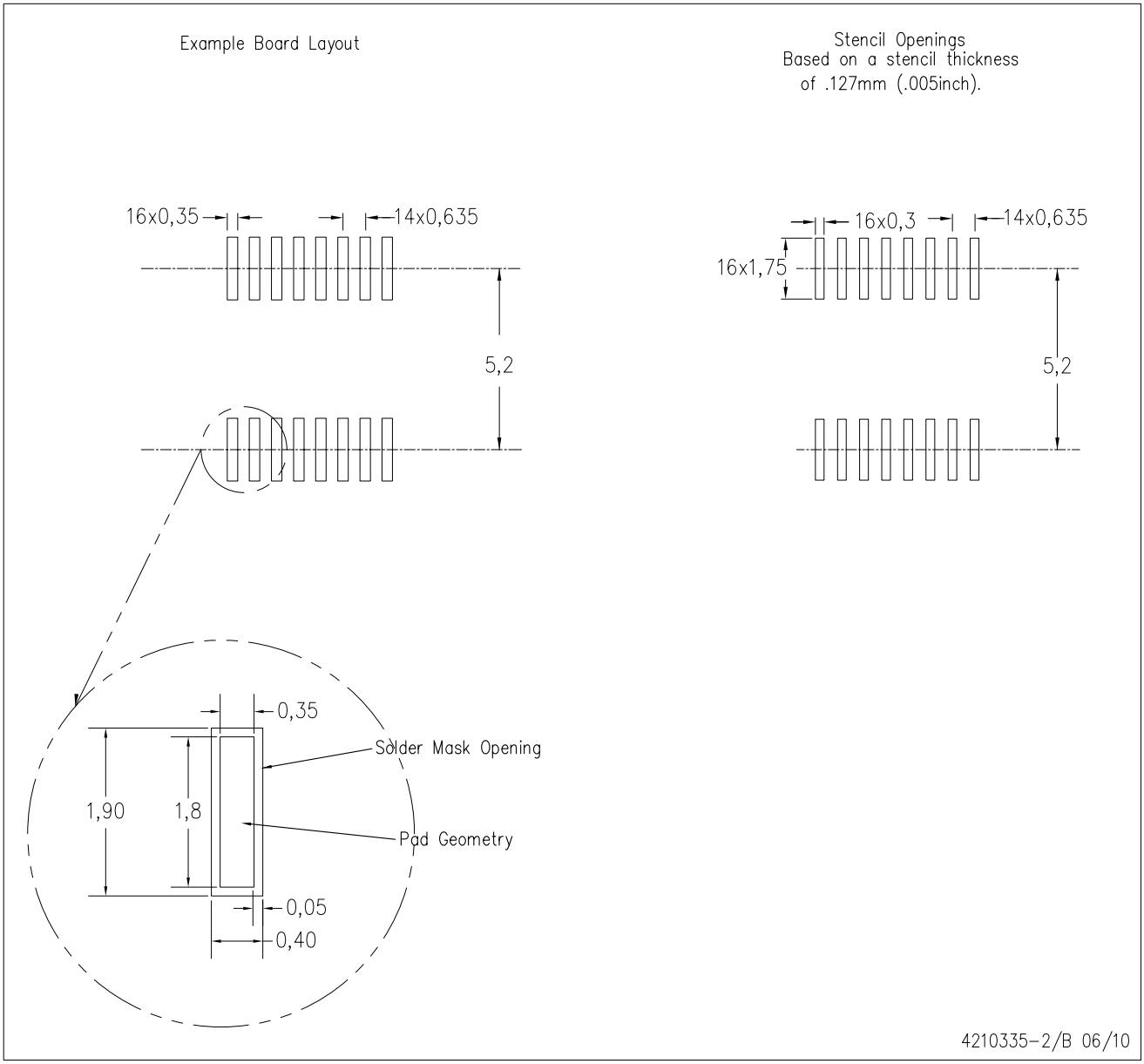
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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