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NTB125N02R, NTP125N02R

Power MOSFET
125 A, 24 V N-Channel
TO-220, D²PAK

Features

- Planar HD3e Process for Fast Switching Performance
- Body Diode for Low t_{rr} and Q_{rr} and Optimized for Synchronous Operation
- Low C_{iss} to Minimize Driver Loss
- Optimized Q_{gd} and $R_{DS(on)}$ for Shoot−through Protection
- Low Gate Charge
- Pb−Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	24	V_{dc}
Gate−to−Source Voltage − Continuous	V_{GS}	±20	V_{dc}
Thermal Resistance − Junction−to−Case Total Power Dissipation @ T_C = 25°C Drain Current − Continuous @ T_C = 25°C, Chip Continuous @ T_C = 25°C, Limited by Package Continuous @ T_A = 25°C, Limited by Wires Single Pulse (t_p = 10 μs)	$R_{\theta JC}$ P_D I_D I_D I_D I_D	1.1 113.6 125 120.5 95 250	°C/W W A A A A
Thermal Resistance − Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C	 $R_{\theta JA}$ P_D I_D	 46 2.72 18.6	 °C/W W A
Thermal Resistance − Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C	 $R_{\theta JA}$ P_D I_D	 63 1.98 15.9	 °C/W W A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 50 V_{dc}, V_{GS} = 10 V_{dc}, I_L = 15.5 A_{pk}, L = 1 mH, R_G = 25 Ω)	E_{AS}	120	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1 inch pad size, (Cu Area 1.127 in^2).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in^2).

PIN ASSIGNMENT

PIN	FUNCTION
1	Gate
2	Drain
3	Source
4	Drain

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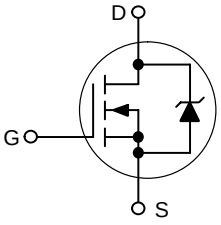
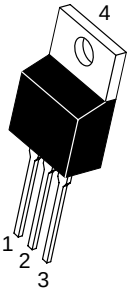
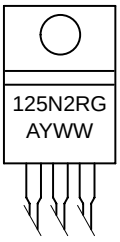
125 AMPERES, 24 VOLTS
$R_{DS(on)}$ = 3.7 mΩ (Typ)

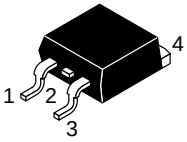


MARKING DIAGRAMS

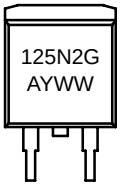


TO−220AB
CASE 221A
STYLE 5





D²PAK
CASE 418AA
STYLE 2



125N2x = Device Code
x = R
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 V_{dc}, I_D = 250 μA_{dc}) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	 25 −	 28 15	 − −	V_{dc} mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}) (V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}, T_J = 125°C)	I_{DSS}	 − −	 − −	 1.5 10	μA_{dc}
Gate−Body Leakage Current (V_{GS} = ±20 V_{dc}, V_{DS} = 0 V_{dc})	I_{GSS}	−	−	±100	nA_{dc}
ON CHARACTERISTICS (Note 3)					
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μA_{dc}) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	 1.0 −	 1.5 5.0	 2.0 −	V_{dc} mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 10 V_{dc}, I_D = 110 A_{dc}) (V_{GS} = 4.5 V_{dc}, I_D = 55 A_{dc}) (V_{GS} = 10 V_{dc}, I_D = 20 A_{dc}) (V_{GS} = 4.5 V_{dc}, I_D = 20 A_{dc})	$R_{DS(on)}$	 − − − −	 3.7 4.9 3.7 4.7	 − − 4.6 6.2	mΩ
Forward Transconductance (Note 3) (V_{DS} = 10 V_{dc}, I_D = 15 A_{dc})	g_{FS}	−	44	−	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 20 V_{dc}, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	−	2710	3440	pF
Output Capacitance		C_{oss}	−	1105	1670	
Transfer Capacitance		C_{rss}	−	227	640	
SWITCHING CHARACTERISTICS (Note 4)					
Turn−On Delay Time	(V_{GS} = 10 V_{dc}, V_{DD} = 10 V_{dc}, I_D = 40 A_{dc}, R_G = 3 Ω)	$t_{d(on)}$	−	11	22	ns
Rise Time		t_r	−	39	80	
Turn−Off Delay Time		$t_{d(off)}$	−	27	40	
Fall Time		tf	−	21	40	
Gate Charge	(V_{GS} = 4.5 V_{dc}, I_D = 40 A_{dc}, V_{DS} = 10 V_{dc}) (Note 3)	Q_T	−	23.6	28	nC
		Q_1	−	5.1	−	
		Q_2	−	11	−	
SOURCE−DRAIN DIODE CHARACTERISTICS					
Forward On−Voltage	(I_S = 20 A_{dc}, V_{GS} = 0 V_{dc}) (Note 3) (I_S = 55 A_{dc}, V_{GS} = 0 V_{dc}) (I_S = 20 A_{dc}, V_{GS} = 0 V_{dc}, T_J = 125°C)	V_{SD}	 − − −	 0.82 0.99 0.65	 1.2 − −	V_{dc}
Reverse Recovery Time	(I_S = 30 A_{dc}, V_{GS} = 0 V_{dc}, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	−	36.5	−	ns
		t_a	−	17.7	−	
		t_b	−	18.8	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.024	−	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NTP125N02R	TO−220AB	50 Units / Rail
NTP125N02RG	TO−220AB (Pb−Free)	50 Units / Rail
NTB125N02R	D^2PAK	50 Units / Rail
NTB125N02RG	D^2PAK (Pb−Free)	50 Units / Rail
NTB125N02RT4	D^2PAK	800 Units / Tape & Reel
NTB125N02RT4G	D^2PAK (Pb−Free)	800 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

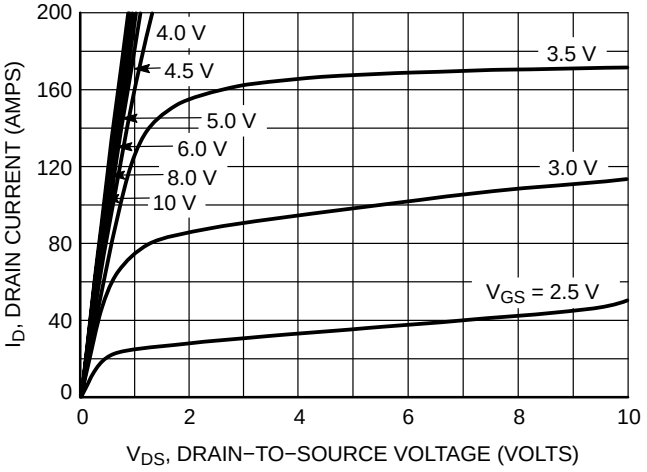


Figure 1. On−Region Characteristics

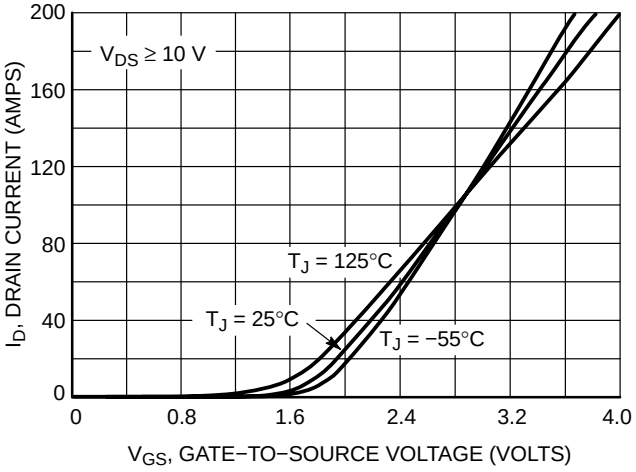


Figure 2. Transfer Characteristics

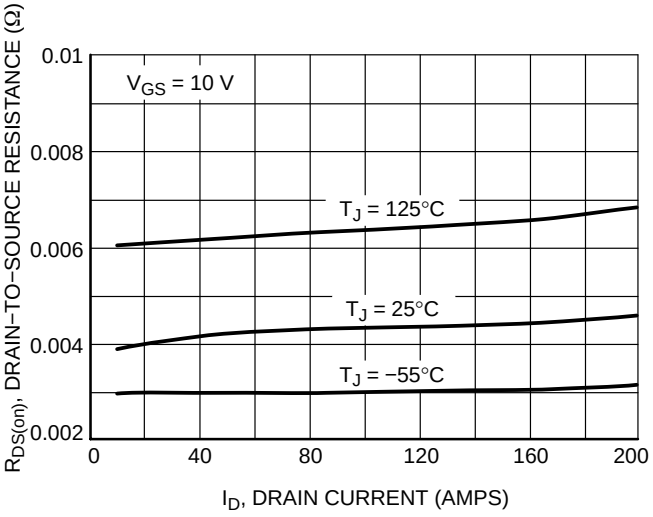


Figure 3. On−Resistance versus Drain Current and Temperature

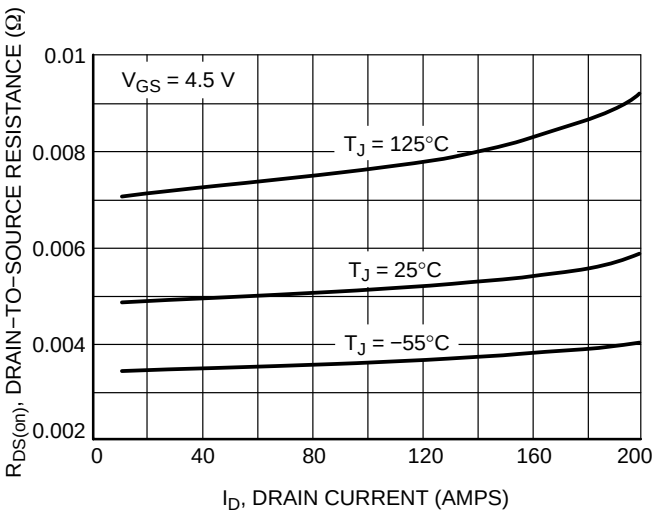


Figure 4. On−Resistance versus Drain Current and Temperature

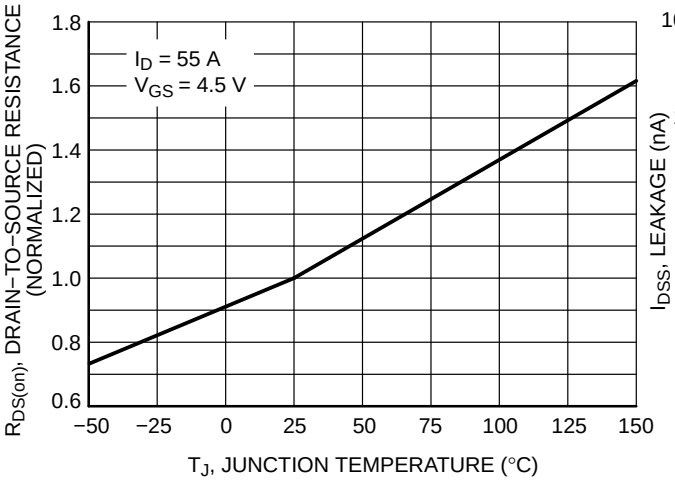


Figure 5. On−Resistance Variation with Temperature

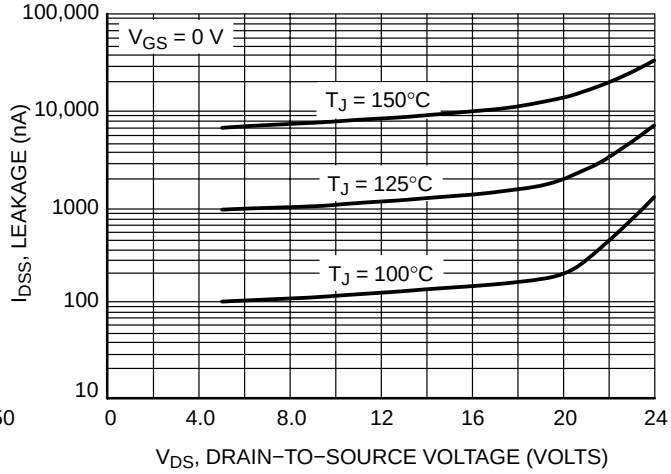


Figure 6. Drain−to−Source Leakage Current versus Voltage

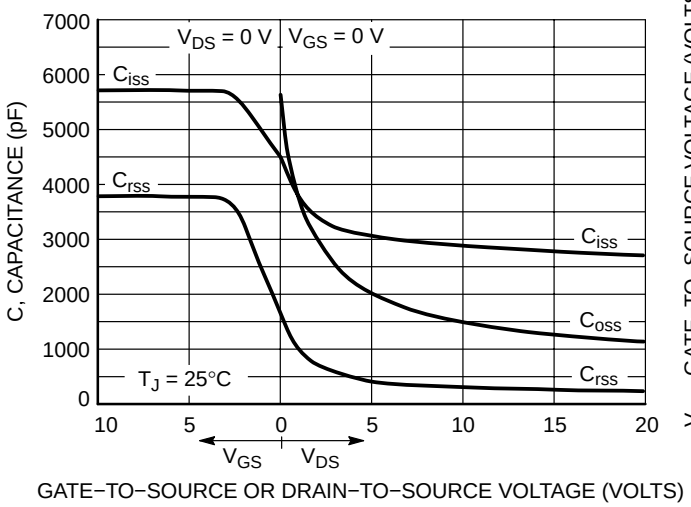


Figure 7. Capacitance Variation

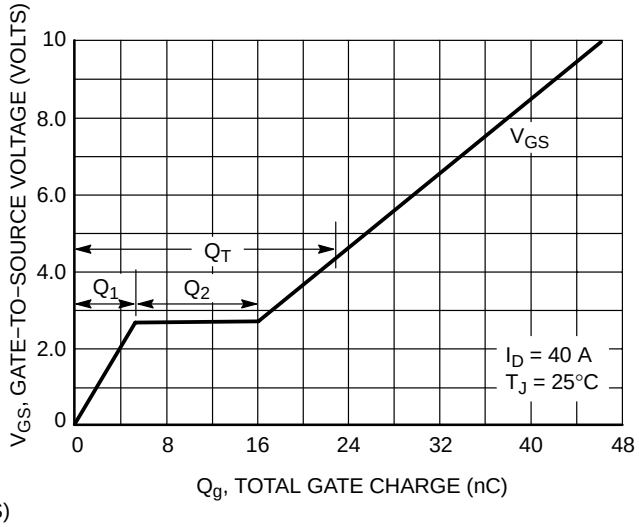


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

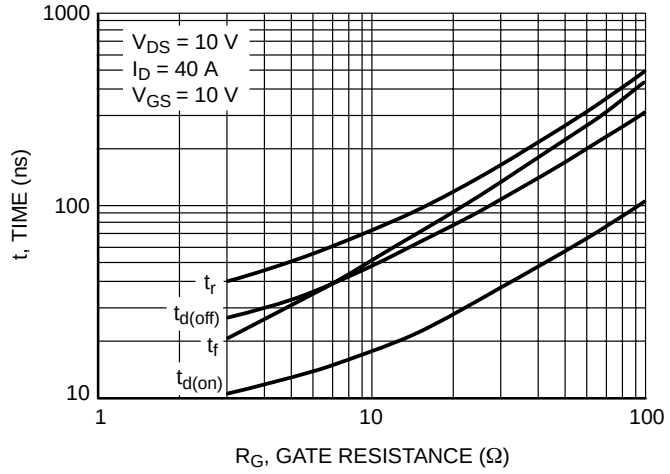


Figure 9. Resistive Switching Time Variation versus Gate Resistance

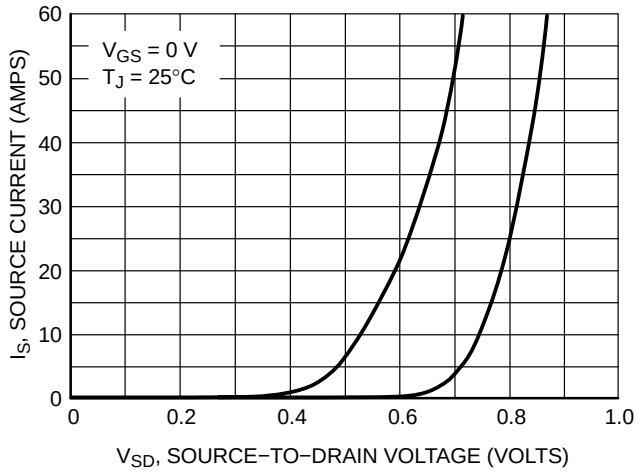


Figure 10. Diode Forward Voltage versus Current

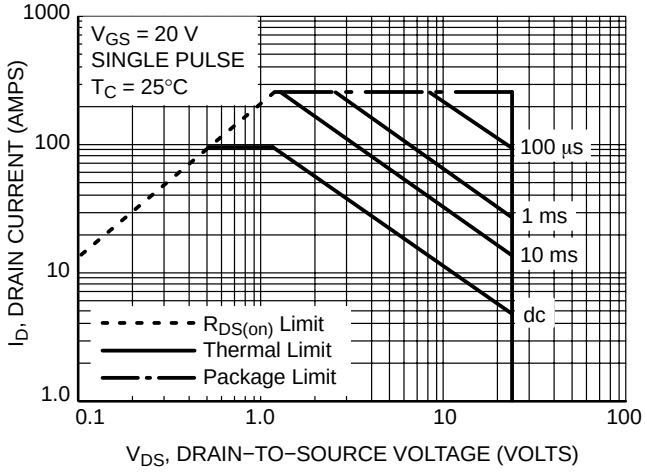


Figure 11. Maximum Rated Forward Biased Safe Operating Area

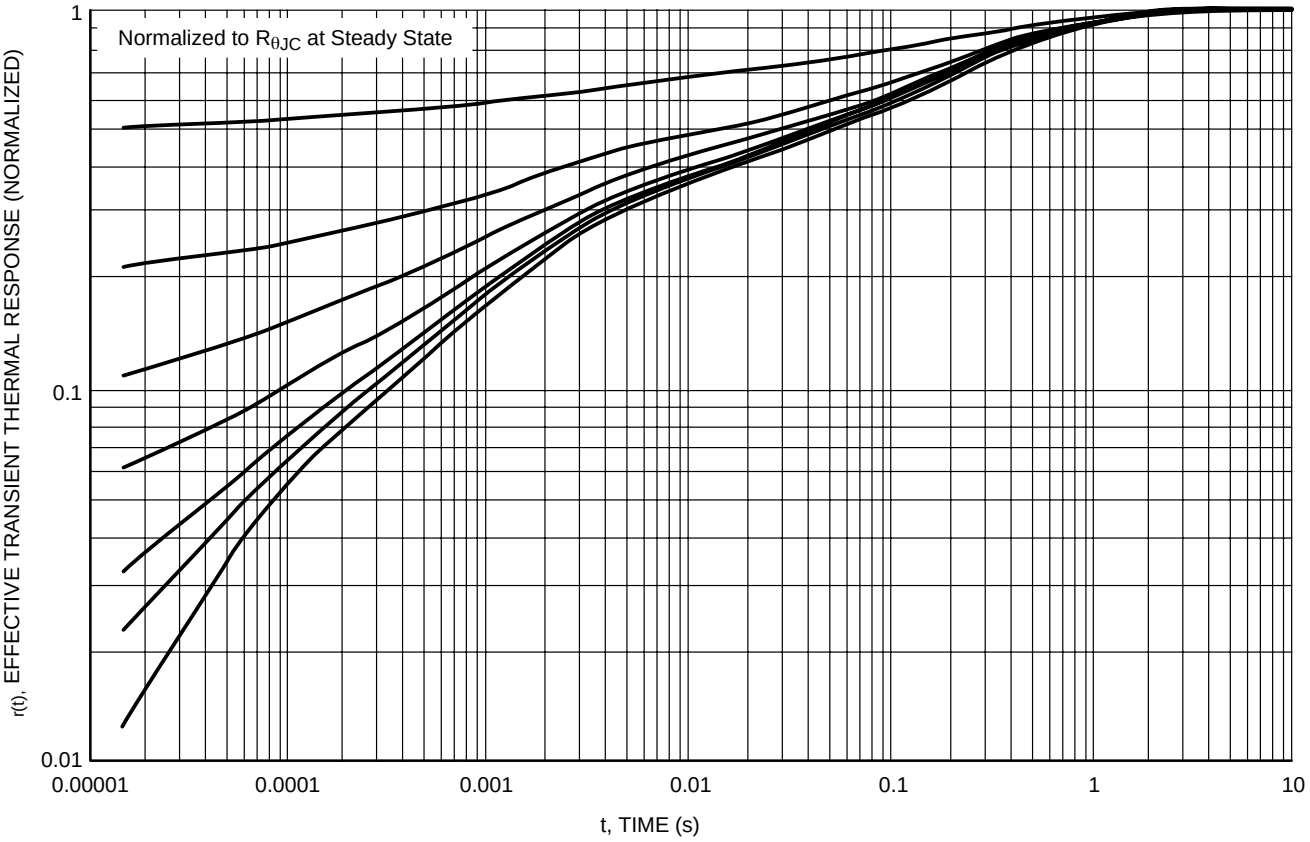
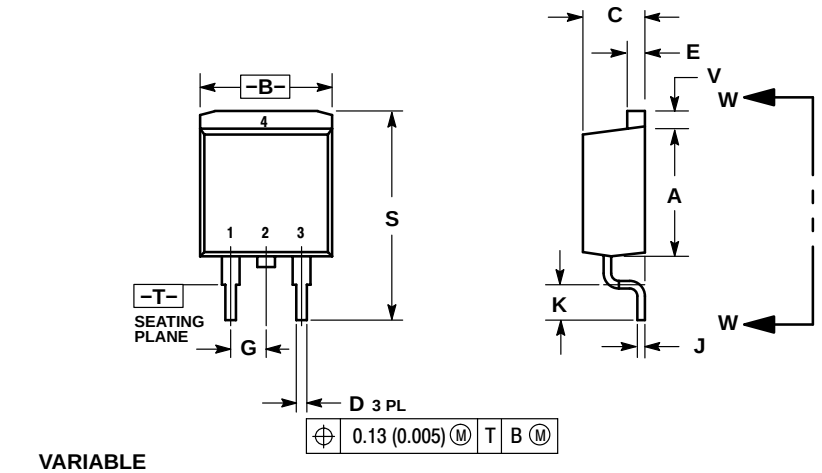


Figure 12. Thermal Response

PACKAGE DIMENSIONS

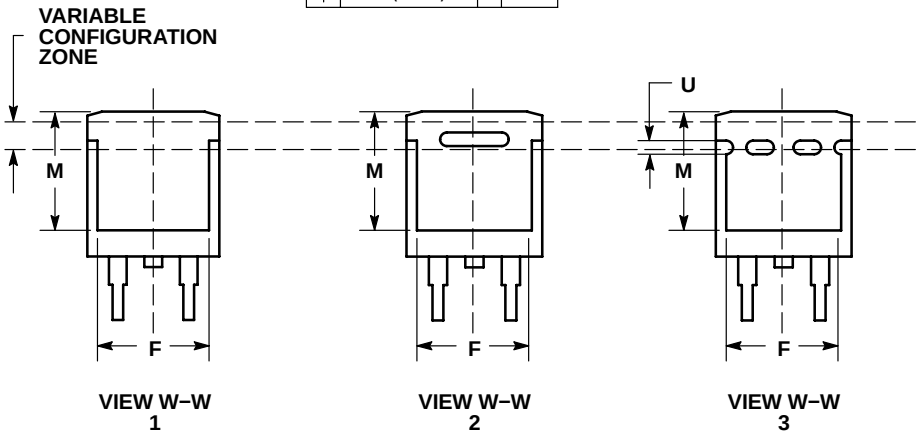
D²PAK
CASE 418AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

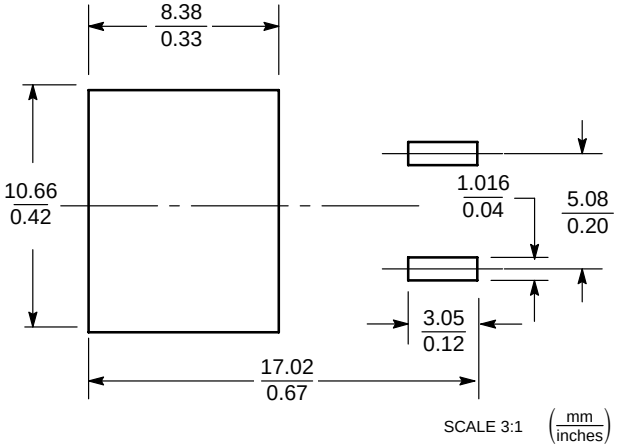
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310	−−−	7.87	−−−
G	0.100 BSC		2.54 BSC	
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280	−−−	7.11	−−−
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



VIEW W−W 1 | VIEW W−W 2 | VIEW W−W 3

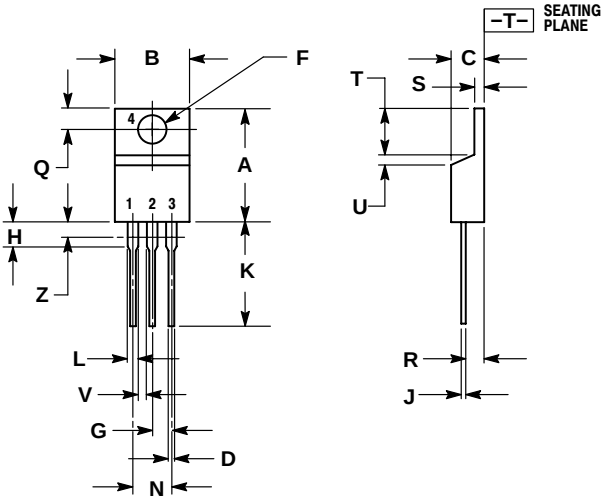
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

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