

Structure : Silicon Monolithic Integrated Circuit
Product Name : Power Driver For CD/D/D Players

Device Name : BD8201FM
Externals dinensional drawing : Figure 1
POWER DISSIPATION : Figure 2
BLOCK DIAGRAM : Figure 3
Applied circuit chart : Figure 4

Features : • It is 4ch driver IC of BTL driver 3 ch and Loading driver 1 ch.

Loading driver is high D range type of MOS Output
With Loading driver Output voltage setting terminal.

· With MUTE SW

• A built-in thermal shutdown circuit is installed. • Built in Power-supply voltage descent Mute.

· BIAS Voltage descent Mute.

· HSOP- M28 Package

## • ABSOLUTE MAXI MUM RATI NOS (Ta=25°C)

Paran <b>e</b> t er	Syntool	Li mits	Uhi t
Power Supply Voltage	Vcc	15	V
Power Dissipation	Pd	2. 2 *	W
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C

\*1 When nounted on the glass/epoxy board with the size: 70 nmpx 70 nmpx the thickness: 1.6 nmpx and the rate of copper foil occupancy area: 3% or less.

Over Ta=25°C, derating at the rate of 17.6 nm/V°C.

# Range of operation power-supply voltage

	_				
Par an <b>e</b> t er	Syntool	MIN	TYP	MAX	Uhi t
BTL driver Pre part power-supply voltage	PREVCC	4. 5	7. 5	14	٧
BTL driver CH1 part power-supply voltage	VCC1	4. 5	7. 5	PREVCC	٧
BTL driver CH2, 3 part power-supply voltage	VCC23	4. 5	5. 0	PREVCC	٧
Loading driver power-supply voltage	LDVCC	4. 5	7. 5	14	٧



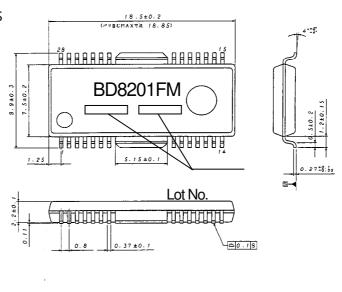
# • ELECTRI C CHARACTERI STI CS

(Unless otherwise noted Ta=25°C, PREVCC=LDVCC=VCC1=7.5V, VCC23=5V, BI AS=1.65V, RL= $8\Omega$ )

Paraneter	Syntool	MIN	TYP.	MAX.	Uhi t	Condition
	-					
Gircuit Current (at no signal) (LDVcc)	ICCLD	-	-	1.5	nA.	Under braking
Circuit Current (at no signal) (Vcc1)	ICC1	-	-	1. 0	nA.	No Ioad applied
Circuit Current (at no signal) (Vcc23)	ICC23	_	_	1.0	mA.	No load applied
Circuit Current (at no signal) (PreVcc)	I CCPRE	ı	_	25	n/A	No load applied
<btl chi∼chs="" driver=""></btl>						
Output Offset Voltage	VOFS	- 50	0	+50	n\v	
Maxinoum-Output Anpolitude (CH1)	VOM	4. 7	5.4	_	V	
Maxinoum Output Anpolitude (CH2,3)	VON23	3.7	4.0	_	V	
Olosed circuit voltage gain (OHI)	GVC1	9	12	15	dB	RI N=10KΩ
Olosed circuit voltage gain (OH2, 3)	GVC2	16	18	20	dB	
Positive and negative voltage gain (CHI~CHB)	ΔGVC	-2.0	0	2.0	dB	
Mute ON Voltage	VMON	GΛD	_	0.5	V	
Mute · Rel ease voltage	VMOFF	2.0	-	PREVCC	V	
Mute terminal inflow current	I NOTE	1	50	100	μА	VNUTE=3. 3V
Bias Terminal Input Current	IBIAS	1	50	100	μΑ	
<loading block="" ch4="" driver=""></loading>						
Output Offset Voltage	VOFSL	- 35	0	+35	n\v	Under braking
Input terninal threshold voltage H	VIΗ	2.8	ı	LDVCC	V	
Input terninal threshold voltageM	MIV	1. 2	-	2, 1	V	
Input terminal threshold voltage L	VIL	G/D	-	0.5	V	
Maxinoum Output Anpolitude	<b>VOMI</b> D	6.7	-	_	V	RL=9Ω
Voltage gain (Loading)	G/LD	4.0	6.0	8. 0	dB	LDCONT=1V
Positive and negative voltage gain (Loading)	Δ GVLD	-2.0	0	2.0	dB	
Input terninal inflow current	IIN	ı	30	60	μΑ	LDI N=3. 3V
Terminal LDCONT inflow current	ILDC	-	25	80	μΑ	LDCO <b>N</b> T=3, 3V

• Not designed for radiation resistance.

# OUTLINE DIMENSIONS, SYMBOLS

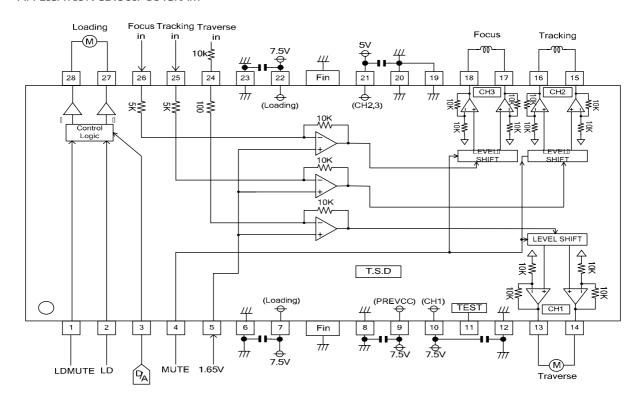


28: EX141-6002

(UNIT: mm)



# APPLICATION CIRCUIT DIAGRAM



T. S. D: (Thermal shutdown) Resistance unit:  $[\Omega]$ 

# • Each terminal explanation

		expranaci on			
Nb ·	Pin Name	Descri pti on	Nb.	Pin Name	Descri pti on
1	LDNOTE	Loading driver NOTE terminal	15	VO2(+)	BTL driver (CH2) positive output terminal
2	LŒN	Loading driver input terminal	16	VO2(-)	BTL driver (CH2) negative output terminal
3	LDCO <b>NT</b>	Loading driver Voltage setting terninal	17	VO3(+)	BTL driver (CHB) positive output terminal
4	MUTE	BTL driver NUTE terminal (CH1, CH2, CH8)	18	VO3(-)	BTL driver (CHB) negative output terminal
5	BIAS	Bias input terminal	19	G/D	GND terninnal (CH2, CH3 POWER part)
6	LDGND	GND terminal (Loading driver part)	20	G/D	GND terninnal (CH2, CH3 POWER part)
7	LDVCC	VCC terminal (Loading driver part)	21	VCC2, 3	Power supply voltage terminal (CH2, CH3 POWER part)
8	PREGND	(BTL driver, Pre part)	22	LDVCC	VCC terninal (Loading driver part)
9	PREVCC	(BTL driver, Pre part)	23	LDG/D	GND terninnal (Loading driver part)
10	VCC1	VCC terminal (CHIPO/MER part)	24	VINI	CHI input terminal
11	TEST	Input terminal for TEST mode	25	VI N2	CH2 input terminal
12	G/D	GND terminal (CHI POMER part)	26	VI NB	CHBinput terminal
13	VOI(-)	BTL driver (CH1) negative output terminal	27	LDOJT(-)	Loading driver negative output terminal
14	VOI(+)	BTL driver (CH1) positive output terminal	28	LDOJT(+)	Loading driver positive output

Note: The positive or negative polarity of driver outputs is determined by the input polarity.

- Function Description
- 1. MUTE(Pin 4)

BTL driver part (CH1 to CH3) can be switched mode ON/OFF by inputting H lever (above 2.0V) or L level (below 0.5V) to this terminal.

2.LDMUTE(Pin 1)

Loading driver part can be switched ON/OFF by inputting H level (above 2.0V) or L level (below 0.5V) to this terminal.

3.BIAS dropping mute

Setting BIAS terminal (Pin5) voltage to 0.7 or below (Typ.) vill activate mute function for BTL driver part (CH1 to CH3). Set BIAS terminal voltage to 1.1V or above.



## 4. The following table shows logics for loading driver operation.

INPUT			OUT	PUT	
LDMUTE	LDIN	LDCONT	OUT+	OUT-	FUNCTION
L	Х	Х	Hi Z	Hi Z	High impedance
Н	Х	<0.7V	HiZ	Hi Z	High impedance
Н	L	>0.7V	L	Н	REV mode
Н	Н	>0.7V	Н	L	FWD mode
Н	M or Hi Z	>0.7V	L	L	Break mode

Although the output voltage can be changed by the input voltage through the LDCONT terminal (gain 6dB Typ.), it never exceeds the maximum output voltage restricted by the power supply voltage even if applying a voltage much larger than the normal value.

Also, output of loading driver corresponded to LDCONT terminal becomes High-impedance mode by setting LDCONT terminal (3pin) to 0.7V or below

## 5. Protection circuit for VCC and GND fault

This IC contains protection circuit for VCC and GND fault to prevent itself from breaking caused by short between BTL driver output pin and VCC (VCC fault) or BTL driver output pin and GND (GND fault).

Make sure output pin should not short to VCC or GND. However in case VCC and GND fault occur, internal circuit prevents IC from breaking by limiting current. (available for only CH1, CH2, CH3)

Protection circuit for GND fault is contained to prevent from breaking caused by short between loading driver output pin and GND. Make sure output pin should not short to GND. However in case GND fault occurs, internal circuit prevents IC from breaking by limiting current.

#### Caution on use

### 1. Bypass capacitor

Connect bypass capacitor ( $0.1\mu$  F) close to this IC pin between power supplies. Also, connect capacitor ( $0\mu$  F  $\sim$  ) which is greater capacity and small ESR close to power supply terminal for reducing impedance.

#### 2 TEST terminal

TEST terminal is pulled-up in IC, therefore use it as open or by shorted with VCC.

#### 3. About absolute maximum ratings

Exceeding the absolute maximum ratings, such as the applied voltage or the operating temperature range, may cause permanent device damage. As these cases cannot be limited to the broken short mode or the open mode, if a special mode where the absolute maximum ratings may be exceeded is assumed, it is recommended to take mechanical safety measures such as attaching fuses.

### 4. About power supply lines

As a measure against the back current regenerated by a counter electromotive force of the motor, a capacitor to be used as a regenerated-current path can be installed between the power supply and GND and its capacitance value should be determined after careful check that any problems, for example, a leak capacitance of the electrolytic capacitor at low temperature, are not found in various characteristics.

### 5 .About GND potential

The electric potential of the GND terminal must be kept lowest in the circuitry at any operation states

### 6 . About thermal design

With consideration of the power dissipation (Pd) under conditions of actual use, a thermal design provided with an enough margin should be done.

## 7. About operations in a strong electric field

When used in a strong electric field, note that a malfunction may occur.

## 8.ASO

When using this IC, the output Tr must be set not to exceed the values specified in the absolute maximum ratings and ASO.

### 9. Thermal shutdown circuit

This IC incorporates a thermal shutdown circuit (TSD circuit). When the chip temperature reaches the value shown below, the coil output to the motor will be set to open. The thermal shutdown circuit is designed only to shut off the IC from a thermal runaway and not intended to protect or guarantee the entire IC functions.

Therefore, users cannot assume that the TSD circuit once activated can be used continuously in the subsequent operations.

TSD ON Temperature [°C] (typ.)	Hysteresis Temperature [°C] (typ.)
175	25

## 10. About earth wiring patterns

When a small signal GND and a large current GND are provided, it is recommended that the large current GND pattern and the small signal GND pattern should be separated and grounded at a single point of the reference point of the set in order to prevent the voltage of the small signal GND from being affected by a voltage change caused by the resistance of the pattern wiring and the large current.

Make sure that the GND wiring patterns of the external components will not change, too.

## 11. About each input terminal

This IC is a monolithic IC which has a P<sup>+</sup>isolations and P substrate to isolate elements each other.

This P layer and an N layer in each element forma PN junction to construct various parasitic elements.

Due to the IC structure, the parasitic elements are inevitably created by the potential relationship.

Activation of the parasitic elements can cause interference between circuits and may result in a malfunction or, consequently, a fatal damage. Therefore, make sure that the IC must not be used under

conditions that may activate the parasitic elements, for example, applying the lower voltage than the ground level(GND, P substrate) to the input terminals.

Note that, while not applying the power supply voltage to the IC, any voltage must not be applied to the input terminals. In addition, do not apply the voltage to input terminals without applying the

power supply voltage to the IC. Also while applying the power supply voltage, each input terminal must be the power supply voltage or less; or within the guaranteed values in the electric characteristics.

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ROHM CO., LTD. 21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto 615-8585, Japan

pan TEL:+81-75-311-2121 FAX:+81-75-315-0172

