

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

Bare Die

OptiMOS™3 Power MOS Transistor Chip
IPC022N03L3

Data Sheet

Rev. 2.5
Final

Industrial & Multimarket

1 Description

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPD075N03L G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Sawn on foil
- Backside metallization: NiV system
- Frontside metallization: AlCu system
- Passivation: Nitride + Imide

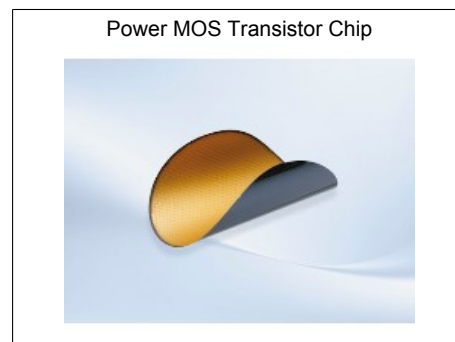
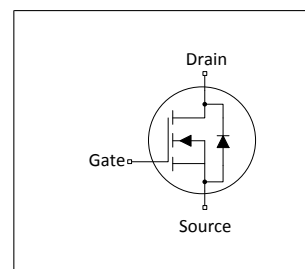


Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---------------|-------------------|-----------------|
| $V_{(BR)DSS}$ | 30 | V |
| $R_{DS(on)}$ | 7.5 ¹⁾ | mΩ |
| Die size | 2.1 x 1.05 | mm ² |
| Thickness | 175 | μm |



| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|---------|-------------|---------------|
| IPC022N03L3 | Chip | not defined | - |

2 Electrical Characteristics on Wafer Level

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|-------------------|------------------|------|--|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 30 | - | - | V | $V_{GS}=0\text{ V}, I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 1 | - | 2.2 | V | $V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 | 1 | μA | $V_{GS}=0\text{ V}, V_{DS}=30\text{ V}$ |
| Gate-source leakage current | I_{GSS} | - | 10 | 100 | nA | $V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$ |
| Drain-source on- resistance | $R_{DS(on)}$ | - | 5.3 ²⁾ | 50 ³⁾ | mΩ | $V_{GS}=10\text{ V}, I_D=2.0\text{ A}$ |
| Reverse diode forward on-voltage | V_{SD} | - | 0.75 | 1.1 | V | $V_{GS}=0\text{ V}, I_F=1\text{ A}$ |
| Internal gate resistance | R_G | - | 1.3 | - | Ω | - |
| Avalanche energy, single pulse | E_{AS} | - | 50 ⁴⁾ | - | mJ | $I_D = 12\text{ A}, R_{GS} = 25\text{ }\Omega$ |

¹⁾ packaged in a PG-TO252-3 (see ref. product)

²⁾ typical bare die $R_{DS(on)}$; $V_{GS}=10\text{ V}$ when used with 1x400μm Al-bond wire

³⁾ limited by wafer test-equipment

⁴⁾ Wafer tested. For general avalanche capability refer to the datasheet of IPD075N03L G

3 Package Outlines

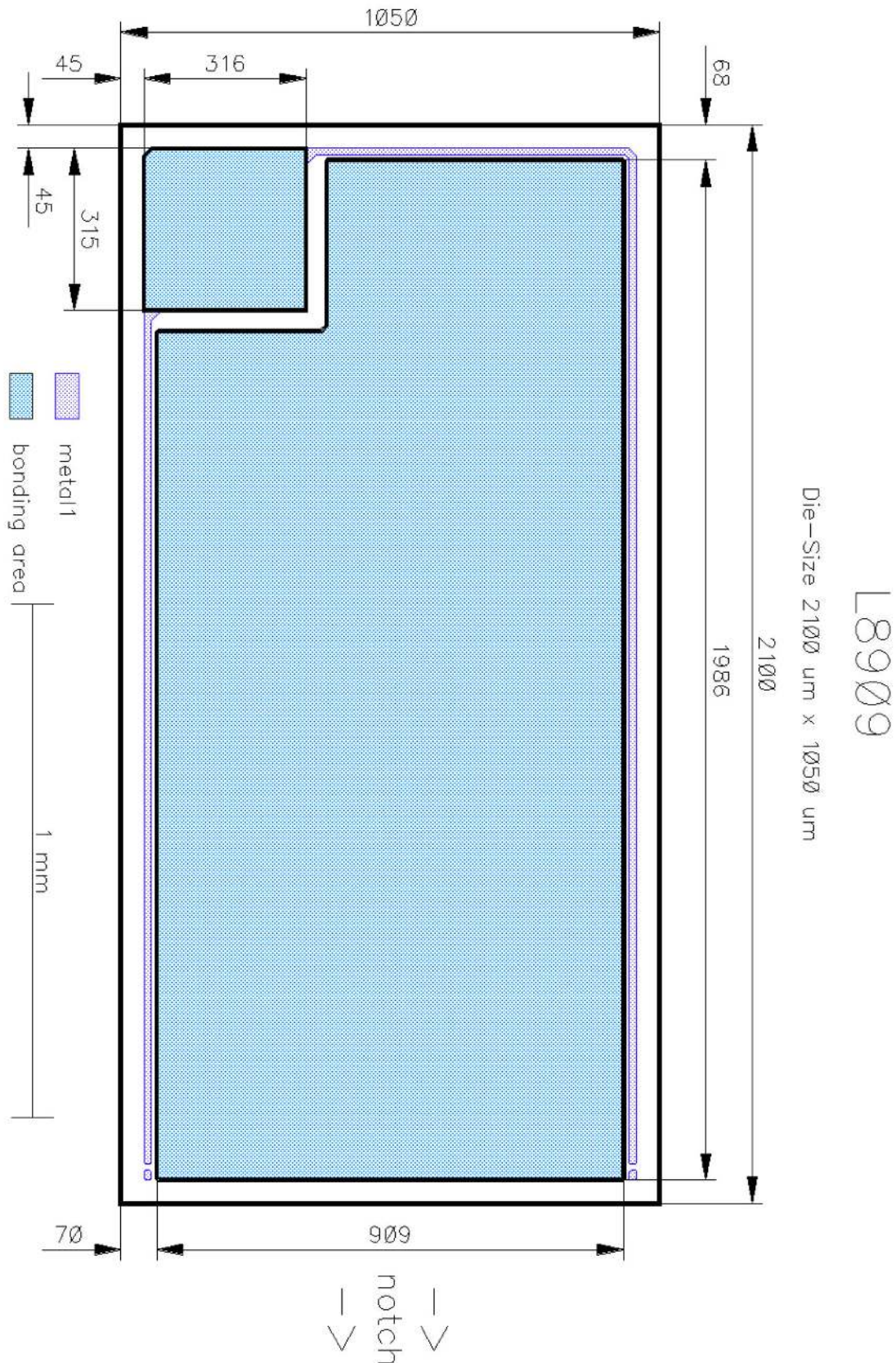


Figure 1 Outline Chip, dimensions in μm

Revision History

IPC022N03L3

Revision: 2014-07-25, Rev. 2.5

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.5 | 2014-07-25 | Release of Final Version |

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