SN65HVDA1040A-Q1 EMC-Optimized High-Speed CAN Bus Transceiver

1 Features

- Qualified for Automotive Applications
- Meets or Exceeds the Requirements of ISO 11898-2 and -5
- GIFT/ICT Compliant
- ESD Protection up to ±12 kV (Human Body Model) on Bus Pins
- Low-Current Standby Mode With Bus Wakeup, <12 µA Maximum
- High Electromagnetic Compliance (EMC)
- SPLIT Voltage Source for Common-Mode Stabilization of Bus Through Split Termination
- Digital Inputs Compatible With 3.3-V and 5-V Microprocessors
- Package Options: SOIC and VSON
- Protection Features
  - Bus-Fault Protection of –27 V to 40 V
  - TXD Dominant Time-Out
  - Thermal Shutdown Protection
  - Power Up and Power Down Glitch-Free Bus Inputs and Outputs
  - High Bus Input Impedance With Low V_{CC} (Ideal Passive Behavior on Bus When Unpowered)

2 Applications

- GMW3122 Dual-Wire CAN Physical Layer
- SAE J2284 High-Speed CAN for Automotive Applications
- SAE J1939 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface

3 Description

The SN65HVDA1040A-Q1 device meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). The device is qualified for use in automotive applications. As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the units bps (bits per second).

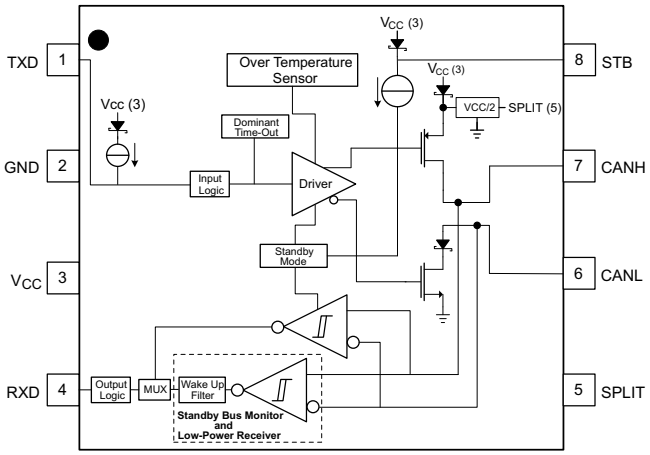
The device is designed for operation in especially harsh environments and includes many device protection features such as undervoltage lock out (UVLO), overtemperature thermal shutdown, wide common-mode range, and loss of ground protection. The bus pins are also protected against external cross-wiring, shorts to –27 V to 40 V, and voltage transients according to ISO 7637.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVDA1040A-Q1	VSON (12)	3.00 mm × 4.00 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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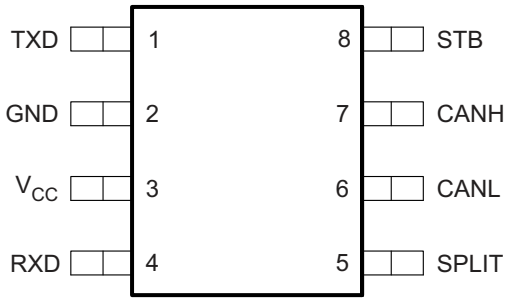
4 Revision History

Changes from Revision C (February 2011) to Revision D **Page**

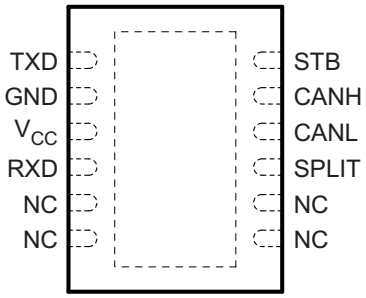
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



DSG Package
12-Pin VSON
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC	VSON		
TXD	1	1	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
GND	2	2	GND	Ground connection
V_{CC}	3	3	Supply	Transceiver 5-V supply voltage input
RXD	4	4	O	CAN receive data output (low in domonint bus state, high in recessive bus state)
SPLIT	5	9	O	Common-mode stabilization output
CANL	6	10	I/O	Low-level CAN bus line
CANH	7	11	I/O	High-level CAN bus line
STB	8	12	I	Standby mode select pin (active high)
NC	—	5-8	NC	No connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
	Voltage range at bus terminals (CANH, CANL, SPLIT)	–27	40	V
I_O	Receiver output current		20	mA
V_I	Voltage input, ISO 7637 transient pulse(2) (CANH, CANL)	–150	100	V
V_I	Voltage input (TXD, STB)	–0.3	6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested in accordance with ISO 7637 test pulses 1, 2, 3a, 3b per IBEE system level test (Pulse 1 = –100 V, Pulse 2 = 100 V, Pulse 3a = –150 V, Pulse 3b = 100 V). If DC may be coupled with ac transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal. This device has been tested with dc bus shorts to 40 V with leading common-mode chokes. If common-mode chokes are used in the system and the bus lines may be shorted to DC, ensure that the choke type and value in combination with the node termination and shorting voltage either will not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	Pins 7 and 6(2)	±12000	V
			Pin 5(3)	±10000	
			All pins	±4000	
		Charged-device model (CDM), per AEC Q100-011		±1500	
		Machine Model(4)		±200	
		IEC 61000-4-2 according to IBEE CAN EMC test specification	Pins 7 and 6 connected to pin 2	±7000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.
(3) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, SPLIT pin stressed with respect to GND.
(4) Tested in accordance JEDEC Standard 22 Test Method A115A and AEC-Q100-003.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
V_{IH}	High-level input voltage	TXD, STB	2	5.25	V
V_{IL}	Low-level input voltage	TXD, STB	0	0.8	V
V_{ID}	Differential input voltage		–6	6	V
I_{OH}	High-level output current	Driver	–70		mA
		Receiver (RXD)	–2		
I_{OL}	Low-level output current	Driver		70	mA
		Receiver (RXD)		2	
T_A	Operating free-air temperature range	See *Thermal Information*	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]			SN65HVDA1040A-Q1 DSG (VSON) 12 PINS	SN65HVDA1040A-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K thermal resistance[2]	290	140	°C/W
		High-K thermal resistance[3]	52	112	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		56	56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		14	50	°C/W
ψ_{JT}	Junction-to-top characterization parameter		6	13	°C/W
ψ_{JB}	Junction-to-board characterization parameter		19	55	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		4.5	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, Low-K board, as specified in JESD51-3, in an environment described in JESD51-2a.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

6.5 Electrical Characteristics

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
SUPPLY							
I_{CC}	5-V supply current	Standby mode	STB at V_{CC}, $V_I = V_{CC}$		6	12	µA
		Dominant	V_I = 0 V, 60-Ω load, STB at 0 V		50	70	mA
		Recessive	$V_I = V_{CC}$, No load, STB at 0 V		6	10	mA
UV_{VCC}	Undervoltage reset threshold			2.8		4	V
DRIVER							
$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 3 and Figure 16	2.9	3.4	4.5	V
		CANL		0.8		1.75	V
$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 3 and Figure 16	2	2.5	3	V
V_O	Bus output voltage (standby mode)		STB at Vcc, R_L = 60 Ω, See Figure 3 and Figure 16	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 3, Figure 16, and Figure 4	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 3, Figure 16, and Figure 4	1.4		3	V
$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 3 and Figure 16	–0.012		0.012	V
			V_I = 3 V, STB at 0 V, No load	–0.5		0.05	V
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)} + V_{O(CANL)}$)		STB at 0 V, R_L = 60 Ω, See Figure 14	0.9 V_{CC}	V_{CC}	1.1 V_{CC}	V
$V_{OC(ss)}$	Steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 9	2	2.5	3	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 9		30		mV
V_{IH}	High-level input voltage, TXD input			2			V
V_{IL}	Low-level input voltage, TXD input					0.8	V
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	µA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	µA
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	µA

(1) All typical values are at 25°C with a 5-V supply.

Electrical Characteristics (continued)

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{OS(ss)}$	Short-circuit steady-state output current, Dominant	V_{CANH} = –12 V, CANL open, TXD = low, See Figure 12	–120	–85		mA
		V_{CANH} = 12 V, CANL open, TXD = low, See Figure 12		0.4	1	
		V_{CANL} = –12 V, CANH open, TXD = low, See Figure 12	–1	–0.6		
		V_{CANL} = 12 V, CANH open, TXD = low, See Figure 12		75	120	
		V_{CANH} = 0 V, CANL open, TXD = low, See Figure 12	–100	–75		
		V_{CANL} = 32 V, CANH open, , TXD = low, See Figure 12		75	125	
$I_{OS(ss)}$	Short-circuit steady-state output current, Recessive	–20 V ≤ V_{CANH} ≤ 32 V, CANL open, TXD = high, See Figure 12	–10		10	mA
		–20 V ≤ V_{CANL} ≤ 32 V, CANH open, TXD = high, See Figure 12	–10		10	
C_O	Output capacitance	See receiver input capacitance				
RECEIVER						
V_{IT+}	Positive-going input threshold voltage, high-speed mode	STB at 0 V, See Table 1		800	900	mV
V_{IT-}	Negative-going input threshold voltage, high-speed mode	STB at 0 V, See Table 1	500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)		100	125		mV
V_{IT}	Input threshold voltage, standby mode	STB at V_{CC}	500		1150	mV
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 7	4	4.6		V
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 7		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current (unpowered bus leakage current)	CANH = CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			3	µA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		6		pF
R_{ID}	Differential input resistance	TXD at 3 V, STB at 0 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V, STB at 0 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching $[1 – (R_{IN\ (CANH)} / R_{IN\ (CANL)})] \times 100\%$	$V_{(CANH)} = V_{(CANL)}$	–3%	0%	3%	
STB PIN						
V_{IH}	High-level input voltage, STB input		2			V
V_{IL}	Low-level input voltage, STB input				0.8	V
I_{IH}	High-level input current	STB at 2 V	–10		0	µA
I_{IL}	Low-level input current	STB at 0.8 V	–10		0	µA
SPLIT PIN						
V_O	Output voltage	–500 µA < I_O < 500 µA	0.3 V_{CC}	0.5 V_{CC}	0.7 V_{CC}	V
$I_{O(stb)}$	Leakage current, standby mode	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	µA

6.6 Power Dissipation Characteristics

over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		112		mW
		V_{CC} = 5.5 V, T_J = 130°C, R_L = 45 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			170	
	Thermal shutdown temperature			185		°C

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	STB at 0 V, See Figure 10	90		230	ns
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	STB at 0 V, See Figure 10	90		230	ns
DRIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, low-to-high level output	STB at 0 V, See Figure 5	25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low level output	STB at 0 V, See Figure 5	25	45	120	ns
t_r	Differential output signal rise time	STB at 0 V, See Figure 5		25		ns
t_f	Differential output signal fall time	STB at 0 V, See Figure 5		45		ns
t_{en}	Enable time from standby mode to normal mode and transmission of dominant	See Figure 8			10	µs
$t_{(dom)}$	Dominant time-out(1)	↓V_I, See Figure 11	300	450	700	µs
RECEIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V , See Figure 7	60	90	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output	STB at 0 V , See Figure 7	45	70	130	ns
t_r	Output signal rise time	STB at 0 V , See Figure 7		8		ns
t_f	Output signal fall time	STB at 0 V , See Figure 7		8		ns
t_{BUS}	Dominant time required on bus for wakeup from standby	STB at V_{CC}, See Figure 13	1.5		5	µs

(1) The TXD dominant time-out ($t_{(dom)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(dom)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where 5 successive dominant bits are followed immediately by an error frame. This, along with the $t_{(dom)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by:
Minimum Bit Rate = 11/ $t_{(dom)}$ = 11 bits / 300 µs = 37 kbps

6.8 Typical Characteristics

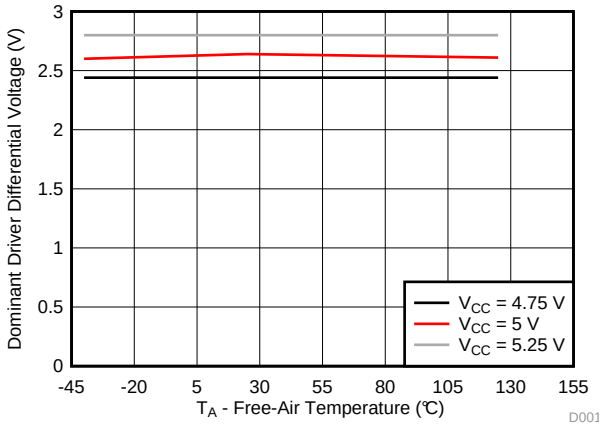


Figure 1. Dominant Driver Differential Voltage vs Free-Air Temperature

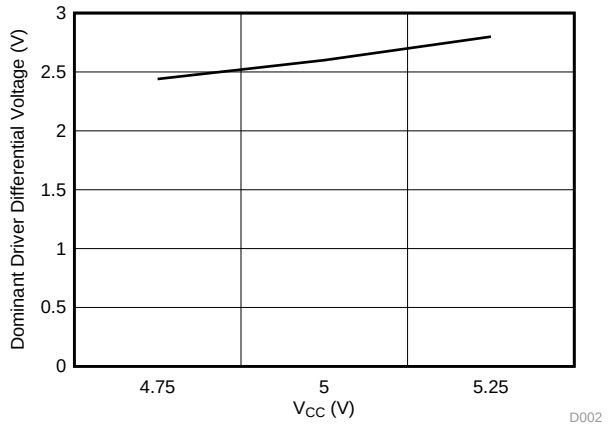


Figure 2. Driver Differential Voltage vs. Supply Voltage

7 Parameter Measurement Information

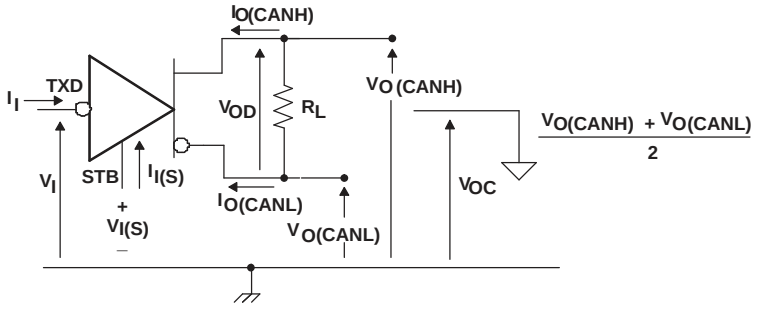


Figure 3. Driver Voltage, Current, and Test Definition

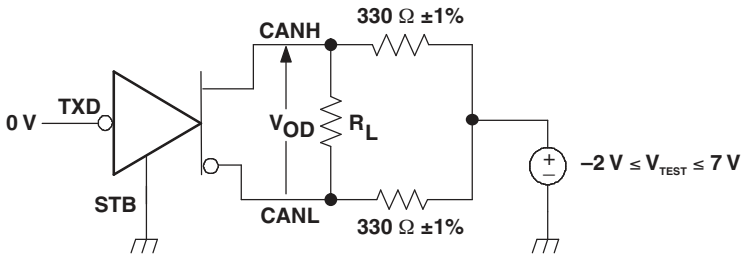


Figure 4. Driver V_{OD} Test Circuit

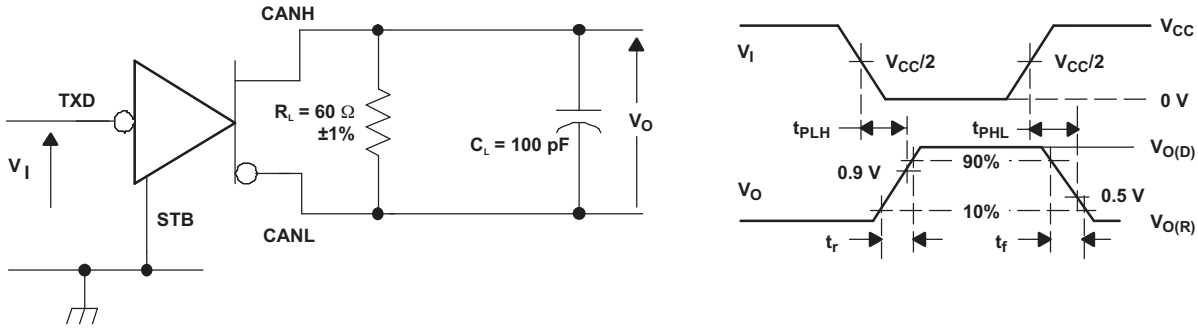


Figure 5. Driver Test Circuit and Voltage Waveforms

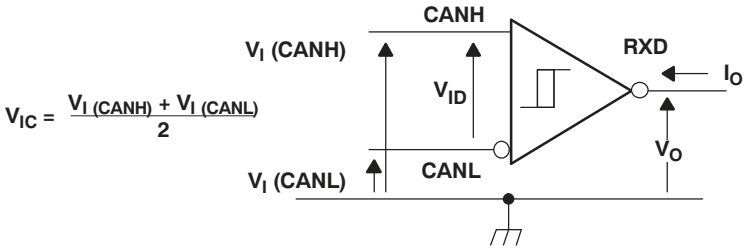
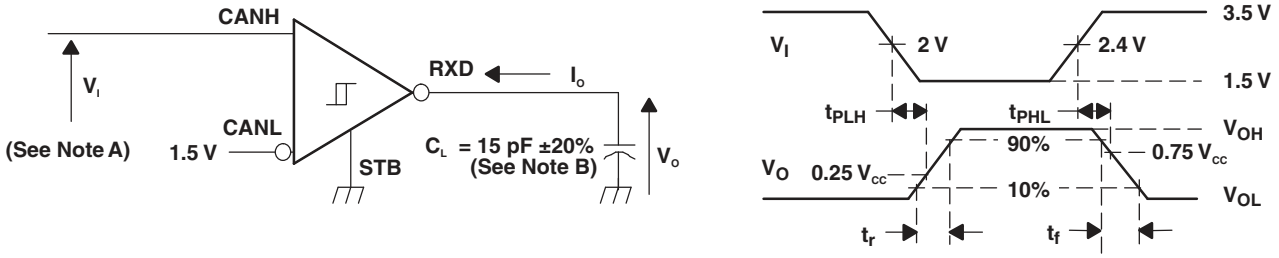


Figure 6. Receiver Voltage and Current Definitions

Parameter Measurement Information (continued)



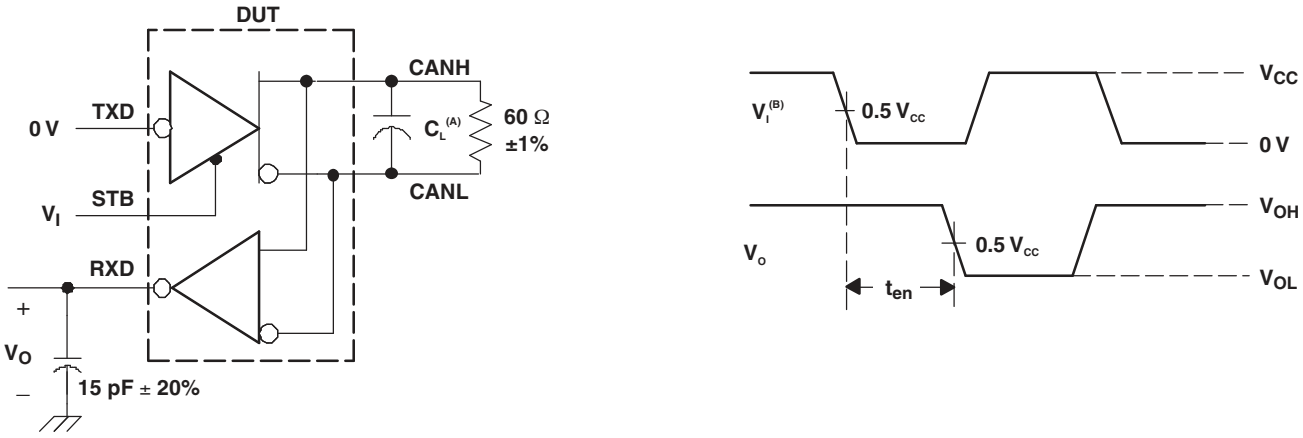
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

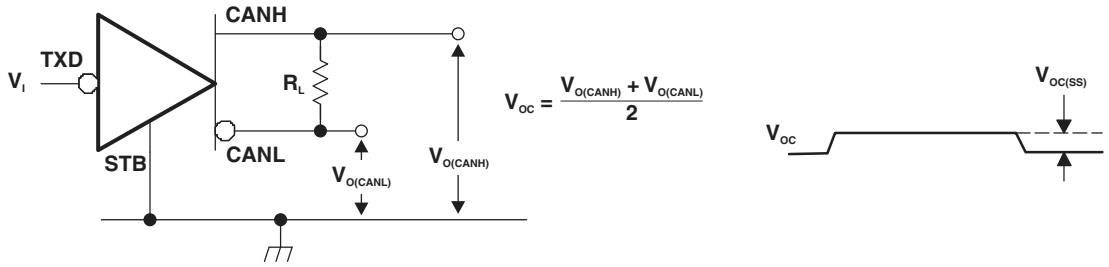
INPUT			OUTPUT R	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$		
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

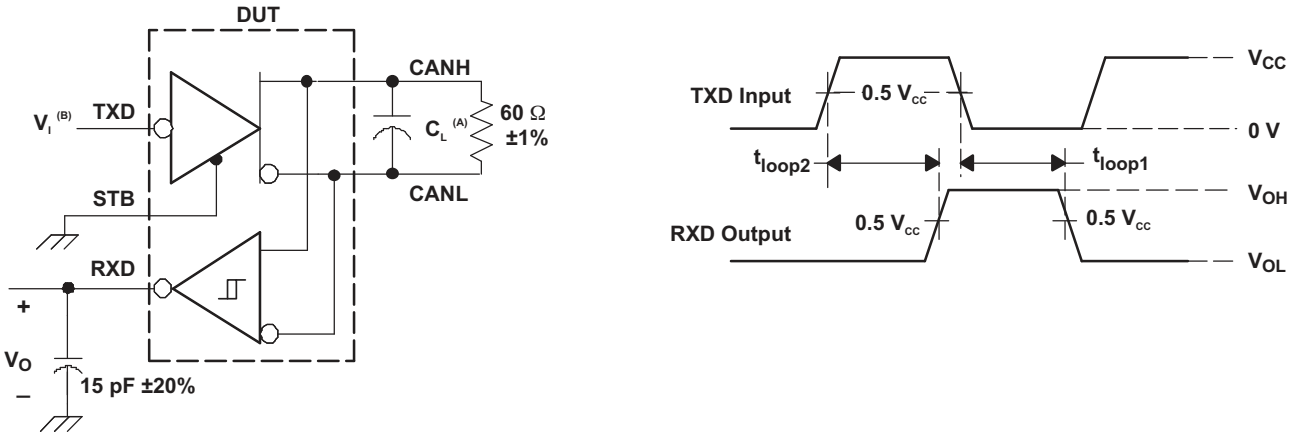
B. All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. t_{en} Test Circuit and Waveforms



NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

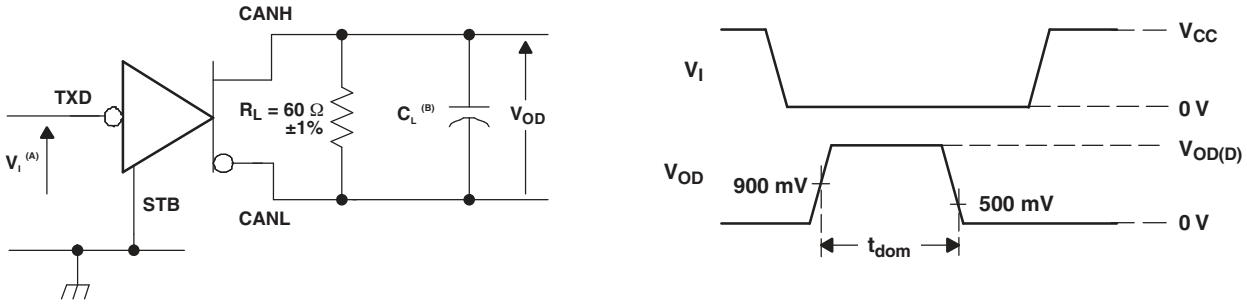
Figure 9. Common-Mode Output Voltage Test and Waveforms



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10. $t_{(LOOP)}$ Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 11. Dominant Time-Out Test Circuit and Waveforms

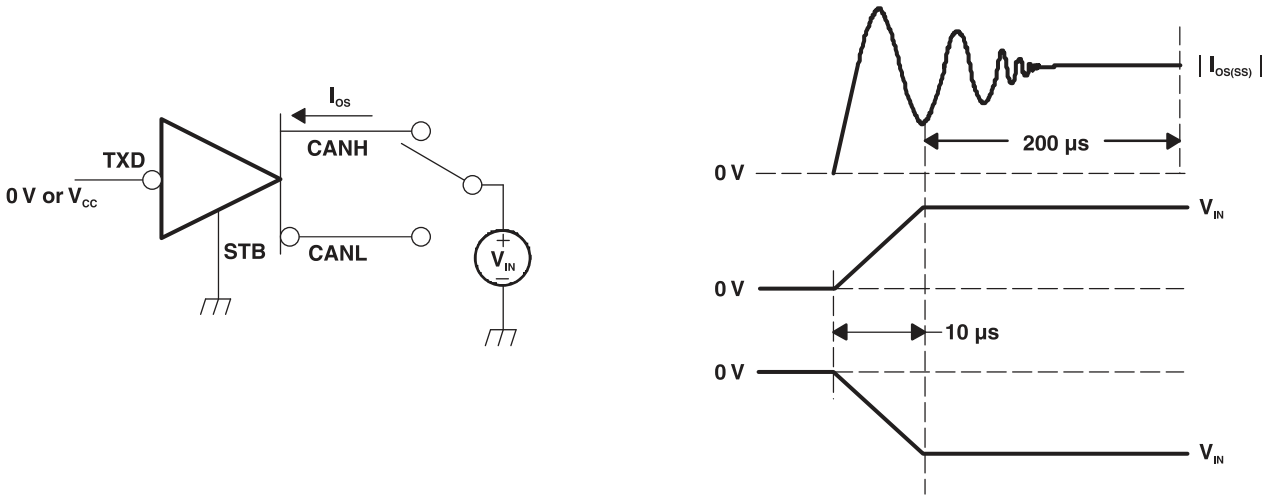
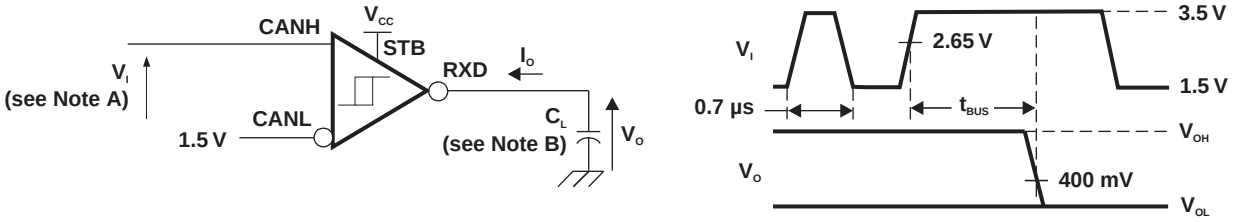


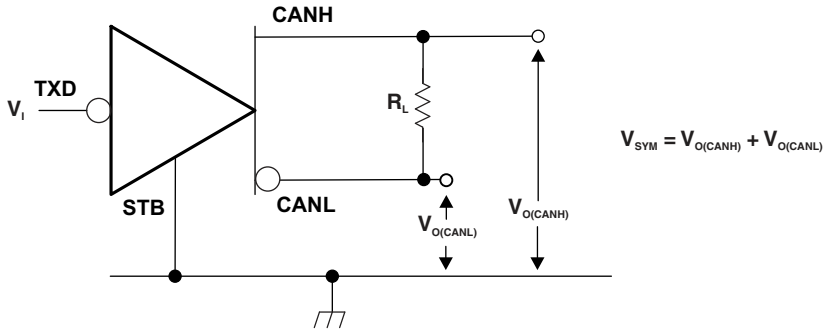
Figure 12. Driver Short-Circuit Current Test and Waveforms



A. For V_I bit width ≤ 0.7 µs, $V_O = V_{OH}$. For V_I bit width ≥ 5 µs, $V_O = V_{OL}$. V_I input pulses are supplied from a generator with the following characteristics: t_r/t_f < 6 ns.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. t_{BUS} Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r/t_f ≤ 6 ns, pulse repetition rate (PRR) = 250 kHz, 50% duty cycle.

Figure 14. Driver Output Symmetry Test Circuit

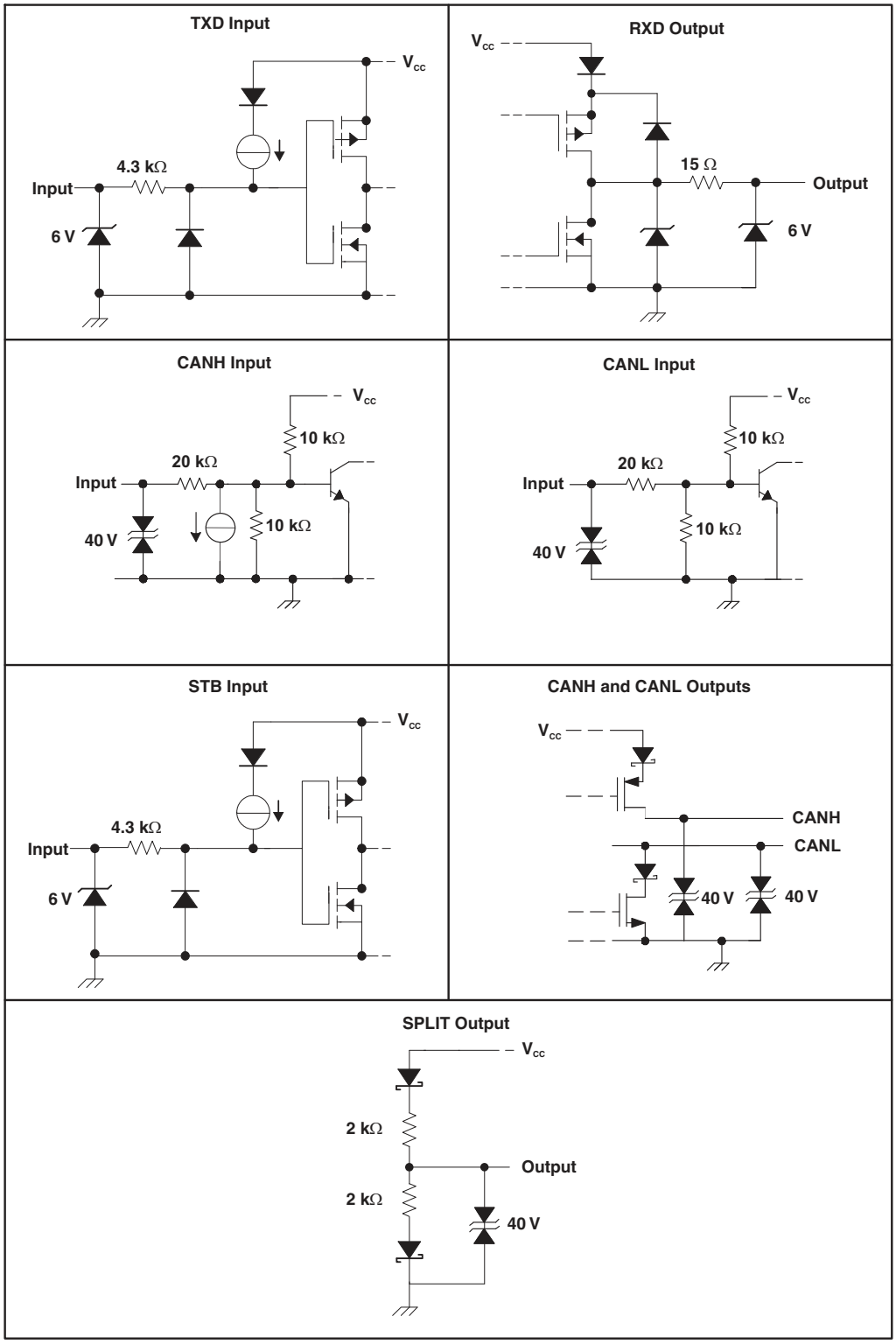


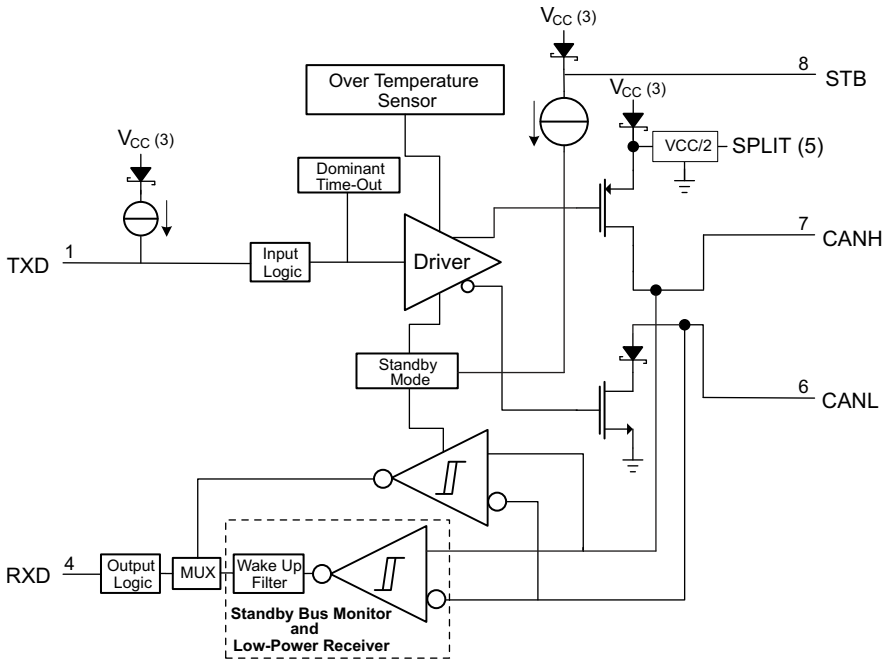
Figure 15. Equivalent Input and Output Schematic Diagrams

8 Detailed Description

8.1 Overview

The SN65HVDA1040A-Q1 CAN tranceiver is compatible with the ISO 11898-2 high-speed CAN (Controller Area Network) physical layer standard. The device is designed to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Modes

The device has two main operating modes: normal mode and standby mode. Operating mode selection is made through the STB input pin.

Table 2. Operating Modes

STB PIN	MODE	DRIVER	RECEIVER	RXD PIN
LOW	NORMAL	Enabled (On)	Enabled (On)	Mirrors CAN bus
HIGH	STANDBY	Disabled (Off)	Low-power wake-up receiver and bus monitor enabled (On)	Low = wake-up request received High = no wake-up request received

8.3.1.1 Bus States by Mode

The CAN bus has three valid states during powered operation depending on the mode of the device. In normal mode the bus may be dominant (logic low) where the bus lines are driven differentially apart or recessive (logic high) where the bus lines are biased to V_{CC}/2 through the high-ohmic internal input resistors R_{IN} of the receiver. The third state is low-power standby mode where the bus lines will be biased to GND through the high-ohmic internal input resistors R_{IN} of the receiver.

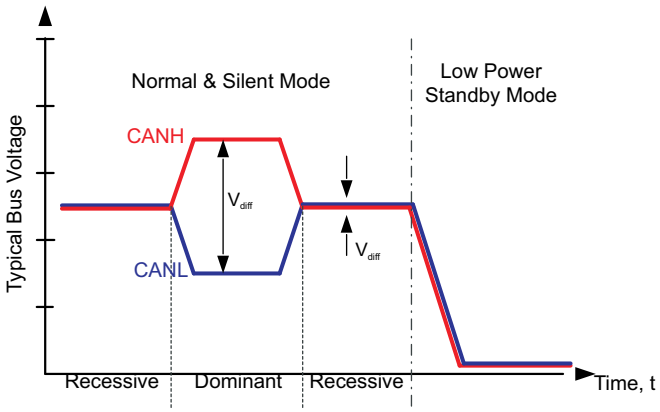


Figure 16. Bus States (Physical Bit Representation)

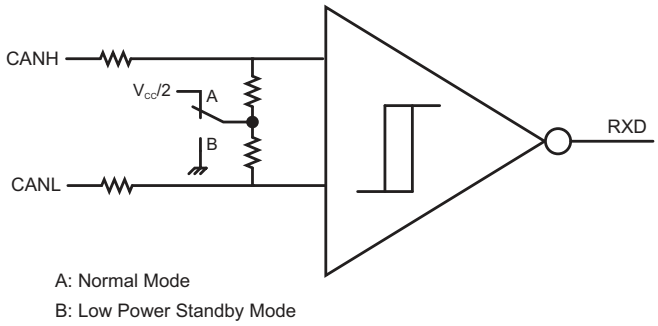


Figure 17. Simplified Common-Mode Bias and Receiver Implementation

8.3.1.2 Normal Mode

This is the normal operating mode of the device. It is selected by setting STB low. The CAN driver and receiver are fully operational and CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state the bus pins are biased to 0.5 × V_{CC}. In dominant state the bus pins (CANH and CANL) are driven differentially apart. Logic high is equivalent to recessive on the bus and logic low is equivalent to a dominant (differential) signal on the bus.

The SPLIT pin is biased to 0.5 × V_{CC} for bus common-mode bus voltage bias stabilization in split termination network applications (see *Application and Implementation*).

8.3.1.3 Standby Mode and RXD Wake-Up Request

This is the low-power mode of the device. It is selected by setting STB high. The CAN driver and main receiver are turned off and bidirectional CAN communication is not possible. The low-power receiver and bus monitor are enabled to allow for wake-up requests through the bus. A wake-up request will be output to RXD (driven low) for any dominant bus transmissions longer than the filter time t_{BUS}. The local protocol controller (MCU) should monitor RXD for transitions and then reactivate the device to normal mode based on the wake-up request. The CAN bus pins are weakly pulled to GND and the SPLIT pin is off (floating).

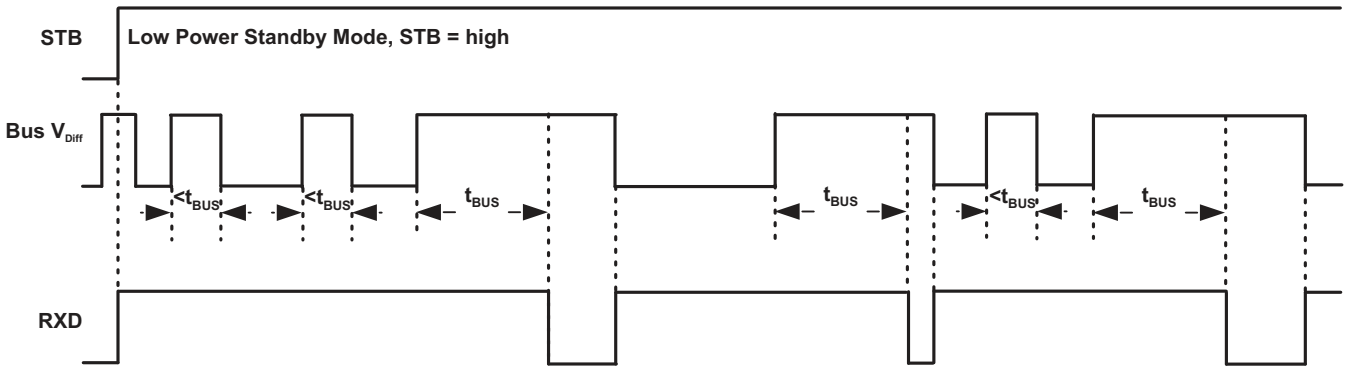


Figure 18. Standby Mode Low-Power Receiver and Bus Monitor Behavior

8.3.2 Protection Features

8.3.2.1 TXD Dominant State Time-Out

During normal mode (the only mode in which the CAN driver is active) the TXD dominant time-out circuit prevents the transceiver from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{DST}. The dominant time-out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit expires (t_{DST}), the CAN bus driver is disabled, thus freeing the bus for communication between other network nodes. The CAN driver is re-activated when a recessive signal is seen on the TXD pin, thus clearing the dominant state time-out. The CAN bus pins will be biased to recessive level during a TXD dominant state time-out and SPLIT will remain on.

NOTE

The maximum dominant TXD time allowed by the TXD Dominant state time-out limits the minimum possible data rate of the device. The CAN protocol allows a maximum of 11 successive dominant bits (on TXD) for the worst case, where 5 successive dominant bits are followed immediately by an error frame. This, along with the $t_{(dom)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = $11/t_{(dom)}$

8.3.2.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold the device will turn off the CAN driver circuits, including the SPLIT pin. This condition is cleared when the temperature drops below the thermal shutdown temperature of the device.

8.3.2.3 Undervoltage Lockout and Unpowered Device

The device has undervoltage detection and lockout on the V_{CC} supply. If an undervoltage condition is detected on V_{CC}, the device protects the bus.

The TXD pin is pulled up to V_{CC} to force a recessive input level if the pin floats. The STB is pulled up to V_{CC} to force the device in standby mode (low power) if the pin floats.

The bus pins (CANH, CANL, and SPLIT) all have extremely low leakage currents when the device is unpowered so it will not load down the bus but be an “ideal passive” load to the bus. This is critical, especially if some nodes of the network will be unpowered while the rest of the network remains in operation.

8.4 Device Functional Modes

Table 3. Driver Function Table(1)

INPUTS		OUTPUTS		BUS STATE
TXD	STB	CANH	CANL	
L	L	H	L	Dominant
H	L	Z	Z	Recessive
Open	L	Z	Z	Recessive
X	H or Open	Y	Y	Recessive

(1) H = high level, L = low level, X = irrelevant, Y = weak pulldown to GND, ? = indeterminate, Z = high impedance

Table 4. Receiver Function Table

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	STB	OUTPUT RXD	BUS STATE
$V_{ID} \geq 0.9$ V	L	L	Dominant
$V_{ID} \geq 1.15$ V	H or Open	L	Dominant
0.5 V < V_{ID} < 0.9 V	X	?	?
$V_{ID} \leq 0.5$ V	X	H	Recessive
Open	X	H	Recessive

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Using With 3.3-V Microcontrollers

The input level threshold for the digital input pins of this device are 3.3-V compatible, however a few application considerations must be taken if using this device with 3.3-V microcontrollers. Both TXD and STB input pins have internal pullup sources to V_{CC}. Some microcontroller vendors recommend using an open-drain configuration on their I/O pins in this case even though the pullup limits the current. As such care must be taken at the application level that TXD and STB have sufficient pullup to meet system timing requirements for CAN. The internal pullup on TXD especially may not be sufficient to overcome the parasitic capacitances and allow for adequate CAN timing; thus, an additional external pullup may be required. Care should also be taken with the RXD pin of the microcontroller as the RXD output of this device drives the full V_{CC} range (5 V). If the microcontroller RXD input pin is not 5-V tolerant, this must be addressed at the application level. Other options include using a CAN transceiver from TI with I/O level adapting or a 3.3-V CAN transceiver.

9.1.2 Using SPLIT With Split Termination

The SPLIT pin voltage output provides 0.5 × V_{CC} in normal mode. The circuit may be used by the application to stabilized the common-mode voltage of the bus by connecting it to the center tap of split termination for the CAN network (see Figure 19 and Figure 20). This pin provides a stabilizing recessive voltage drive to offset leakage currents of unpowered transceivers or other bias imbalances that might bring the network common-mode voltage away from 0.5 × V_{CC}. Using this feature in a CAN network improves electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltage levels at the start of message transmissions.

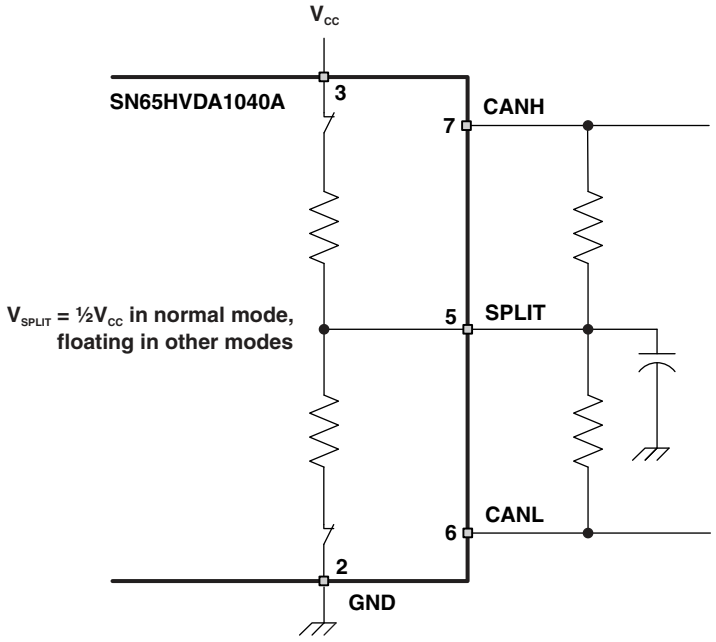


Figure 19. Split Pin Stabilization Circuitry and Application

9.2 Typical Application

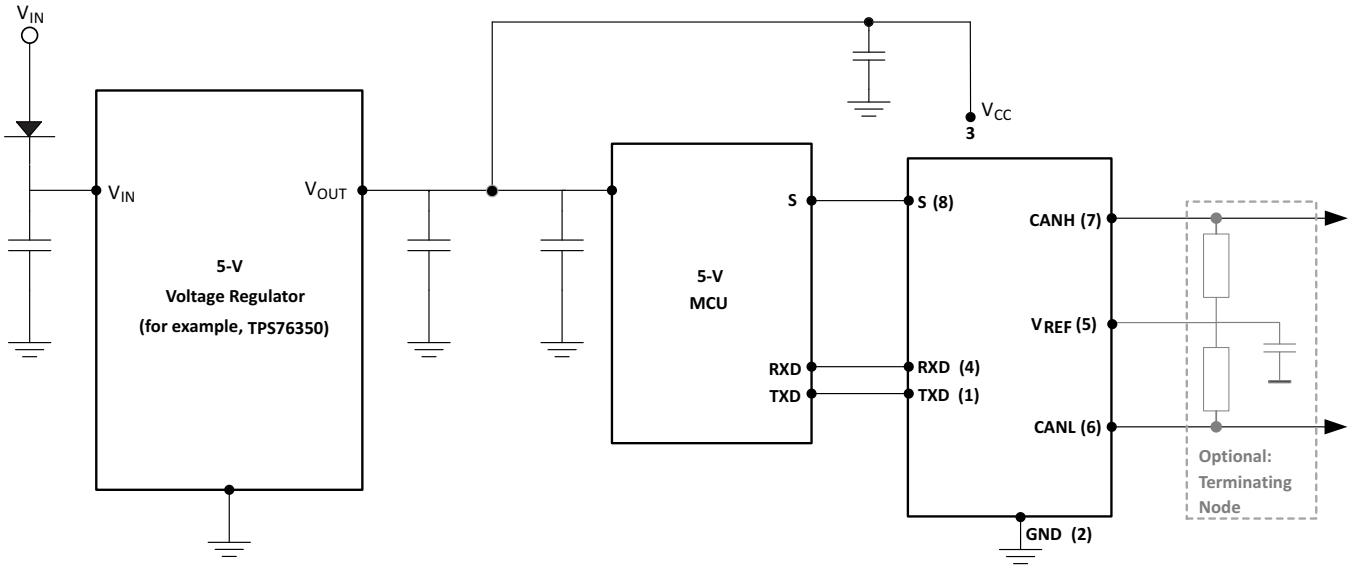


Figure 20. Typical Application Using Split Termination for Stabilization

9.2.1 Design Requirements

9.2.1.1 Bus Loading, Length, and Number of Nodes

The ISO 11898 Standard specifies up to 1 Mbps data rate, maximum bus length of 40 meters, maximum drop line (stub) length of 0.3 meters, and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet, and NMEA200.

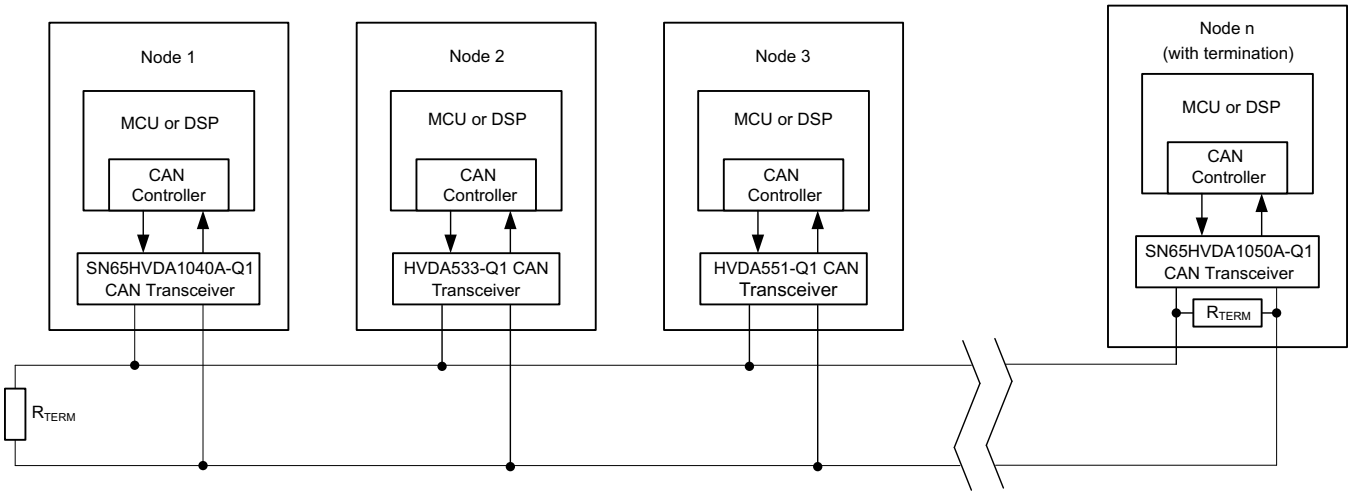


Figure 21. Typical CAN Bus Drawing

Typical Application (continued)

A high number of nodes requires a transceiver with high input impedance and wide common-mode range such as the SN65HVDA1040A-Q1 CAN transceiver. ISO 11898-2 specifies the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The SN65HVDA1040A-Q1 device is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common-mode range of –2 V to 7 V through a 330-Ω coupling network. This network represents the bus loading of 90 SN65HVDA1040A-Q1 transceivers based on their minimum differential input resistance of 30 kΩ. Therefore, the SN65HVDA1040A-Q1 supports up to 90 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1-km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

9.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used (see Figure 22 and *Using SPLIT With Split Termination*).

Care should be taken when determining the power ratings of the termination resistors. A typical worst case fault condition is if the system power supply and ground were shorted across the termination resistance which would result in much higher current through the termination resistance than the CAN transceiver's current limit.

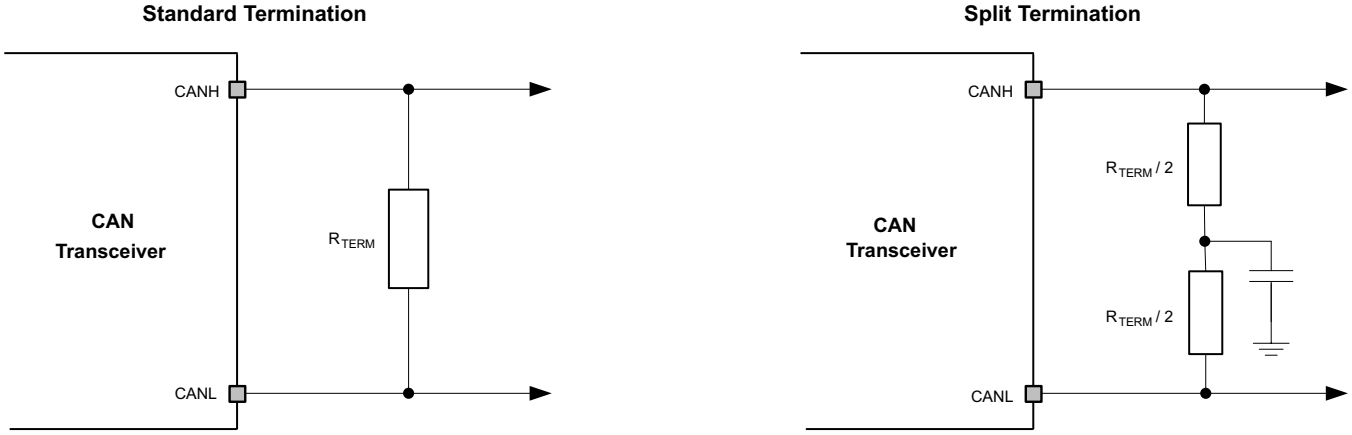


Figure 22. CAN Termination Schematic

9.2.1.3 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (the TXD pin) to the differential outputs (the CANH and CANL pins), plus the delay from the receiver inputs (the CANH and CANL) to its output (the RXD pin). A typical loop delay for the SN65HVDA1040A-Q1 transceiver is displayed in Figure 24 and Figure 25.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Transient Voltage Suppresser (TVS) Diodes

Transient voltage suppressors are the preferred protection components for a CAN bus due to their low capacitance, which allows them to be designed into every node of a multinode network without requiring a reduction in data rate. With response times of a few picoseconds and power ratings of up to several kilowatts, TVS diodes present the most effective protection against ESD, burst, and surge transients.

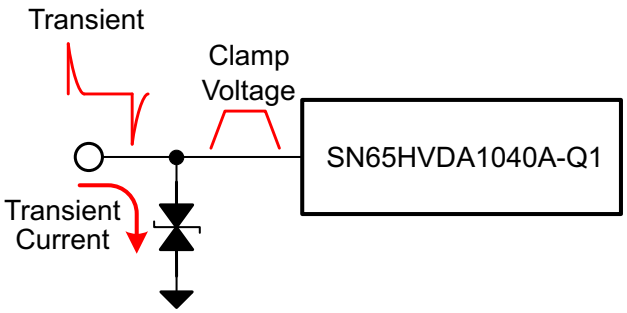


Figure 23. Transient Voltage Suppresser (TVS) Diodes Schematic

9.2.3 Application Curves

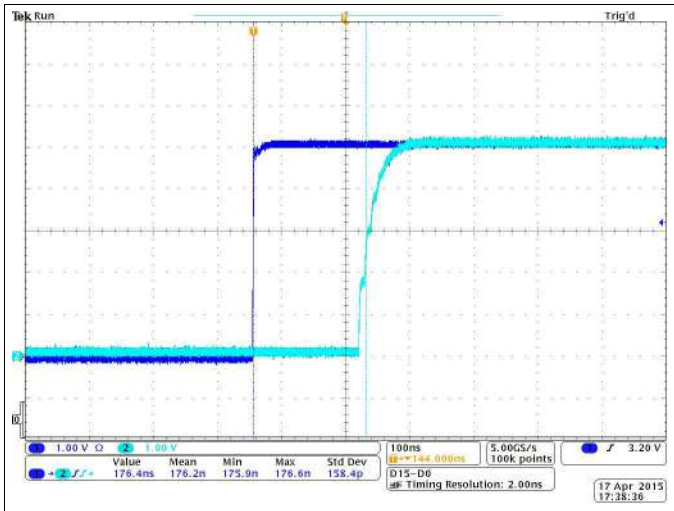


Figure 24. $t_{(LOOP)}$ Delay Waveform Dominant to Recessive

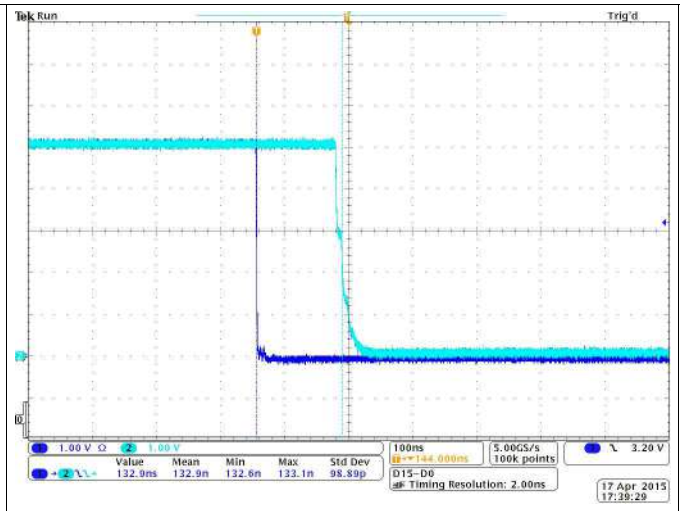


Figure 25. $t_{(LOOP)}$ Delay Waveform Recessive to Dominant

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close as possible to the V_{CC} supply pins as possible. The TPS76350 device is a linear voltage regulator suitable for the 5-V supply rail.

11 Layout

11.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. On-chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use V_{CC} and ground planes to provide low inductance.

NOTE

High-frequency current follows the path of least inductance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bidirectional diode or varistor solution) and bus filter capacitors C5 and C7 are shown in Figure 26.

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 22 shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground through capacitor C6. Split termination provides common-mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this will cause signal integrity issues if the bus is not properly terminated on both ends.

Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples include C2 and C3 (V_{CC}).

Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3, and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.

Because the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-kΩ to 10-kΩ pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open-drain host processor is used to drive the TXD pin of the device an external pullup resistor between 1 kΩ and 10 kΩ should be used to drive the recessive input state of the device.

Pin 5: SPLIT should be connected to the center point of a split temrination scheme to help stabalize the common-mode voltage to V_{CC} /2. If SPLIT is unused it should be left floating.

Pin 8: Is shown assuming the mode pin, STB, will be used. If the device will only be used in normal mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

11.2 Layout Example

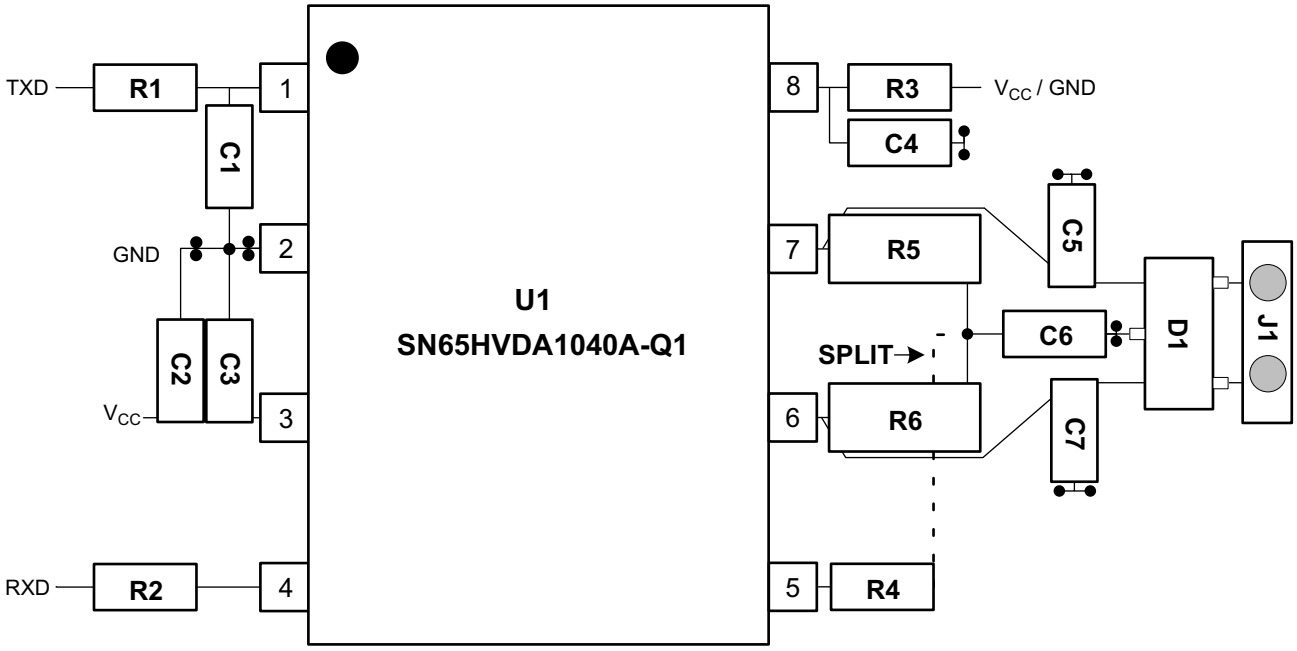


Figure 26. Typical CAN Bus Layout Example

11.3 PCB and Thermal Considerations for VSON Package

The VSON package verson of this device has an exposed thermal pad which should be connected with vias to a thermal plane. Even though this pad is not electrically connected internally TI recommends connecting the exposed pad to the GND plane. Refer to the mechanical information on the package at the end of this data sheet and application report *QFN/SON PCB Attachement* (SLUA271) for more information on proper use of this package.

11.4 ESD Protection

A typical application that employees a CAN bus network may require some form of ESD, burst, and surge protection to shield the CAN transceiver against unwanted transients that can potential damage the transceiver. To help shield the SN65HVDA1040A-Q1 transceiver against these high energy transients, transient voltage suppressors can be implemented on the CAN differential bus terminals. These devices will help absorb the impact of a ESD, burst, and/or surge strike.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

QFN/SON PCB Attachement (SLUA271)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HVDA1040AQDSJRQ1	ACTIVE	VSON	DSJ	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A1040A	Samples
SN65HVDA1040AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1040A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

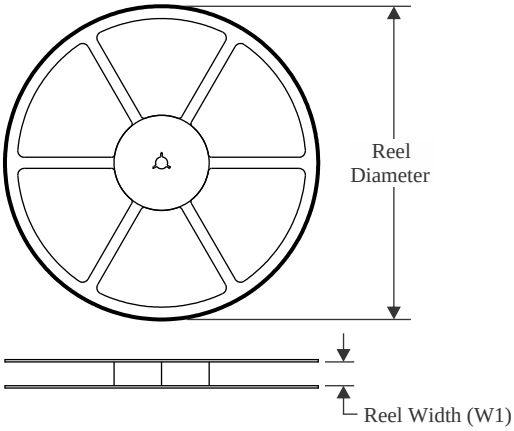
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

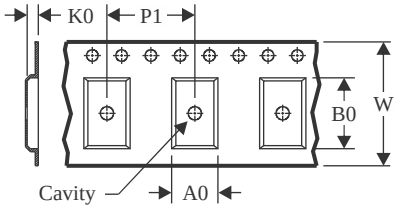
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

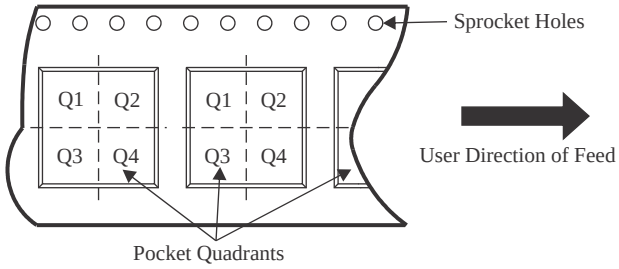


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

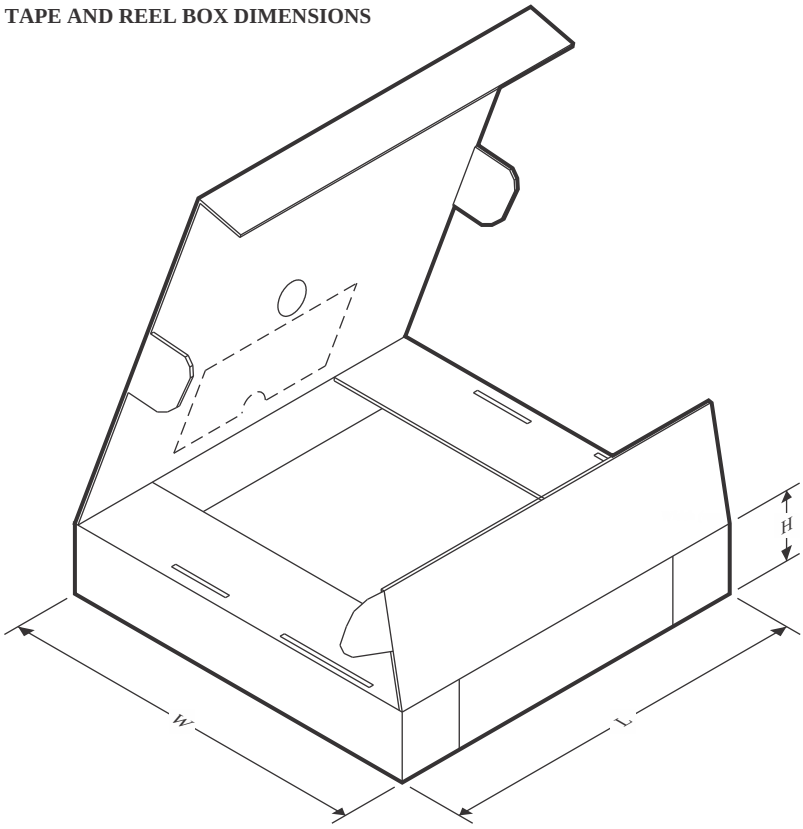
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HVDA1040AQDSJRQ1	VSON	DSJ	12	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
SN65HVDA1040AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

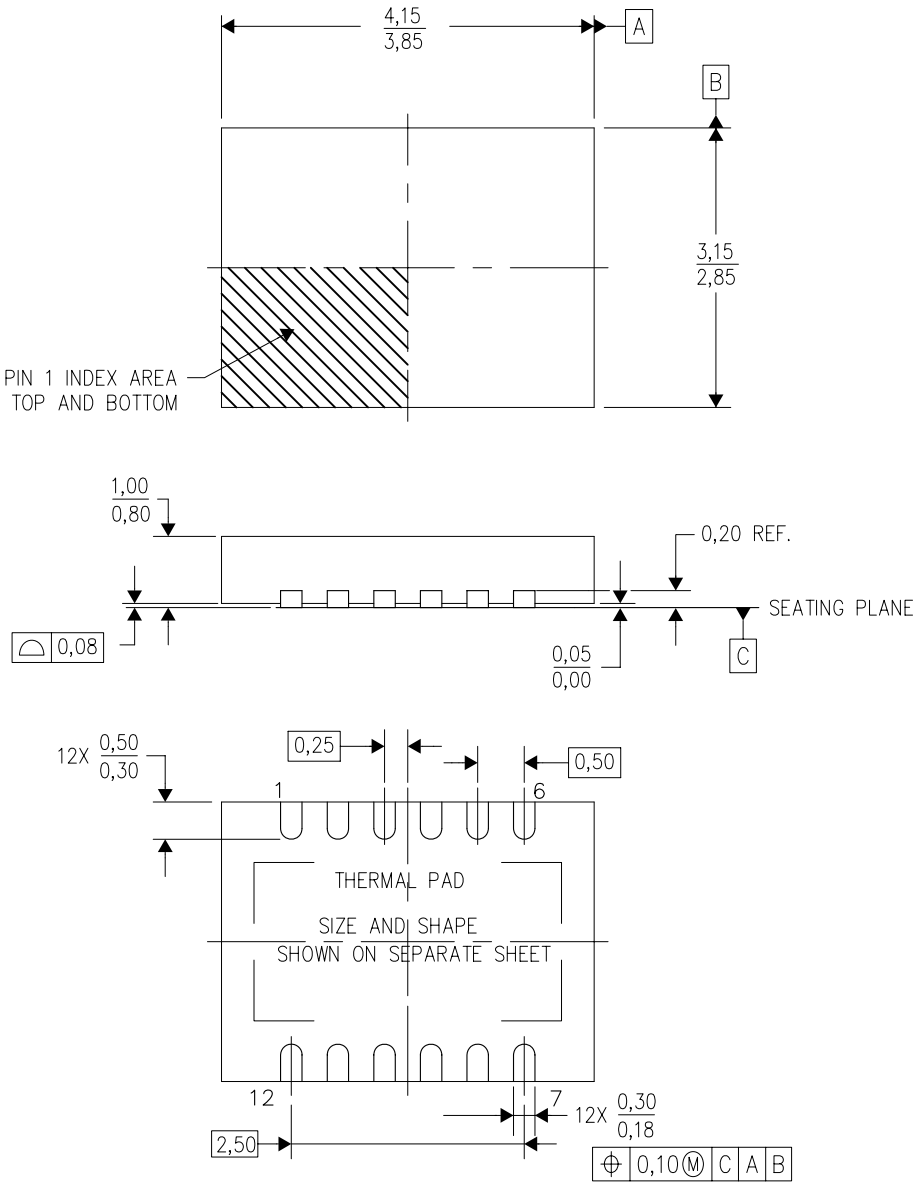
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HVDA1040AQDSJRQ1	VSON	DSJ	12	3000	356.0	356.0	35.0
SN65HVDA1040AQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

DSJ (R–PVSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–229.

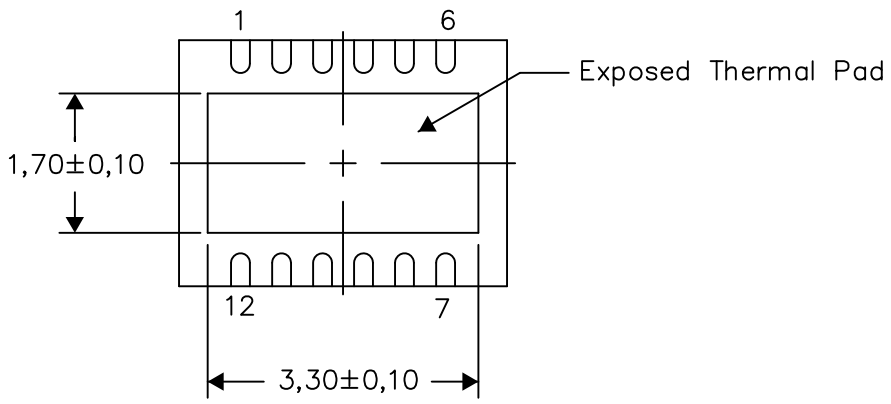
DSJ (R–PVSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



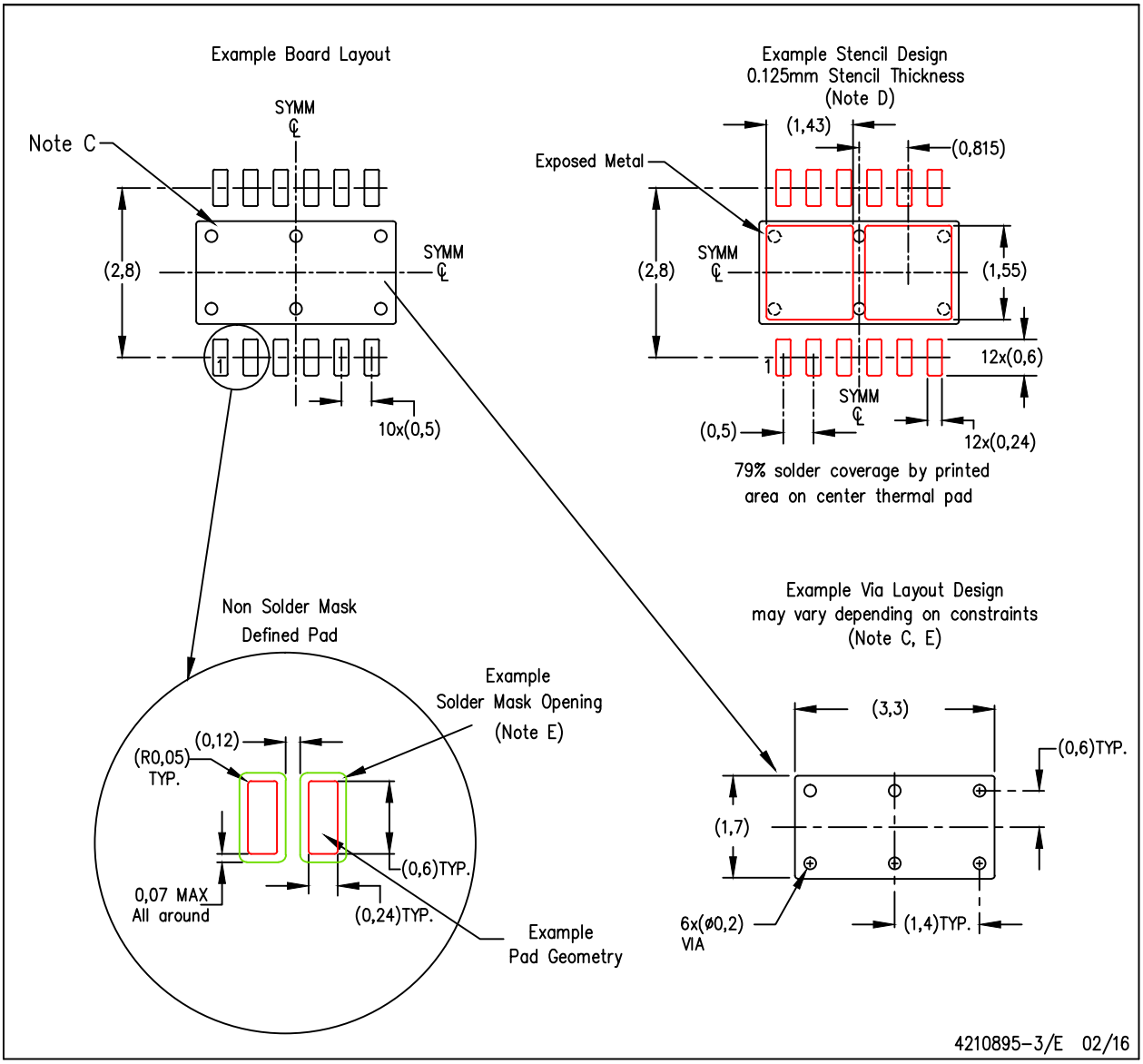
Bottom View

Exposed Thermal Pad Dimensions

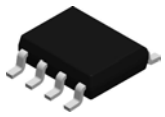
4208549–2/G 04/15

NOTE: All linear dimensions are in millimeters

DSJ (R–PVSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

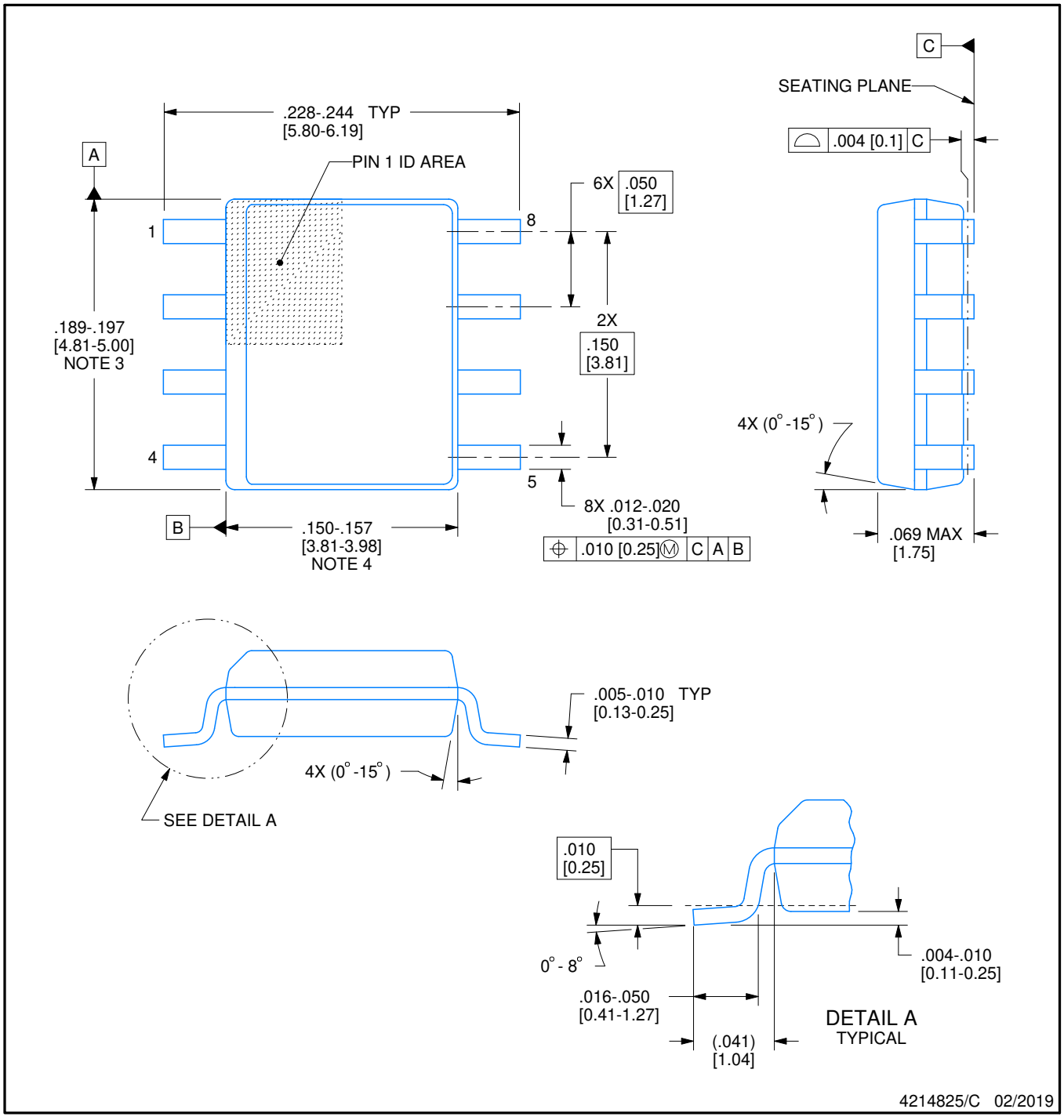


PACKAGE OUTLINE

D0008A

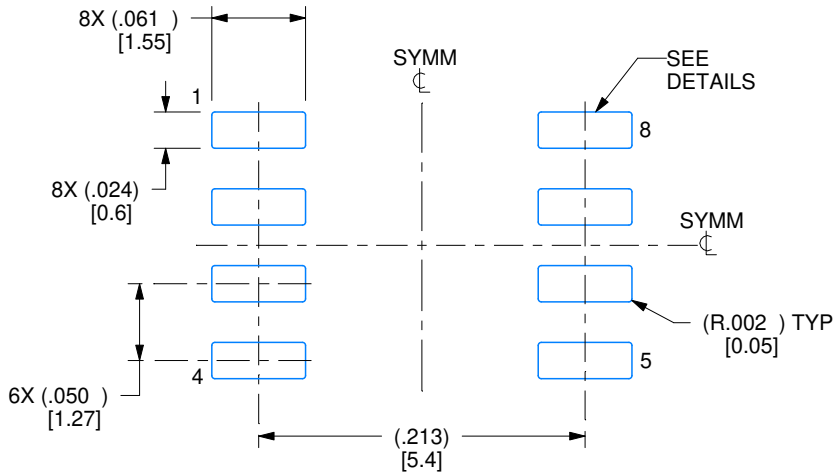
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

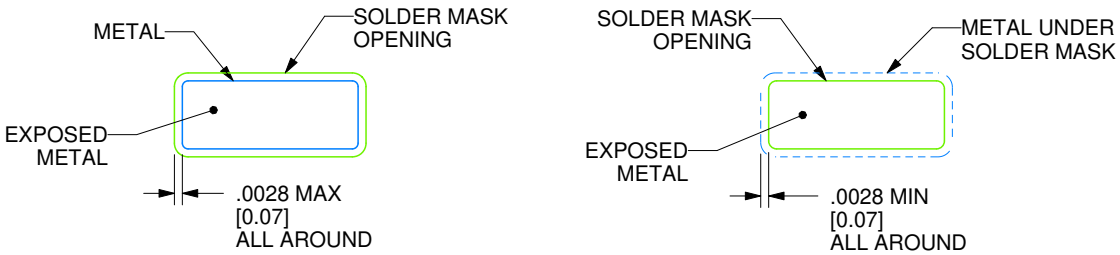


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

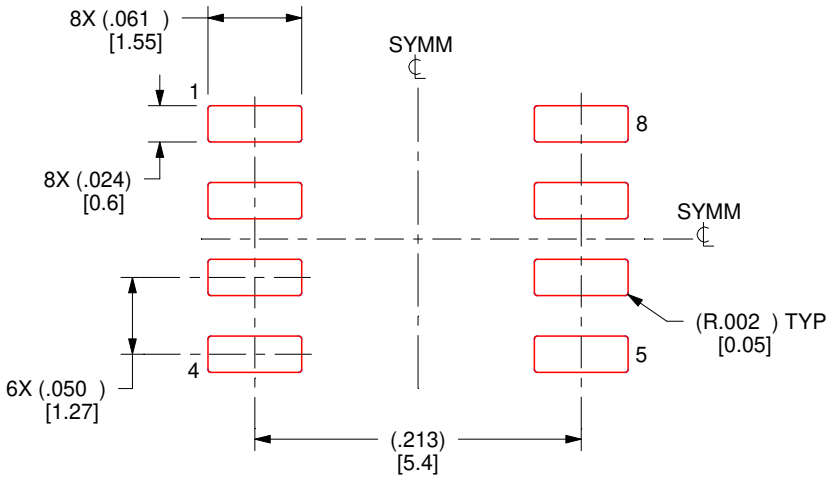
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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