

# LTC4372, LTC4373 Low Quiescent Current Dual Ideal Diodes

## DESCRIPTION

The DC2969A circuit board enables evaluation of the [LTC®4372](#) and [LTC4373](#) low quiescent current ideal diode controllers. The DC2969A-A option is assembled with the LTC4372 controller, whereas DC2969A-B is assembled with the LTC4373 controller. DC2969A includes two independent ideal diode circuits sharing a common ground, operating over a 2.5V to 33V range, and protecting the load against reverse inputs of up to -28V. One of these

circuits includes a high side load switch in series with the ideal diode allowing load on/off control with the SHDN/UV jumper. In addition, input dropouts are blocked from the output, permitting capacitors to hold up the load when input power fails. Each channel can carry up to 20A.

[Design files for this circuit board are available.](#)

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## PERFORMANCE SUMMARY Specifications are at T<sub>A</sub> = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Limits	VIN Operating	2.5		33	V
	VINA DC Survival	-28		50	V
	VINB DC Survival	-28		36	V
Undervoltage Threshold (DC2969A-B VINB Only)	VINB Rising	2.80	3	3.20	V
	VINB Falling	2.35	2.5	2.65	V
Output Current	2.5V ≤ VIN ≤ 5V			10	A
	5V < VIN ≤ 33V			20	A

## QUICK START PROCEDURE

There are exposed conductors on the bottom of the board, and any banana plugs present will protrude through the bottom of the board. Even though the board is equipped with standoffs, the underlying surface should be non-conductive and clear of any wire, solder, and other conductive debris.

A simple demonstration of DC2969A's operation is as follows:

1. Position the two SHDN/UV jumpers to enable both channels: LO for DC2969A-A, HI for DC2969A-B.
2. Connect two adjustable power supplies, initially turned off or set to 0V. Connect one supply to VINA and nearby GND, the second to VINB and its associated GND (see Figure 1). Join the outputs of VOUTA and VOUTB at the input of a 10A capable DC load, initially turned off or set to 0A.
3. Adjust one power supply to 12V. Set the DC load to 10A. Check that the output is roughly within 50mV of the input.
4. Slowly adjust the other power supply up and down relative to the first while monitoring the power supply currents. The higher supply will carry the load current, with a narrow transition region where the input voltages are nearly identical and the supplies droop share. If one supply is turned off or shorted, the output voltage will not collapse—the other supply will carry the load.
5. Each channel can be individually controlled by its associated SHDN/UV jumper. For example, if VINB is adjusted to 12V and VINA is set to 10V, VINB supply will source the entire load current. If SHDNB/UVB jumper is subsequently set to HI for DC2969A-A or LO for DC2969A-B, channel B will turn off and the full load current will be provided by channel A. Note that turning off channel A through the SHDNA/UVA jumper only turns off the M1A MOSFET channel; the M1A body diode always provides a parallel current path. Do not flow more than 2A through the MOSFET body diode, else M1A may heat up to destruction. Positioning channel B jumper at DIV (DC2969A-B only) provides a 3V rising and 2.5V falling undervoltage lockout threshold on VINB. Unless the SHDNB/UVB turret is being driven, do not use DIV position for DC2969A-A as it floats the SHDN pin.
6. Dial any supply below ground up to -28V and check that the output voltage is limited to roughly -1V.

## BOARD DESCRIPTION

### Overview

DC2969A features two independent LTC4372 or LTC4373 ideal diode circuits sharing a common ground. Each channel handles up to 20A at room temperature with no air flow. The board has 2oz copper on the outer layers. Reference designators are duplicated for the two sections of the board; the upper section is suffixed A while the lower section is suffixed B. Universal footprints have been provided (on both outer layers) for the MOSFETs to accommodate power SO8, DPAK, and D2PAK packages. Probe pads have been provided for circuit nodes without turrets.

Below is a brief description of the main components of DC2969A. Components without an A or B suffix refer to both channels.

### U1 – Ideal Diode Controller

U1 is LTC4372 for DC2969A-A and LTC4373 for DC2969A-B, both in an 8-pin MSOP package. Please refer to the controller datasheets for details on their operation.

### M1 – Ideal Diode MOSFET

M1 is the Infineon N-channel MOSFET BSC026N08NS5 in a SuperSO8 package. It was selected for its 80V drain-source breakdown voltage,  $\pm 20V V_{GS(max)}$ , and  $2.2m\Omega$  drain-source on-state resistance (at  $10V V_{GS}$ ). M1's  $\pm 20V V_{GS(max)}$  is protected by the ideal diode controller's internal GATE-to-SOURCE 11.7V clamp. When input is at  $-28V$  and output is at 33V, M1's drain-source is at 61V, safely below its 80V breakdown. During a supply short-circuit to ground with parasitic wire inductance to the IN/SOURCE pins, these pins can swing all the way down to  $-40V$ . If output is held up at 33V by load capacitors, M1 drain-source is subject to 73V, which is also safely below its 80V breakdown.

At 20A load current and  $V_{IN} > 5V$ , the forward drop across M1 will be 44mV and power dissipation will be 0.88W. For  $V_{IN} \leq 5V$ , the controller gate drive drops to 6.5V and M1  $R_{DS(ON)}$  increases to  $3m\Omega$ , yielding 30mV forward drop and 0.3W power dissipation at 10A. Note that these

calculations use typical on-resistance at  $25^\circ C$  and do not consider MOSFET self-heating. Since MOSFET  $R_{DS(ON)}$  rises sharply as gate drive falls to 4.5V, be cautious while operating below 5V input since a combination of low U1 gate drive and high M1 threshold voltage may cause excessive MOSFET power dissipation.

### M2B – Switch MOSFET

M2B is the Nexperia N-channel MOSFET PSMN1R7-60BS in a 3-lead D2PAK package. It was selected for its 60V drain-source breakdown voltage,  $\pm 20V V_{GS(max)}$ , large safe operating area (SOA), and  $1.66m\Omega$  drain-source on-state resistance (at  $10V V_{GS}$ ). M2B's  $\pm 20V V_{GS(max)}$  is protected by the ideal diode controller's internal GATE-to-SOURCE 11.7V clamp. When input is at 33V and output is at 0V, M2B's drain-source is at 33V, safely below its 60V breakdown. Care should be taken when turning on into an output capacitor or load current that the M2B inrush power dissipation is within its SOA.

At 20A load current and  $V_{IN} > 5V$ , the forward drop across M2B is 33mV and power dissipation is 0.66W. For  $V_{IN} \leq 5V$ , the controller gate drive drops to 6.5V and M2B  $R_{DS(ON)}$  increases to  $2m\Omega$ , yielding 20mV forward drop and 0.2W power dissipation at 10A. Note that these calculations use typical on-resistance at  $25^\circ C$  and do not consider MOSFET self-heating. Since MOSFET  $R_{DS(ON)}$  rises sharply as gate drive falls to 4.5V, be cautious while operating below 5V input since a combination of low U1 gate drive and high M2B threshold voltage may cause excessive MOSFET power dissipation.

### CGB – Switch Gate Capacitor

A 10nF CGB capacitor is installed to slow down GATEB ramp up rate. This reduces the inrush current into the output load capacitor to  $C_L \cdot I_{GATE(UP)} / C_{GATE}$ , where  $I_{GATE(UP)}$  is the GATE pull-up current provided by the ideal diode controller (20 $\mu A$ ) and  $C_{GATE}$  is a combination of M2B's  $C_{RSS}$  (0.6nF) and the external CGB (10nF). GATEB ramp rate calculates to 1.9V/ms, yielding 190mA inrush current per 100 $\mu F$  of output capacitance.

## BOARD DESCRIPTION

### D1 to D3 – Input and Output TVS

D2B and D3B clamping voltages are chosen to accommodate normal operating voltage on the input and output while limiting any voltage transients below the controller's and MOSFET's absolute maximum ratings. D1, D2A, and D3A are not installed.

### JP1 – Enable/Off Control

This jumper controls whether the MOSFET channel is forced off or the ideal diode control is enabled (see Table 1). Enabled doesn't imply MOSFET turn-on since that depends on VIN to VOUT differential voltage being above the controller's 30mV turn-on threshold. Note that when M1A is forced off, there is still a parallel current path through its inherent body diode. To avoid M1A damage, do not pass more than 2A through its body diode.

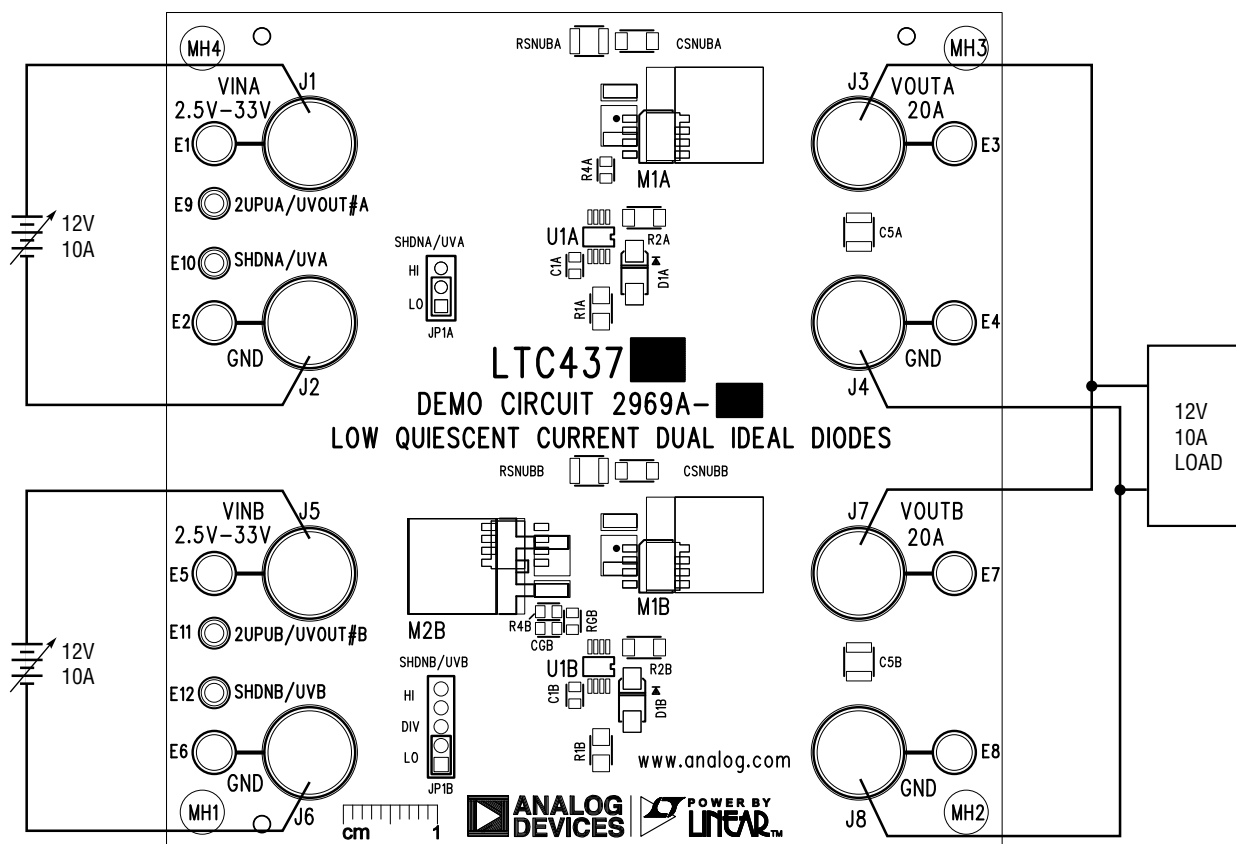
Table 1. Jumper Setting

Jumper Position	DC2969A-A (LTC4372 SHDN)	DC2969A-B (LTC4373 UV)
JP1A = HI	M1A Off	M1A Enabled
= LO	M1A Enabled	M1A Off
JP1B = HI	M1B & M2B Off	M1B & M2B Enabled
= DIV	Floats SHDN!	VINB 2.5V/3V UV
= LO	M1B & M2B Enabled	M1B & M2B Off

### Optional Components

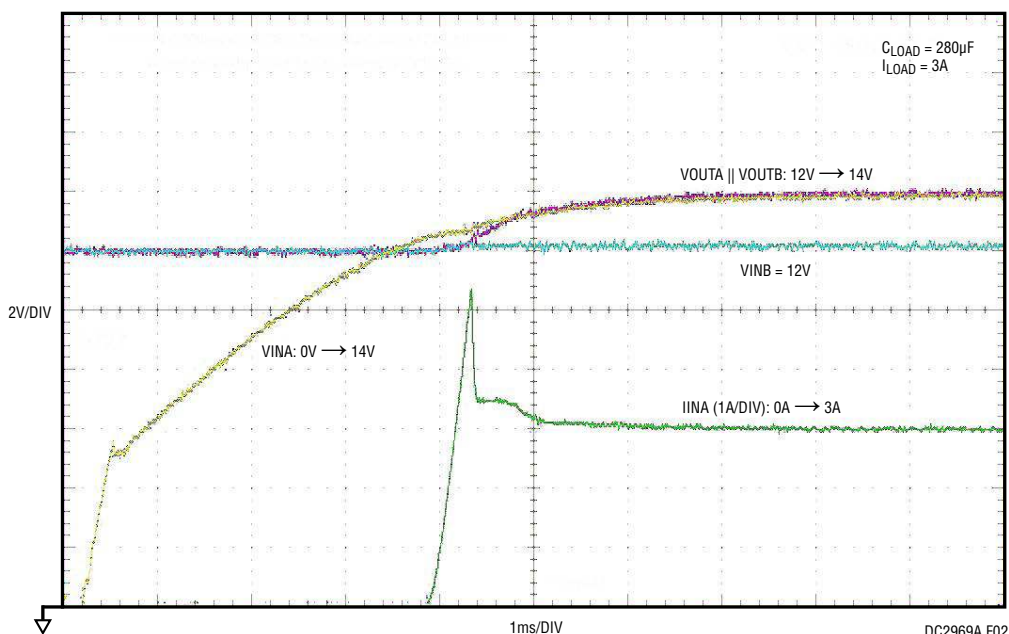
Pads for optional (or uninstalled) components have been provided on the board to try out other circuits from the controller datasheet.

## SCHEMATIC DIAGRAM



DC2969A F01

Figure 1. Measurement Equipment Setup



DC2969A F02

Figure 2. VINA and VINB Ideal Diode-OR: VINB is at 12V while VINA turns on from 0V to 14V



## ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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