VC707 Evaluation Board for the Virtex-7 FPGA

User Guide

UG885 (v1.8) February 20, 2019

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/05/12	1.0	Initial Xilinx release.
10/08/12	1.1	Chapter 1, VC707 Evaluation Board Features: In Table 1-1, notes for J37 changed to Samtec ASP_134486_01. The board photo in Figure 1-2 was replaced. In Table 1-3, GPGA (U1) Bank 32 was deleted. A note was added about the user clock for Figure 1-10. In Table 1-15, FPGA pin AN1 changed to AM4 and pin AN2 changed to AM3. In SGMII GTX Transceiver Clock Generation, 25 MHz LVDS clock changed to 125 MHz LVDS clock. The Figure 1-10 title also changed from 25 MHz to 125 MHz. In Table 1-23, pin AR42 changed to AT42. In Figure 1-33, switching regulator supply voltage UG63 for MGTVCCAUX was updated. In Table 1-29, device type PTD08D021W (V_{OUT} A) power rail voltage changed to 1.80V. In Table 1-32, values for rail number 3 changed. In Appendix C, Xilinx Constraints File, the entire listing was replaced. Appendix F, Regulatory and Compliance Information now includes a link to the Declaration of Conformity and markings for waste electrical and electronic equipment (WEEE), restriction of hazardous substances (RoHS), and CE compliance.

Date	Version	Revision
02/01/13	1.2	Updated VC707 Board Features, Table 1-1, Virtex-7 XC7VX485T-2FFG1761C FPGA, FPGA Configuration, USB JTAG, System Clock (SYSCLK_P and SYSCLK_N), HDMI Video Output, I2C Bus, Table 1-15, User I/O, Table 1-26, Power Management, and VITA 57.1 FMC2 HPC Connector (Partially Populated). Updated Figure 1-5, Figure 1-16, and Figure 1-25. Updated paragraph following Table 1-4, Figure 1-7, Figure 1-19, Figure 1-20, and Table 1-24. Added CPU Reset Pushbutton, User Rotary Switch, User SMA, and PCIe Form Factor Board TI Power System Cooling. Added Table 1-27 and Table 1-28. Replaced PTD08D021W with PTD08D210W in Table 1-29. Added third paragraph to the introduction in Appendix C, Xilinx Constraints File. Added UG483 and removed NXP Semiconductors in Appendix G, Additional Resources. Added second paragraph to the introduction in Appendix F, Regulatory and Compliance Information.
08/22/13	1.3	Updated Figure 1-2, Table 1-1, Table 1-12, Table 1-13, and Table 1-14. Updated Linear BPI Flash Memory. Replaced Master UCF Listing with Appendix C, Xilinx Constraints File.
05/12/14	1.4	Updated disclaimer and copyright. In Table 1-27, changed U1 FPGA pin N39 to M39, B36 to A35, and B37 to A36.
09/20/14	1.5	Added note to Table 1-1 and Table 1-27. Updated Table 1-7. Changed Net Name column heading to FHG1761 Placement in Table 1-11. Added I/O standard information to Table 1-4, Table 1-5, Table 1-8, Table 1-10, Table 1-18, Table 1-21, Table 1-23, Table 1-26, Table 1-27 and Table 1-28. Updated schematic net name for pins C34 and D35 in Table 1-27 and Table 1-28. Updated GTX Transceivers. Added Figure A-3.
04/07/15	1.6	Added notes to Jitter Attenuated Clock and I2C Bus. Updated Table 1-24. Deleted redundant Figure B-2 FMC2 HPC Connector Pinout in Appendix B, VITA 57.1 FMC Connector Pinouts. Added information for ordering the ATX power supply adapter cable.
09/01/15	1.6.1	Made typographical edits.
03/26/16	1.7	Updated transceiver bank MGT_BANK_119 in Table 1-11. Updated GPIO pin for CPU reset pushbutton switch in Table 1-26. Updated U1 FPGA pins for J37 FMC2 HPC pins B12, B13, B32, and B33 in Table 1-28. Added thickness information in Appendix E, Board Specifications.
08/12/16	1.7.1	Made a typographical edit.
02/20/19	1.8	Added the latest version of ESD Directive in Chapter 1, Electrostatic Discharge Caution. Updated the description of Chapter 1, DDR3 Memory. Updated the U1 FPGA Pin for F31 and F32 in Table 1-28. In Appendix C, Xilinx Constraints File changed the title of the appendix, updated the description and removed the VC707 Board XDC Listing. Updated Appendix F, Regulatory and Compliance Information. Updated Appendix G, References

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Appendix B: VITA 57.1 FMC Connector Pinouts

Appendix C: Xilinx Constraints File

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Chapter 1

VC707 Evaluation Board Features

Overview

The VC707 evaluation board for the Virtex®-7 FPGA provides a hardware environment for developing and evaluating designs targeting the Virtex-7 XC7VX485T-2FFG1761C FPGA. The VC707 board provides features common to many embedded processing systems, including a DDR3 SODIMM memory, an 8-lane PCI Express® interface, a tri-mode Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be added by using mezzanine cards attached to either of two VITA-57 FPGA mezzanine connectors (FMC) provided on the board. Two high pin count (HPC) FMCs are provided. See VC707 Board Features for a complete list of features. The details for each feature are described in Feature Descriptions.

Additional Information

See Appendix G, Additional Resources for references to documents, files and resources relevant to the VC707 board.

VC707 Board Features

- Virtex-7 XC7VX485T-2FFG1761C FPGA
- 1 GB DDR3 memory SODIMM
- 128 MB Linear byte peripheral interface (BPI) Flash memory
- USB 2.0 ULPI Transceiver
- Secure Digital (SD) connector
- USB JTAG through Digilent module
- Clock Generation
    - Fixed 200 MHz LVDS oscillator (differential)
    - I^2C programmable LVDS oscillator (differential)
    - SMA connectors (differential)
    - SMA connectors for GTX transceiver clocking
- GTX transceivers
    - FMC1 HPC connector (eight GTX transceivers)
    - FMC2 HPC connector (eight GTX transceiver)
    - SMA connectors (one pair each for TX, RX, and REFCLK)
    - PCI Express (eight lanes)
    - Small form-factor pluggable plus (SFP+) connector
    - Ethernet PHY SGMII interface (RJ-45 connector)

- PCI Express endpoint connectivity
  - Gen1 8-lane (x8)
  - Gen2 8-lane (x8)
- SFP+ Connector
- 10/100/1000 tri-speed Ethernet PHY
- USB-to-UART bridge
- HDMI™ codec
- I^2C bus
  - I^2C MUX
  - I^2C EEPROM (1 KB)
  - USER I^2C programmable LVDS oscillator
  - DDR3 SODIMM socket
  - HDMI codec
  - FMC1 HPC connector
  - FMC2 HPC connector
  - SFP+ connector
  - I^2C programmable jitter-attenuating precision clock multiplier
- Status LEDs
  - Ethernet status
  - Power good
  - FPGA INIT
  - FPGA DONE
- User I/O
  - User LEDs (eight GPIO)
  - User pushbuttons (five directional)
  - CPU reset pushbutton
  - User DIP switch (8-pole GPIO)
  - User SMA GPIO connectors (one pair)
  - LCD character display (16 characters x 2 lines)
- Switches
  - Power on/off slide switch
  - FPGA_PROB_B pushbutton
  - Configuration mode DIP switch
- VITA 57.1 FMC1 HPC Connector
- VITA 57.1 FMC2 HPC Connector
- Power management
  - PMBus voltage and current monitoring through TI power controller
- XADC header
- Configuration options
  - Linear BPI Flash memory

- USB JTAG configuration port
- Platform cable header JTAG configuration port

The VC707 board block diagram is shown in Figure 1-1. The VC707 board schematics are available for download from the VC707 Evaluation Kit product page on the Docs & Designs tab at www.xilinx.com/vc707.

Electrostatic Discharge Caution

Caution! ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.

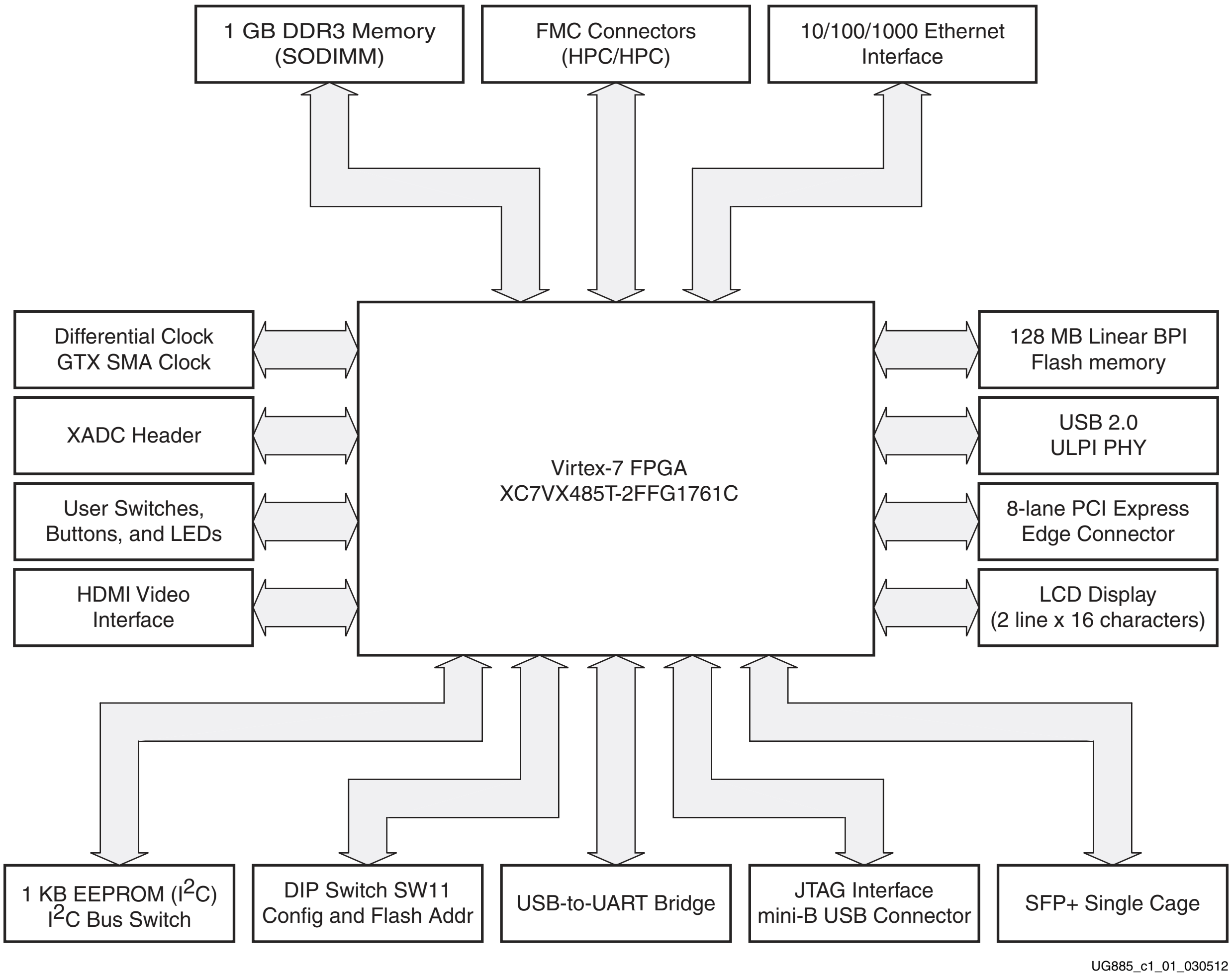

Figure 1-1: **VC707 Board Block Diagram**

Feature Descriptions

Figure 1-2 shows the VC707 board. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

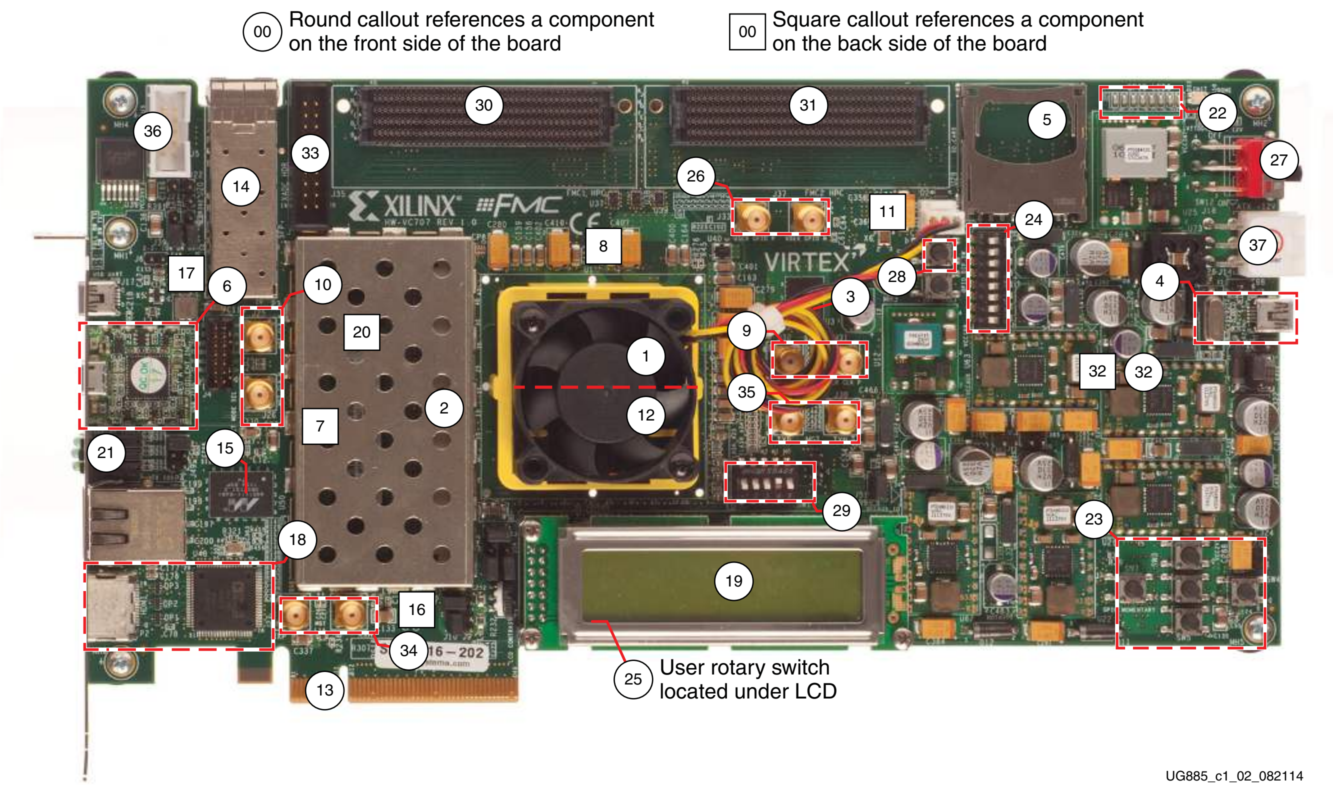

Figure 1-2: **VC707 Board Component Locations**

Table 1-1: **VC707 Board Component Descriptions**

Callout	Reference Designator	Component Description	Notes	Schematic 0381418 Page Number
1	U1	Virtex-7 FPGA with cooling fan	XC7VX485T-2FFG1761C	
2	J1	DDR3 SODIMM memory (1 GB)	Micron MT8JTF12864HZ-1G6G1	21
3	U3	BPI parallel NOR flash memory (1 Gb)	Micron PC28F00AG18FE	35
4	U8, J2	USB ULPI transceiver, USB mini-B connector	SMSC USB3320-EZK	44
5	U29	SD card interface connector	Molex 67840-8001	37
6	U26	USB JTAG interface, USB micro-B connector	Digilent USB JTAG module	20
7	U51	System clock, 200 MHz, LVDS (back side of board)	SiTime SIT9102-243N25E200.0000	32

Table 1-1: **VC707 Board Component Descriptions *(Cont'd)***

Callout	Reference Designator	Component Description	Notes	Schematic 0381418 Page Number
8	U34	I^2C programmable user clock LVDS, 156.250 MHz default frequency (back side of board)	Silicon Labs SI570BAB0000544DG	32
9	J31, J32	User SMA clock	Rosenberger 32K10K-400L5	32
10	J25, J26	GTX transceiver SMA reference clock	Rosenberger 32K10K-400L5	32
11	U24	Jitter attenuated clock (back side of board)	Silicon Labs SI5324C-C-GM	33
12		GTX transceiver Quad 111 – Quad 119	Embedded within FPGA U1	12 – 15
13	P1	PCI Express connector	8-lane card edge connector	30
14	P3	SFP/SFP+ module connector	Molex 74441-0010	31
15	U50	10/100/1000 Mb/s Ethernet PHY	Marvell M88E1111-BAB1C000	34
16	U2	SGMII GTX transceiver clock generator	ICS ICS84402IAGI-01LF	32
17	U44	USB-to-UART bridge	Silicon Labs CP2103GM	36
18	P2, U48	HDMI video connector, HDMI controller	Molex 500254-1927, AD ADV7511KSTZ-P	43, 42
19	J23	LCD character display and connector	2 x 7 0.1 inch male header	39
20	U52	I^2C Bus Switch (back side of board)	TI PCA9548ARGER	41
21	DS11–DS13	Ethernet status LEDs	EPHY status LED, dual green	34
22	DS2–DS9	User LEDs	GPIO LEDs, green 0603	38
23	SW3–SW7	User pushbuttons, active-High	E-Switch TL3301EP100QG	38
24	SW2	User DIP Switch	8-pole C and K SDA08H1SBD	38
25	SW10	User rotary switch (under LCD assembly)	Panasonic EVQ-WK4001	38
26	J33, J34	User SMA GPIO	Rosenberger 32K10K-400L5	32
27	SW12	Power on/off switch	C&K 1201M2S3AQE2	45
28	SW9	FPGA PROG pushbutton	E-Switch TL3301EP100QG	38
29	SW11	Config mode/upper linear flash address dip switch	5-pole C&K SDA05H1IBD	36
30	J35	FMC HPC1 connector (J35)	Samtec ASP_134486_01	22–25
31	J37	FMC HPC2 connector (J37)	Samtec ASP_134486_01	26–29
32		Power management system (front and back side of board)	TI UCD9248PFC in conjunction with various regulators	45–55
33	J19	Xilinx XADC header	2 x 10 0.1inch male header	40
34	J27, J28	GTX receiver SMA (RX)	Rosenberger 32K10K-400L5	32
35	J29/J30	GTX transmitter SMA (TX)	Rosenberger 32K10K-400L5	32
36	J5	2 x 5 shrouded PMBus connector	Assman HW10G-0202	46
37	J18	12V power input 2 x 3 connector	Molex 39-30-1060	46

Notes:

1. Jumper header locations are identified in Appendix A, Default Switch and Jumper Settings.

Virtex-7 XC7VX485T-2FFG1761C FPGA

[Figure 1-2, callout 1]

The VC707 board is populated with the Virtex-7 XC7VX485T-2FFG1761C FPGA.

For further information on Virtex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 1], and *7 Series FPGAs Packaging and Pinout Product Specifications User Guide* (UG475) [Ref 14].

To determine the type of FPGA resident on the VC707 board, refer to the Master Answer Record listed in Appendix G: References.

FPGA Configuration

The VC707 board supports two of the five 7 series FPGA configuration modes:

- Master BPI using the onboard Linear BPI Flash memory
- JTAG using a type-A to micro-B USB cable for connecting the host PC to the VC707 board configuration port

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-2. The mode switches M2, M1, and M0 are on SW11 positions 3, 4, and 5 respectively as shown in Figure 1-3.

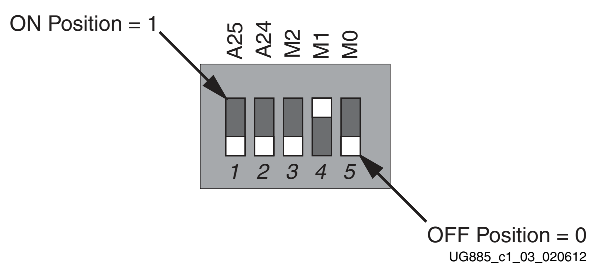

Figure 1-3: **SW11 Default Settings**

The default mode setting is M[2:0] = `010`, which selects Master BPI at board power-on. See Configuration Options for detailed information about the mode switch SW11.

Table 1-2: **VC707 Board FPGA Configuration Modes**

Configuration Mode	SW13 DIP switch Settings (M[2:0])	Bus Width	CCLK Direction
Master BPI	`010`	x8, x16	Output
JTAG	`101`	x1	Not Applicable

For full details on configuring the FPGA, see *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3].

I/O Voltage Rails

There are 17 I/O banks available on the Virtex-7 device. Sixteen I/O banks are available on the VC707 board, bank 31 is not used. The voltages applied to the FPGA I/O banks used by the VC707 board are listed in Table 1-3.

Table 1-3: **I/O Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8_FPGA	1.8V
Bank 13	VCC1V8_FPGA	1.8V
Bank 14	VCC1V8_FPGA	1.8V
Bank 15	VCC1V8_FPGA	1.8V
Bank 16(1)	VADJ_FPGA	1.8V (default)
Bank 17(1)	VADJ_FPGA	1.8V (default)
Bank 18(1)	VADJ_FPGA	1.8V (default)
Bank 19(1)	VADJ_FPGA	1.8V (default)
Bank 31	NOT USED	NA
Bank 33	VCC1V8_FPGA	1.8V
Bank 34	VADJ_FPGA	1.8V (default)
Bank 35	VADJ_FPGA	1.8V (default)
Bank 36	FMC1_VIO_B_M2C	Variable
Bank 37	VCC1V5_FPGA	1.5V
Bank 38	VCC1V5_FPGA	1.5V
Bank 39	VCC1V5_FPGA	1.5V

Notes:

1. The VADJ_FPGA rail can support up to 1.8V due to FPGA HP bank connections to FMC. For more information on VADJ_FPGA see Power Management.

DDR3 Memory

[Figure 1-2, callout 2]

The memory module at J1 is a 1 GB DDR3 small outline dual-inline memory module (SODIMM). It provides volatile synchronous dynamic random access memory (SDRAM) for storing user code and data.

- Part number: MT8JTF12864HZ-1G6G1 (Micron Technology)
- Supply voltage: 1.5V
- Configuration: 1GB (128 Mb x 64)
- Datapath width: 64 bits
- Data rate: Up to 1,600 MT/s

The VC707 XC7VX485T FPGA memory interface performance is documented in the *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics* (DS183) [Ref 2].

The DDR3 interface is implemented across I/O banks 37, 38, and 39. Each bank is a 1.5V high-performance bank having a dedicated DCI VRP/N resistor connection. An external 0.75V reference VTTREF is provided for data interface banks 37 and 39. Any interface connected to these banks that requires a reference voltage must use this FPGA voltage reference. The connections between the DDR3 memory and the FPGA are listed in Table 1-4.

Table 1-4: **DDR3 Memory Connections to the FPGA**

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
A20	DDR3_A0	SSTL15	98	A0
B19	DDR3_A1	SSTL15	97	A1
C20	DDR3_A2	SSTL15	96	A2
A19	DDR3_A3	SSTL15	95	A3
A17	DDR3_A4	SSTL15	92	A4
A16	DDR3_A5	SSTL15	91	A5
D20	DDR3_A6	SSTL15	90	A6
C18	DDR3_A7	SSTL15	86	A7
D17	DDR3_A8	SSTL15	89	A8
C19	DDR3_A9	SSTL15	85	A9
B21	DDR3_A10	SSTL15	107	A10/AP
B17	DDR3_A11	SSTL15	84	A11
A15	DDR3_A12	SSTL15	83	A12_BC_N
A21	DDR3_A13	SSTL15	119	A13
F17	DDR3_A14	SSTL15	80	A14
E17	DDR3_A15	SSTL15	78	A15
D21	DDR3_BA0	SSTL15	109	BA0
C21	DDR3_BA1	SSTL15	108	BA1

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
D18	DDR3_BA2	SSTL15	79	BA2
N14	DDR3_D0	SSTL15	5	DQ0
N13	DDR3_D1	SSTL15	7	DQ1
L14	DDR3_D2	SSTL15	15	DQ2
M14	DDR3_D3	SSTL15	17	DQ3
M12	DDR3_D4	SSTL15	4	DQ4
N15	DDR3_D5	SSTL15	6	DQ5
M11	DDR3_D6	SSTL15	16	DQ6
L12	DDR3_D7	SSTL15	18	DQ7
K14	DDR3_D8	SSTL15	21	DQ8
K13	DDR3_D9	SSTL15	23	DQ9
H13	DDR3_D10	SSTL15	33	DQ10
J13	DDR3_D11	SSTL15	35	DQ11
L16	DDR3_D12	SSTL15	22	DQ12
L15	DDR3_D13	SSTL15	24	DQ13
H14	DDR3_D14	SSTL15	34	DQ14
J15	DDR3_D15	SSTL15	36	DQ15
E15	DDR3_D16	SSTL15	39	DQ16
E13	DDR3_D17	SSTL15	41	DQ17
F15	DDR3_D18	SSTL15	51	DQ18
E14	DDR3_D19	SSTL15	53	DQ19
G13	DDR3_D20	SSTL15	40	DQ20
G12	DDR3_D21	SSTL15	42	DQ21
F14	DDR3_D22	SSTL15	50	DQ22
G14	DDR3_D23	SSTL15	52	DQ23
B14	DDR3_D24	SSTL15	57	DQ24
C13	DDR3_D25	SSTL15	59	DQ25
B16	DDR3_D26	SSTL15	67	DQ26
D15	DDR3_D27	SSTL15	69	DQ27
D13	DDR3_D28	SSTL15	56	DQ28
E12	DDR3_D29	SSTL15	58	DQ29
C16	DDR3_D30	SSTL15	68	DQ30

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
D16	DDR3_D31	SSTL15	70	DQ31
A24	DDR3_D32	SSTL15	129	DQ32
B23	DDR3_D33	SSTL15	131	DQ33
B27	DDR3_D34	SSTL15	141	DQ34
B26	DDR3_D35	SSTL15	143	DQ35
A22	DDR3_D36	SSTL15	130	DQ36
B22	DDR3_D37	SSTL15	132	DQ37
A25	DDR3_D38	SSTL15	140	DQ38
C24	DDR3_D39	SSTL15	142	DQ39
E24	DDR3_D40	SSTL15	147	DQ40
D23	DDR3_D41	SSTL15	149	DQ41
D26	DDR3_D42	SSTL15	157	DQ42
C25	DDR3_D43	SSTL15	159	DQ43
E23	DDR3_D44	SSTL15	146	DQ44
D22	DDR3_D45	SSTL15	148	DQ45
F22	DDR3_D46	SSTL15	158	DQ46
E22	DDR3_D47	SSTL15	160	DQ47
A30	DDR3_D48	SSTL15	163	DQ48
D27	DDR3_D49	SSTL15	165	DQ49
A29	DDR3_D50	SSTL15	175	DQ50
C28	DDR3_D51	SSTL15	177	DQ51
D28	DDR3_D52	SSTL15	164	DQ52
B31	DDR3_D53	SSTL15	166	DQ53
A31	DDR3_D54	SSTL15	174	DQ54
A32	DDR3_D55	SSTL15	176	DQ55
E30	DDR3_D56	SSTL15	181	DQ56
F29	DDR3_D57	SSTL15	183	DQ57
F30	DDR3_D58	SSTL15	191	DQ58
F27	DDR3_D59	SSTL15	193	DQ59
C30	DDR3_D60	SSTL15	180	DQ60
E29	DDR3_D61	SSTL15	182	DQ61
F26	DDR3_D62	SSTL15	192	DQ62

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
D30	DDR3_D63	SSTL15	194	DQ63
M13	DDR3_DM0	SSTL15	11	DM0
K15	DDR3_DM1	SSTL15	28	DM1
F12	DDR3_DM2	SSTL15	46	DM2
A14	DDR3_DM3	SSTL15	63	DM3
C23	DDR3_DM4	SSTL15	136	DM4
D25	DDR3_DM5	SSTL15	153	DM5
C31	DDR3_DM6	SSTL15	170	DM6
F31	DDR3_DM7	SSTL15	187	DM7
M16	DDR3_DQS0_N	DIFF_SSTL15	10	DQS0_N
N16	DDR3_DQS0_P	DIFF_SSTL15	12	DQS0_P
J12	DDR3_DQS1_N	DIFF_SSTL15	27	DQS1_N
K12	DDR3_DQS1_P	DIFF_SSTL15	29	DQS1_P
G16	DDR3_DQS2_N	DIFF_SSTL15	45	DQS2_N
H16	DDR3_DQS2_P	DIFF_SSTL15	47	DQS2_P
C14	DDR3_DQS3_N	DIFF_SSTL15	62	DQS3_N
C15	DDR3_DQS3_P	DIFF_SSTL15	64	DQS3_P
A27	DDR3_DQS4_N	DIFF_SSTL15	135	DQS4_N
A26	DDR3_DQS4_P	DIFF_SSTL15	137	DQS4_P
E25	DDR3_DQS5_N	DIFF_SSTL15	152	DQS5_N
F25	DDR3_DQS5_P	DIFF_SSTL15	154	DQS5_P
B29	DDR3_DQS6_N	DIFF_SSTL15	169	DQS6_N
B28	DDR3_DQS6_P	DIFF_SSTL15	171	DQS6_P
E28	DDR3_DQS7_N	DIFF_SSTL15	186	DQS7_N
E27	DDR3_DQS7_P	DIFF_SSTL15	188	DQS7_P
H20	DDR3_ODT0	SSTL15	116	ODT0
H18	DDR3_ODT1	SSTL15	120	ODT1
C29	DDR3_RESET_B	LVCMOS15	30	RESET_B
J17	DDR3_S0_B	SSTL15	114	S0_B
J20	DDR3_S1_B	SSTL15	121	S1_B
G17	DDR3_TEMP_EVENT	SSTL15	198	EVENT_B
F20	DDR3_WE_B	SSTL15	113	WE_B

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
K17	DDR3_CAS_B	SSTL15	115	CAS_B
E20	DDR3_RAS_B	SSTL15	110	RAS_B
K19	DDR3_CKE0	SSTL15	73	CKE0
J18	DDR3_CKE1	SSTL15	74	CKE1
G18	DDR3_CLK0_N	DIFF_SSTL15	103	CK0_N
H19	DDR3_CLK0_P	DIFF_SSTL15	101	CK0_P
F19	DDR3_CLK1_N	DIFF_SSTL15	104	CK1_N
G19	DDR3_CLK1_P	DIFF_SSTL15	102	CK1_P

The VC707 DDR3 SODIMM interface adheres to the constraints guidelines in the DDR3 *Design Guidelines* section of *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 4]. The VC707 DDR3 SODIMM interface is a 40Ω impedance implementation. Other memory interface details are available in UG586 and *7 Series FPGAs Memory Resources User Guide* (UG473) [Ref 5]. For more details on the DDR3 SODIMM, see the Micron Semiconductor MT8JTF12864HZ-1G6G1 data sheet [Ref 17].

Linear BPI Flash Memory

[Figure 1-2, callout 3]

The Linear BPI Flash memory located at U3 provides 128 MB of nonvolatile storage that can be used for configuration or software storage. The data, address, and control signals are connected to the FPGA. The BPI Flash memory device is packaged in a 64-pin BGA.

- Part number: PC28F00AG18FE (Micron)
- Supply voltage: 1.8V
- Datapath width: 16 bits (26 address lines and 7 control signals)
- Data rate: Up to 80 MHz

The Linear BPI Flash memory can synchronously configure the FPGA in Master BPI mode at the 80 MHz data rate supported by the PC28F00AG18FE flash memory. The fastest configuration method uses the external 80 MHz oscillator connected to the FPGA's EMCCLK pin.

Multiple bitstreams can be stored in the Linear BPI Flash. The two most significant address bits (A25, A24) of the flash memory are connected to DIP switch SW11 positions 1 and 2 respectively, and to the RS1 and RS0 pins of the FPGA. By placing valid XC7VX485T bitstreams at four different offset addresses in the flash memory, 1 of the 4 bitstreams can be selected to configure the FPGA by appropriately setting the DIP switch SW11. The connections between the BPI Flash memory and the FPGA are listed in Table 1-5.

Table 1-5: **BPI Flash Memory Connections to the FPGA**

FPGA (U1) Pin	Net Name	I/O Standard	BPI Flash Memory (U3)	
			Pin Number	Pin Name
AJ28	FLASH_A0	LVCMOS18	A1	A1
AH28	FLASH_A1	LVCMOS18	B1	A2
AG31	FLASH_A2	LVCMOS18	C1	A3
AF30	FLASH_A3	LVCMOS18	D1	A4
AK29	FLASH_A4	LVCMOS18	D2	A5
AK28	FLASH_A5	LVCMOS18	A2	A6
AG29	FLASH_A6	LVCMOS18	C2	A7
AK30	FLASH_A7	LVCMOS18	A3	A8
AJ30	FLASH_A8	LVCMOS18	B3	A9
AH30	FLASH_A9	LVCMOS18	C3	A10
AH29	FLASH_A10	LVCMOS18	D3	A11
AL30	FLASH_A11	LVCMOS18	C4	A12
AL29	FLASH_A12	LVCMOS18	A5	A13
AN33	FLASH_A13	LVCMOS18	B5	A14
AM33	FLASH_A14	LVCMOS18	C5	A15
AM32	FLASH_A15	LVCMOS18	D7	A16
AV41	FLASH_A16	LVCMOS18	D8	A17
AU41	FLASH_A17	LVCMOS18	A7	A18
BA42	FLASH_A18	LVCMOS18	B7	A19
AU42	FLASH_A19	LVCMOS18	C7	A20
AT41	FLASH_A20	LVCMOS18	C8	A21
BA40	FLASH_A21	LVCMOS18	A8	A22
BA39	FLASH_A22	LVCMOS18	G1	A23
BB39	FLASH_A23	LVCMOS18	H8	A24
AW42	FLASH_A24	LVCMOS18	B6	A25
AW41	FLASH_A25	LVCMOS18	B8	A26
NA	NC	NA	H1	A27
AM36	FLASH_D0	LVCMOS18	F2	DQ0
AN36	FLASH_D1	LVCMOS18	E2	DQ1
AJ36	FLASH_D2	LVCMOS18	G3	DQ2
AJ37	FLASH_D3	LVCMOS18	E4	DQ3
AK37	FLASH_D4	LVCMOS18	E5	DQ4

Table 1-5: **BPI Flash Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	BPI Flash Memory (U3)	
			Pin Number	Pin Name
AL37	FLASH_D5	LVCMOS18	G5	DQ5
AN35	FLASH_D6	LVCMOS18	G6	DQ6
AP35	FLASH_D7	LVCMOS18	H7	DQ7
AM37	FLASH_D8	LVCMOS18	E1	DQ8
AG33	FLASH_D9	LVCMOS18	E3	DQ9
AH33	FLASH_D10	LVCMOS18	F3	DQ10
AK35	FLASH_D11	LVCMOS18	F4	DQ11
AL35	FLASH_D12	LVCMOS18	F5	DQ12
AJ31	FLASH_D13	LVCMOS18	H5	DQ13
AH34	FLASH_D14	LVCMOS18	G7	DQ14
AJ35	FLASH_D15	LVCMOS18	E7	DQ15
AM34	FLASH_WAIT	LVCMOS18	F7	WAIT
BB41	FPGA_FWE_B	LVCMOS18	G8	WE_B
BA41	FLASH_OE_B	LVCMOS18	F8	OE_B
N10	FPGA_CCLK	LVCMOS18	E6	CLK
AL36	FLASH_CE_B	LVCMOS18	B4	CE_B
AY37	FLASH_ADV_B	LVCMOS18	F6	ADV_B
AG11	FPGA_INIT_B	LVCMOS18	D4	RST_B

Additional FPGA bitstreams can be stored and used for configuration by setting the Warm Boot Start Address (WBSTAR) register contained in 7 series FPGAs. More information is available in the reconfiguration and multiboot section in *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3].

The configuration section of *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3] provides details on the Master BPI configuration mode.

Figure 1-4 shows the connections of the linear BPI Flash memory on the VC707 board. For more details, see the Micron PC28F00AG18FE data sheet [Ref 17].

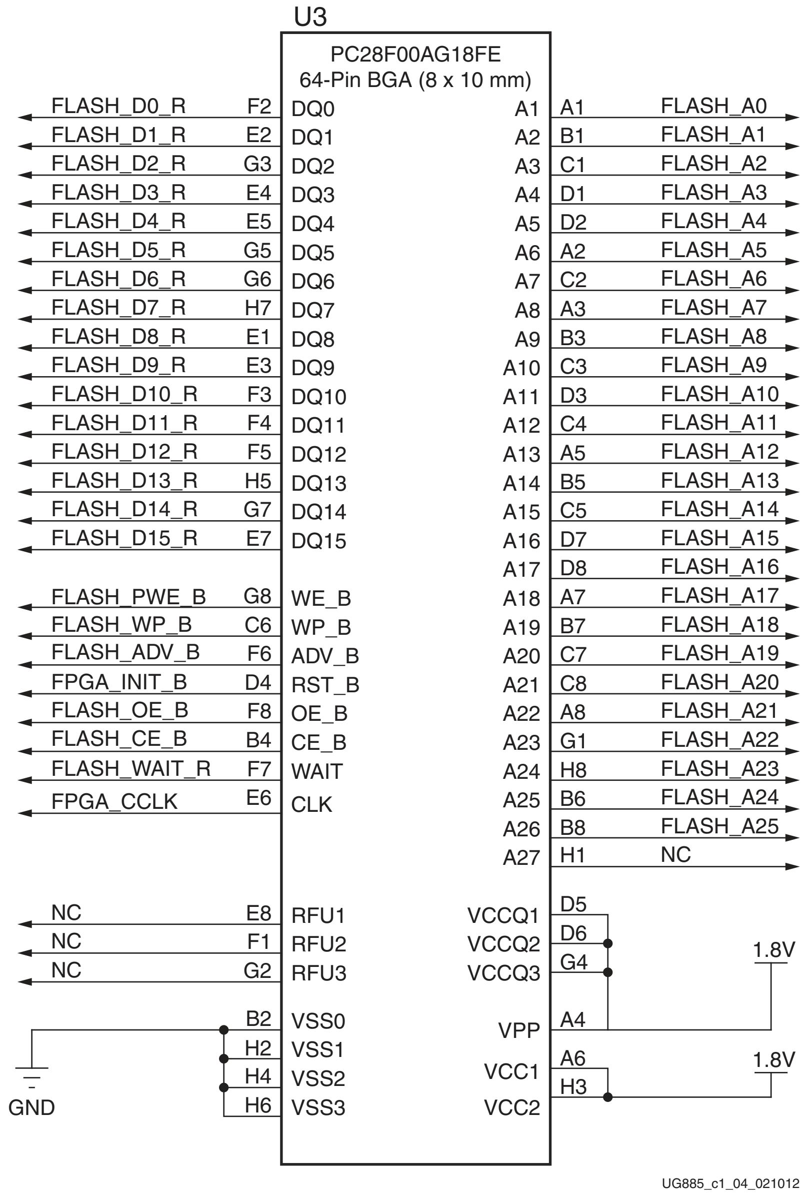

Figure 1-4: **128 MB Linear Flash Memory (U3)**

USB 2.0 ULPI Transceiver

[Figure 1-2, callout 4]

The VC707 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver (U8) to support a USB connection to the host computer. A USB cable is supplied in the VC707 Evaluation Kit (type-A connector to host computer, mini-B connector to VC707 board connector J2).

The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The USB3320 is clocked by a 24 MHz crystal. The ULPI interface supports two clocking modes selected by jumper on J14:

- 24 MHz ULPI output clock mode (default): No jumper on J14. The PHY drives the UPLI clock. This is the default setting.
- 60 MHz ULPI input clock mode: Jumper across J14 pins 1–2.

Consult the SMSC USB3320 data sheet for clocking mode details [Ref 18].

The FPGA interface to the USB3320 transceiver is implemented through the AXI universal serial bus 2.0 device IP. See *LogiCORE IP AXI Universal Serial Bus 2.0 Device Product Guide for Vivado Design Suite* (PG137) [Ref 6]

Note: The AXI universal serial bus 2.0 device IP supports USB-supplied power mode only. Jumpers on headers J13 and J45 must be configured to their default state as described here:

- J13 = jumper removed
- J45 = jumper across pins 1–2

Figure 1-5 shows the shield for the USB mini-B connector (J2) can be tied to GND by a jumper on header J44 pins 1–2 (default). The USB shield can optionally be connected through a capacitor to GND by installing a tantalum capacitor (body size C) at location C326 and jumping pins 2-3 on header J44.

The connections between the USB mini-B connector at J2 and the PHY at U8 are listed in Table 1-6.

Table 1-6: **USB Connector Pin Assignments and Signal Definitions Between J2 and U8**

USB Connector J2		Net Name	Description	USB3320 (U8) Pin
Pin	Name			
1	VBUS	USB_SMSC_VBUS	+5V from host system	22
2	D_N	USB_SMSC_HEADER_N	Bidirectional differential serial data (N-side)	19
3	D_P	USB_SMSC_HEADER_P	Bidirectional differential serial data (P-side)	18
4	GND	USB_SMC_GND	Signal ground	33

The connections between the USB 2.0 PHY at U8 and the FPGA are listed in Table 1-7.

Table 1-7: **USB 2.0 ULPI Transceiver Connections to the FPGA**

FPGA (U1) Pin	Net Name	I/O Standard	USB3320 (U8) Pin
AV36	USB_SMSC_DATA0	LVCMOS18	3
AW36	USB_SMSC_DATA1	LVCMOS18	4
BA34	USB_SMSC_DATA2	LVCMOS18	5
BB34	USB_SMSC_DATA3	LVCMOS18	6
BA36	USB_SMSC_DATA4	LVCMOS18	7
AT34	USB_SMSC_DATA5	LVCMOS18	9
AY35	USB_SMSC_DATA6	LVCMOS18	10
AW35	USB_SMSC_DATA7	LVCMOS18	13
BA35	USB_SMSC_NXT	LVCMOS18	2
BB36	USB_SMSC_RESET_B	LVCMOS18	27
BB32	USB_SMSC_STP	LVCMOS18	29
BB33	USB_SMSC_DIR	LVCMOS18	31
AV34	USB_SMSC_REFCLK_OPTION	LVCMOS18	26
AY32	USB_SMSC_CLKOUT	LVCMOS18	1

Figure 1-5 shows the USB 2.0 ULPI Transceiver circuitry.

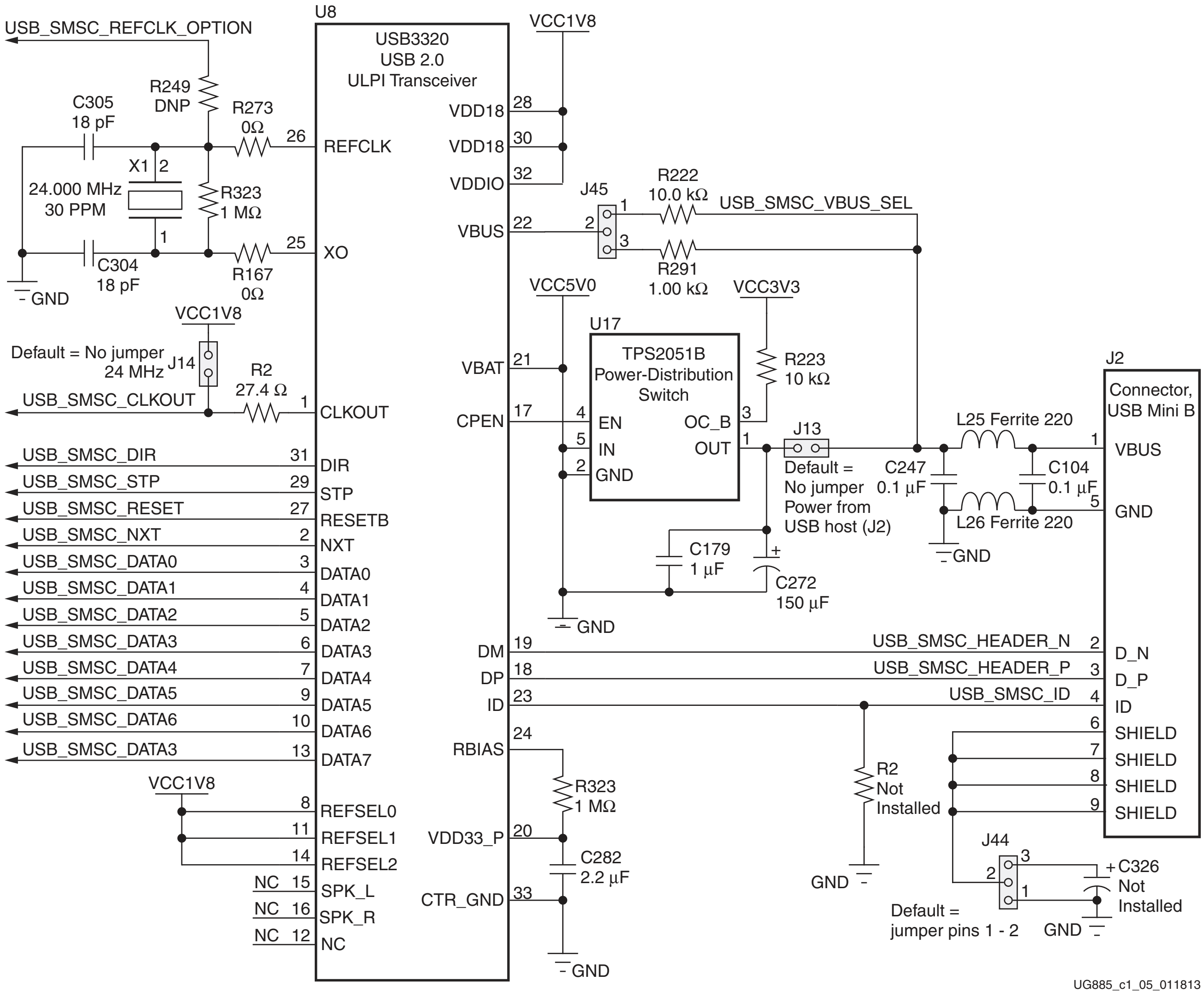

Figure 1-5: **USB 2.0 ULPI Transceiver**

SD Card Interface

[Figure 1-2, callout 5]

The VC707 board includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose nonvolatile SDIO memory cards and peripherals. The SD card slot is designed to support 50 MHz high speed SD cards.

The SDIO signals are connected to I/O bank 13 which has its VCCO set to 1.8V. A TI TXB0108 8-bit bidirectional voltage-level translator (U31) is used between the FPGA and the SD card connector (U29). Figure 1-6 shows the connections of the SD card interface on the VC707 board.

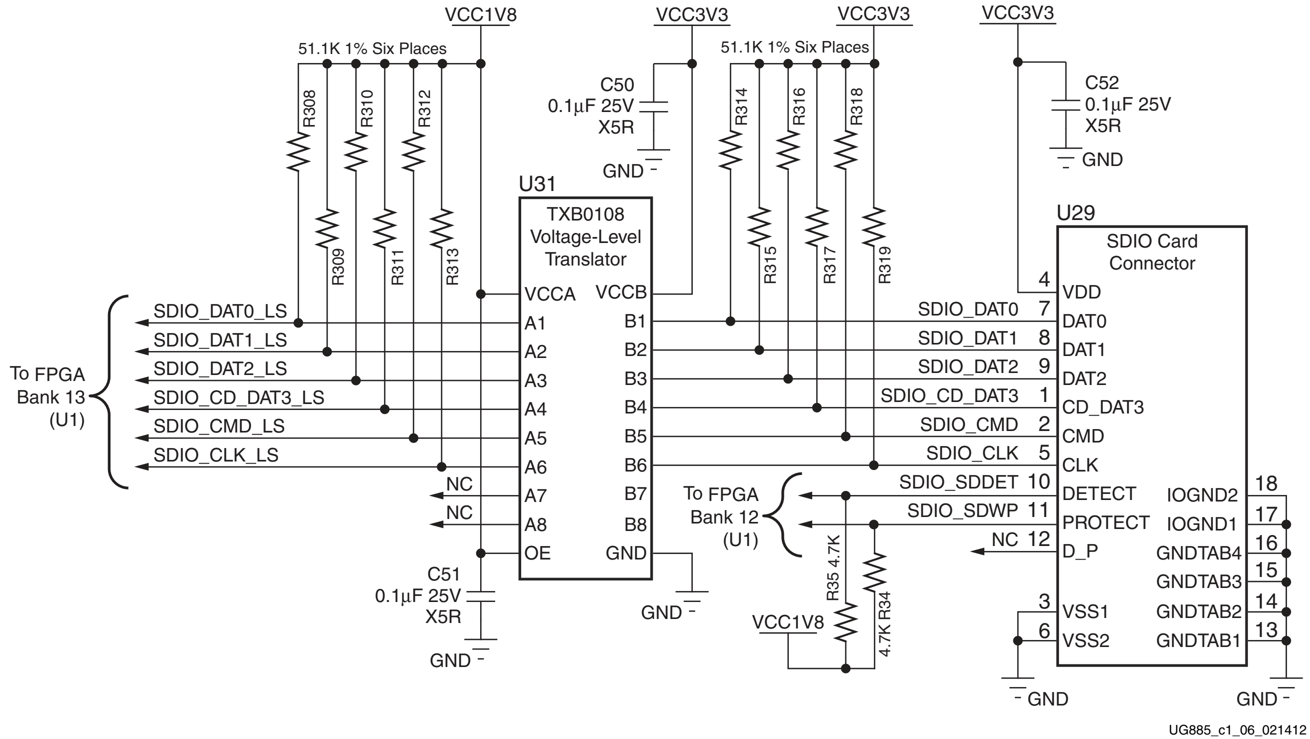

Figure 1-6: **SD Card Interface**

Table 1-8 lists the SD card interface connections to the FPGA.

Table 1-8: **SDIO Connections to the FPGA**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Level Shifter (U31)		SDIO Connector (U29)	
			Pin Number	Pin Name	Pin Number	Pin Name
AR32	SDIO_SDWP	LVCMOS18	N/A	N/A	11	SDWP
AP32	SDIO_SDDET	LVCMOS18	N/A	N/A	10	SDDET
AP30	SDIO_CMD_LS	LVCMOS18	6	A5	2	CMD
AN30	SDIO_CLK_LS	LVCMOS18	7	A6	5	CLK
AV31	SDIO_DAT2_LS	LVCMOS18	4	A3	9	DAT2
AU31	SDIO_DAT1_LS	LVCMOS18	3	A2	8	DAT1
AR30	SDIO_DAT0_LS	LVCMOS18	1	A1	7	DAT0
AT30	SDIO_CD_DAT3_LS	LVCMOS18	5	A4	1	CD_DAT3

USB JTAG

[Figure 1-2, callout 6]

JTAG configuration is provided through a Digilent onboard USB-to-JTAG configuration logic module (U26) where a host computer accesses the VC707 board JTAG chain through a type-A (host side) to micro-B (VC707 board side) USB cable.

A 2-mm JTAG header (J4) is also provided in parallel for access by Xilinx download cables such as the Platform Cable USB II and the Parallel Cable IV.

The JTAG chain of the VC707 board is illustrated in Figure 1-7. JTAG configuration is allowed at any time regardless of FPGA mode pin settings. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pin settings at SW11.

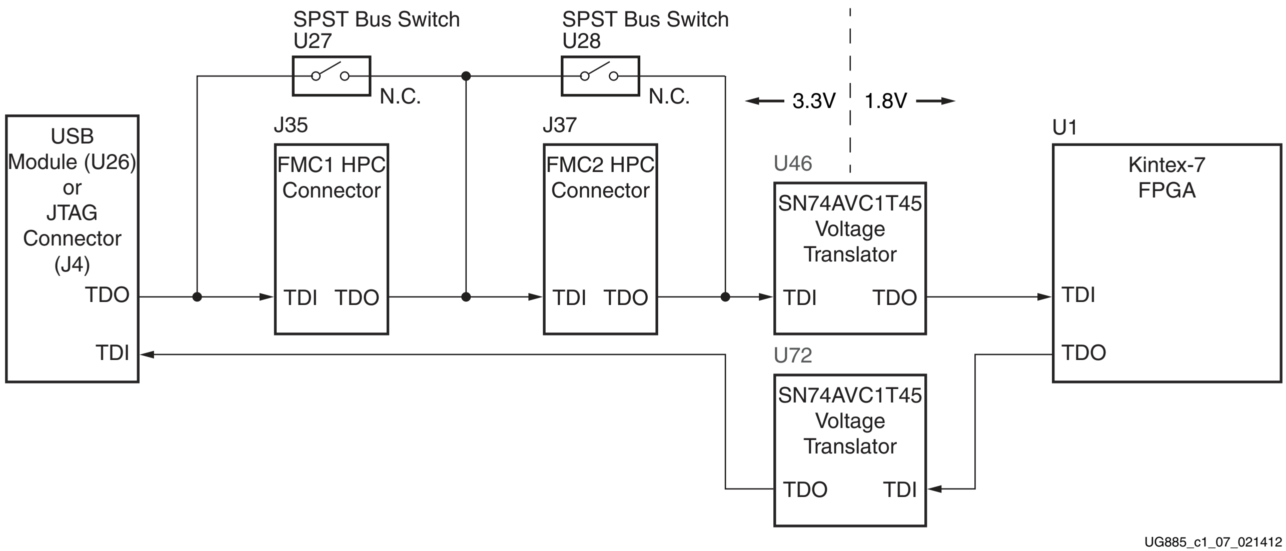

Figure 1-7: **JTAG Chain Block Diagram**

When an FMC mezzanine card is attached to the VC707 board it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U27 and U28. The SPST switches are in a normally closed state and transition to an open state when an FMC mezzanine card is attached. Switch U27 adds an attached FMC1 HPC mezzanine card to the FPGAs JTAG chain as determined by the FMC_HPC_PRSNT_M2C_B signal. Switch U28 adds an attached FMC2 HPC mezzanine card to the FPGAs JTAG chain as determined by the FMC2_LPC_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection via a device or bypass jumper to ensure that the JTAG chain connects to the FPGA U1.

The JTAG connectivity on the VC707 board allows a host computer to download bitstreams to the FPGA using the Xilinx® iMPACT software. In addition, the JTAG connector allows debug tools such as the Vivado serial I/O analyzer or a software debugger to access the FPGA. The iMPACT software tool can also indirectly program the Linear BPI Flash memory. To accomplish this, the iMPACT software configures the FPGA with a temporary design to access and program the BPI memory device.

The JTAG circuit details are shown in Figure 1-8.

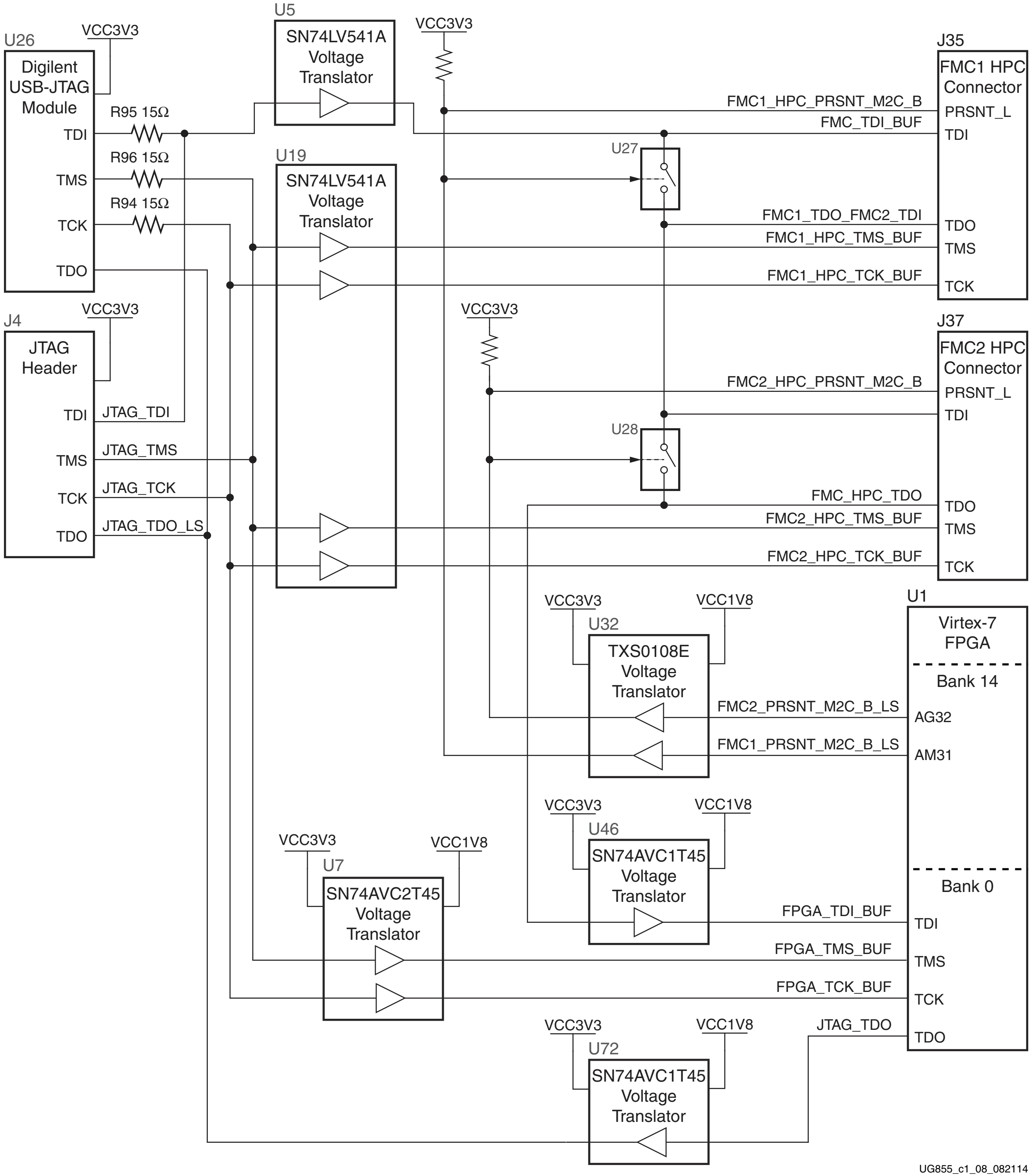

Figure 1-8: **JTAG Circuit**

Clock Generation

The VC707 board provides five clock sources for the FPGA. Table 1-9 lists the source devices for each clock.

Table 1-9: **VC707 Board Clock Sources**

Clock Name	Clock Source	Description
System Clock	U51	SiT9102 2.5V LVDS 200 MHz Fixed Frequency Oscillator (SiTime). See System Clock (SYSCLK_P and SYSCLK_N).
User Clock	U34	Si570 3.3V LVDS I^{2}C Programmable Oscillator, 156.250 MHz default (Silicon Labs). See Programmable User Clock (USER_CLOCK_P and USER_CLOCK_N).
User SMA Clock (differential pair)	J31	USER_SMA_CLOCK_P (Net name). See User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N).
	J32	USER_SMA_CLOCK_N (Net name). See User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N).
GTX SMA REF Clock (differential pair)	J25	SMA_MGT_REFCLK_C_P (Net name). See GTX SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N).
	J26	SMA_MGT_REFCLK_C_N (Net name). See GTX SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N).
Jitter Attenuated Clock	U24	Si5324C LVDS precision clock multiplier/jitter attenuator (Silicon Labs). See Jitter Attenuated Clock.

Table 1-10 lists the pin-to-pin connections from each clock source to the FPGA.

Table 1-10: **Clock Connections, Source to FPGA**

Clock Source Pin	Net Name	I/O Standard	FPGA (U1) Pin
U51.5	SYSCLK_N	LVDS	E18
U51.4	SYSCLK_P	LVDS	E19
U34.5	USER_CLOCK_N	LVDS	AL34
U34.4	USER_CLOCK_P	LVDS	AK34
J26.1	SMA_MGT_REFCLK_N	N/A (MGT REFCLK INPUT)	AK7
J25.1	SMA_MGT_REFCLK_P	N/A (MGT REFCLK INPUT)	AK8
J32.1	USER_SMA_CLOCK_N	LVCMOS18	AK32
J31.1	USER_SMA_CLOCK_P	LVCMOS18	AJ32
U24.29	Si5324_OUT_N	N/A (MGT REFCLK INPUT)	AD7
U24.28	Si5324_OUT_P	N/A (MGT REFCLK INPUT)	AD8

System Clock (SYSCLK_P and SYSCLK_N)

[Figure 1-2, callout 7]

The VC707 board has a LVDS 200 MHz oscillator (U51) soldered onto the back side of the board and wired to an FPGA MRCC clock input on bank 38. This 200 MHz signal pair is named SYSCLK_P and SYSCLK_N, which are connected to FPGA U1 pins E19 and E18 respectively.

- Oscillator: SiTime SiT9102AI-243N25E200.00000 (200 MHz)
- PPM frequency tolerance: 50 ppm
- Differential Output

For more details, see the SiTime SiT9102 data sheet [Ref 19]. The system clock circuit is shown in Figure 1-9.

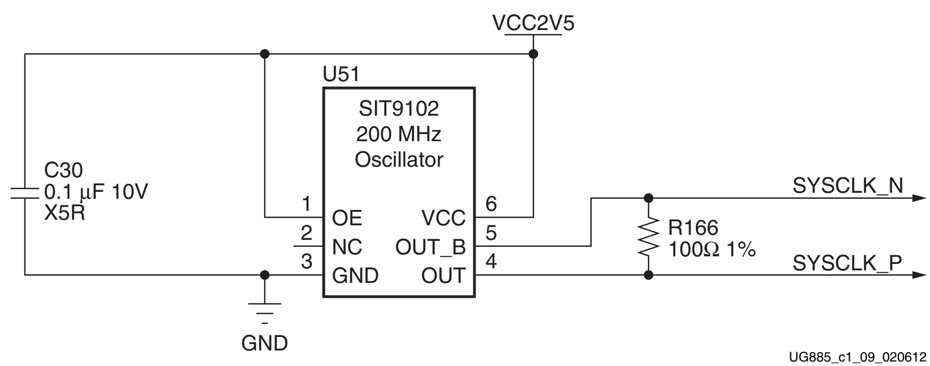

Figure 1-9: **System Clock Source**

Programmable User Clock (USER_CLOCK_P and USER_CLOCK_N)

[Figure 1-2, callout 8]

The VC707 board has a programmable low-jitter 3.3V differential oscillator (U34) connected to the FPGA MRCC inputs of bank 14. This USER_CLOCK_P and USER_CLOCK_N clock signal pair are connected to FPGA U1 pins AK34 and AL34 respectively. On power-up the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I^2C interface. Power cycling the VC707 board reverts the user clock to its default frequency of 156.250 MHz.

- Programmable Oscillator: Silicon Labs Si570BAB0000544DG (10 MHz - 810 MHz)
- Differential Output

For more details, see the Silicon Labs Si570 data sheet [Ref 20]. The user clock circuit is shown in Figure 1-10.

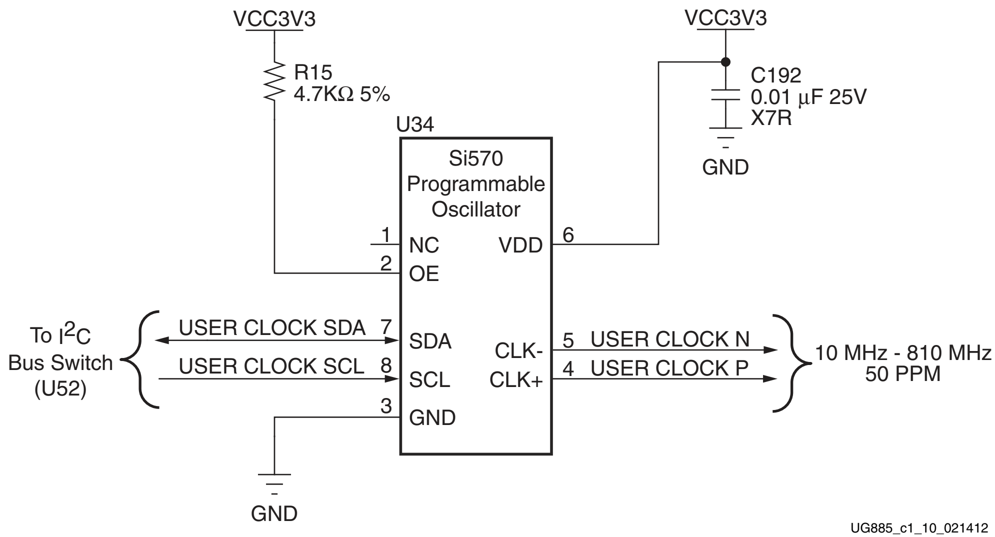

Figure 1-10: **User Clock Source**

Note: In Figure 1-10, USER_CLOCK_N and USER_CLOCK_P are differential clock signals.

User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N)

[Figure 1-2, callout 9]

An external high-precision clock signal can be provided to the FPGA bank 14 by connecting differential clock signals through the onboard 50Ω SMA connectors J31 (P) and J32 (N). The differential clock signal names are USER_SMA_CLOCK_P and USER_SMA_CLOCK_N, which are connected to FPGA U1 pins AJ32 and AK32 respectively. The user-provided 1.8 V differential clock circuit is shown in Figure 1-11.

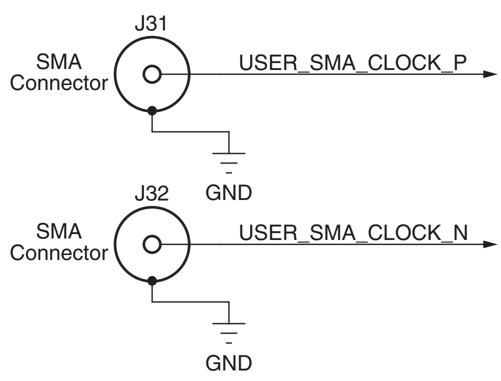

Figure 1-11: **User SMA Clock Source**

GTX SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N)

[Figure 1-2, callout 10]

The VC707 board includes a pair of SMA connectors for a GTX clock wired to GTX Quad bank 113. This differential clock has signal names SMA_MGT_REFCLK_P and SMA_REFCLK_N, which are connected to FPGA U1 pins AK8 and AK7 respectively. Figure 1-12 shows this AC-coupled clock circuit.

- External user-provided GTX reference clock on SMA input connectors
- Differential Input

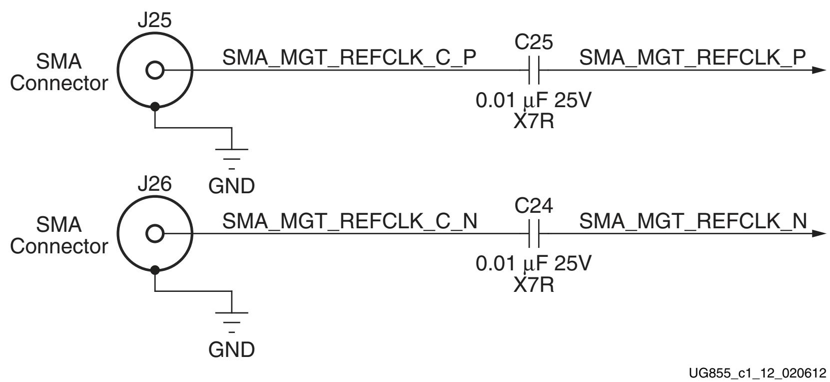

Figure 1-12: **GTX SMA Clock Source**

Jitter Attenuated Clock

[Figure 1-2, callout 11]

The VC707 board includes a Silicon Labs Si5324 jitter attenuator U24 on the back side of the board. FPGA user logic can implement a clock recovery circuit and then output this clock to a differential I/O pair on I/O bank 13 (REC_CLOCK_C_P, FPGA U1 pin AW32 and REC_CLOCK_C_N, FPGA U1 pin AW33) for jitter attenuation. The jitter attenuated clock (Si5324_OUT_C_P, Si5324_OUT_C_N) is then routed as a reference clock to GTX Quad 114 inputs MGTREFCLK0P (FPGA U1 pin AD8) and MGTREFCLK0N (FPGA U1 pin AD7).

The primary purpose of this clock is to support CPRI/OBSAI applications that perform clock recovery from a user-supplied SFP/SFP+ module and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTX transceiver. The jitter attenuated clock circuit is shown in Figure 1-13.

> ***Caution!*** The Silicon Labs Si5324 U24 pin 1 reset net SI5324_RST must be driven High to enable the device. The U24 pin 1 net SI5328_RST is level-shifted to 1.8V by U39 and is connected to FPGA U1 bank 13 pin AT36.

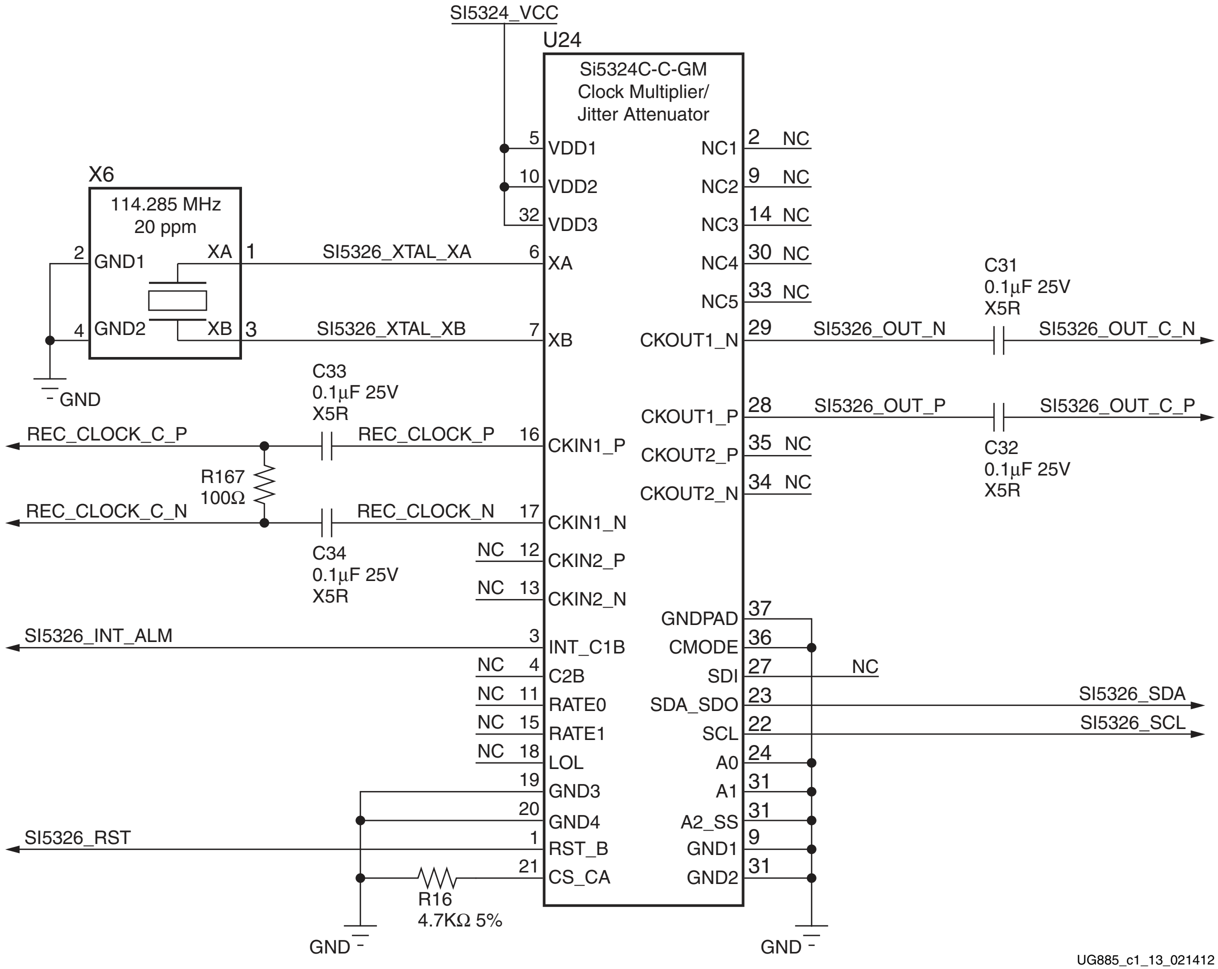

Figure 1-13: **Jitter Attenuated Clock**

See the Silicon Labs Si5324 data sheet for more information on this device [Ref 20].

GTX Transceivers

[Figure 1-2, callout 12]

The VC707 board provides access to 27 GTX transceivers:

- Eight of the GTX transceivers are wired to the PCI Express x8 endpoint edge connector (P1) fingers
- Eight of the GTX transceivers are wired to the FM1 HPC connector (J35)
- Eight of the GTX transceivers are wired to the FMC2 HPC connector (J37)
- One GTX is wired to SMA connectors (RX: J27, J28 TX: J29, J30)
- One GTX is wired to the SFP/SFP+ Module connector (P3)
- One GTX is used for the SGMII connection to the Ethernet PHY (U50)

The GTX transceivers in 7 series FPGAs are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTX Quad of interest. Seven of the nine GTX Quads are used on the VC707 board, with connectivity as shown here (Quads 111 and 112 are not used):

- Quad 113:
  - MGTREFCLK0 - SGMII clock
  - MGTREFCLK1 - SMA clock
  - Contains 3 GTX transceivers with one each allocated to SMA, SGMII and SFP
  - Contains 1 unused GTX transceiver
- Quad 114:
  - MGTREFCLK0 - Si5324 jitter attenuator
  - Contains 4 GTX transceivers for PCIe® lanes 4–7
- Quad 115:
  - MGTREFCLK1 - PCIe edge connector clock
  - Contains 4 GTX transceivers for PCIe lanes 0–3
- Quad 116:
  - MGTREFCLK0 - FMC2 HPC GBTCLK1
  - Contains 4 GTX transceivers for FMC2 HPC (DP4 – DP7)
- • Quad 117:
  - MGTREFCLK0 - FMC2 HPC GBTCLK0
  - Contains 4 GTX transceivers for FMC2 HPC (DP0 – DP3)
- Quad 118:
  - MGTREFCLK0 - FMC1 HPC GBTCLK1
  - Contains 4 GTX transceivers for FMC1 HPC (DP4 – DP7)
- Quad 119:
  - MGTREFCLK0 - FMC1 HPC GBTCLK0
  - Contains 4 GTX transceivers for FMC1 HPC (DP0 – DP3)

Table 1-11 lists the GTX interface connections to the FPGA (U1).

Table 1-11: **GTX Interface Connections for FPGA U1**

Transceiver Bank	FHG1761 Placement	Connections
MGT_BANK_113	GTXE2_CHANNEL_X1Y0	SMA
	GTXE2_CHANNEL_X1Y1	SGMII
	GTXE2_CHANNEL_X1Y2	SFP+
	GTXE2_CHANNEL_X1Y3	NC
	MGTREFCLK0	SGMII_CLK
	MGTREFCLK1	SMA_MGT_REFCLK
MGT_BANK_114	GTXE2_CHANNEL_X1Y4	PCIe7
	GTXE2_CHANNEL_X1Y5	PCIe6
	GTXE2_CHANNEL_X1Y6	PCIe5
	GTXE2_CHANNEL_X1Y7	PCIe4
	MGTREFCLK0	Si5324
	MGTREFCLK1	NC

Table 1-11: **GTX Interface Connections for FPGA U1 *(Cont'd)***

Transceiver Bank	FHG1761 Placement	Connections
MGT_BANK_115	GTXE2_CHANNEL_X1Y8	PCIe3
	GTXE2_CHANNEL_X1Y9	PCIe2
	GTXE2_CHANNEL_X1Y10	PCIe1
	GTXE2_CHANNEL_X1Y11	PCIe0
	MGTREFCLK0	NC
	MGTREFCLK1	PCIe_CLK
MGT_BANK_116	GTXE2_CHANNEL_X1Y12	FMC2 HPC DP4
	GTXE2_CHANNEL_X1Y13	FMC2 HPC DP5
	GTXE2_CHANNEL_X1Y14	FMC2 HPC DP6
	GTXE2_CHANNEL_X1Y15	FMC2 HPC DP7
	MGTREFCLK0	FMC2 HPC GBT_CLK1
	MGTREFCLK1	NC
MGT_BANK_117	GTXE2_CHANNEL_X1Y16	FMC2 HPC DP0
	GTXE2_CHANNEL_X1Y17	FMC2 HPC DP1
	GTXE2_CHANNEL_X1Y18	FMC2 HPC DP2
	GTXE2_CHANNEL_X1Y19	FMC2 HPC DP3
	MGTREFCLK0	FMC2 HPC GBT_CLK0
	MGTREFCLK1	NC
MGT_BANK_118	GTXE2_CHANNEL_X1Y20	FMC1 HPC DP4
	GTXE2_CHANNEL_X1Y21	FMC1 HPC DP5
	GTXE2_CHANNEL_X1Y22	FMC1 HPC DP6
	GTXE2_CHANNEL_X1Y23	FMC1 HPC DP7
	MGTREFCLK0	FMC1 HPC GBT_CLK1
	MGTREFCLK1	NC
MGT_BANK_119	GTXE2_CHANNEL_X1Y24	FMC1 HPC DP0
	GTXE2_CHANNEL_X1Y25	FMC1 HPC DP1
	GTXE2_CHANNEL_X1Y26	FMC1 HPC DP2
	GTXE2_CHANNEL_X1Y27	FMC1 HPC DP3
	MGTREFCLK0	FMC1 HPC GBT_CLK0
	MGTREFCLK1	NC

For more information on the GTX transceivers, see *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 7].

PCI Express Endpoint Connectivity

[Figure 1-2, callout 13]

The 8-lane PCI Express edge connector performs data transfers at the rate of 2.5 gigatransfers per second (GT/s) for a Gen1 application and 5.0 GT/s for a Gen2 application. The PCIe transmit and receive signal datapaths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair. The 7 series FPGAs GTX transceivers are used for multi-gigabit per second serial interfaces.

The XC7VX485T-2FFG1761C FPGA (-2 speed grade) included with the VC707 board supports up to Gen2 x8.

The PCIe clock is input from the edge connector. It is AC coupled to the FPGA through the MGTREFCLK1 pins of Quad 115. PCIE_CLK_Q0_P is connected to FPGA U1 pin AB8, and the _N net is connected to pin AB7. The PCI Express clock circuit is shown in Figure 1-14.

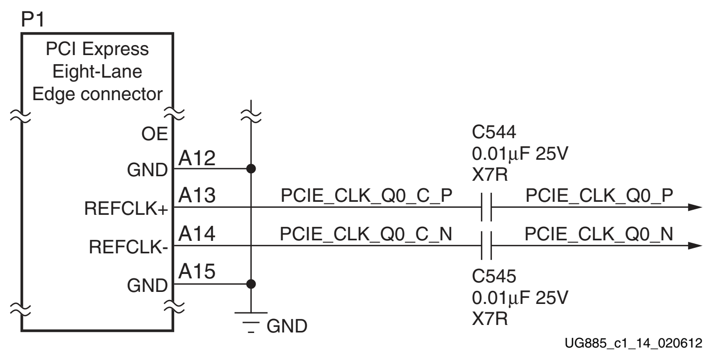

Figure 1-14: **PCI Express Clock**

PCIe lane width/size is selected through jumper J49 (Figure 1-15). The default lane size selection is 1-lane (J49 pins 1 and 2 jumpered).

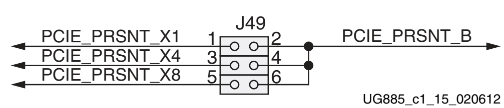

Figure 1-15: **PCI Express Lane Size Select Jumper J49**

Table 1-12 lists the PCIe edge connector connections at P1.

Table 1-12: **PCIe Edge Connector Connections GTX Quad 115**

Net Name	FPGA (U1) Pin	PCIe Edge Connector (P1)		Function	FHG1761 Placement
		Pin	Name		
PCIE_RX0_P	Y4	B14	PETp0	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y11
PCIE_RX0_N	Y3	B15	PETn0	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y11
PCIE_RX1_P	AA6	B19	PETp1	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y10
PCIE_RX1_N	AA5	B20	PETn1	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y10
PCIE_RX2_P	AB4	B23	PETp2	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y9
PCIE_RX2_N	AB3	B24	PETn2	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y9
PCIE_RX3_P	AC6	B27	PETp3	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y8

Table 1-12: **PCIe Edge Connector Connections GTX Quad 115 *(Cont'd)***

Net Name	FPGA (U1) Pin	PCIe Edge Connector (P1)		Function	FHG1761 Placement
		Pin	Name		
PCIE_RX3_N	AC5	B28	PETn3	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y8
PCIE_RX4_P	AD4	B33	PETp4	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y7
PCIE_RX4_N	AD3	B34	PETn4	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y7
PCIE_RX5_P	AE6	B37	PETp5	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y6
PCIE_RX5_N	AE5	B38	PETn5	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y6
PCIE_RX6_P	AF4	B41	PETp6	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y5
PCIE_RX6_N	AF3	B42	PETn6	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y5
PCIE_RX7_P	AG6	B45	PETp7	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y4
PCIE_RX7_N	AG5	B46	PETn7	Integrated Endpoint block receive pair	GTXE2_CHANNEL_X1Y4
PCIE_TX0_P	W2	A16	PERp0	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y11
PCIE_TX0_N	W1	A17	PERn0	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y11
PCIE_TX1_P	AA2	A21	PERp1	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y10
PCIE_TX1_N	AA1	A22	PERn1	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y10
PCIE_TX2_P	AC2	A25	PERp2	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y9
PCIE_TX2_N	AC1	A26	PERn2	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y9
PCIE_TX3_P	AE2	A29	PERp3	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y8
PCIE_TX3_N	AE1	A30	PERn3	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y8
PCIE_TX4_P	AG2	A35	PERp4	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y7
PCIE_TX4_N	AG1	A36	PERn4	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y7
PCIE_TX5_P	AH4	A39	PERp5	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y6
PCIE_TX5_N	AH3	A40	PERn5	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y6
PCIE_TX6_P	AJ2	A43	PERp6	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y5
PCIE_TX6_N	AJ1	A44	PERn6	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y5
PCIE_TX7_P	AK4	A47	PERp7	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y4
PCIE_TX7_N	AK3	A48	PERn7	Integrated Endpoint block transmit pair	GTXE2_CHANNEL_X1Y4
Si5324_OUT_C_P	AD8	A13	REFCLK+	Integrated Endpoint block differential clock pair from PCIe	MGT_BANK_114 (not Quad 115)
Si5324_OUT_C_N	AD7	A14	REFCLK-	Integrated Endpoint block differential clock pair from PCIe	MGT_BANK_114 (not Quad 115)
PCIE_PRSNT_B	J49 2, 4, 6	A1	PRSNT#1	J49 Lane Size Select jumper	NA
PCIE_WAKE_B	AV33	B11	WAKE#	Integrated Endpoint block wake signal, not connected on KC705 Board	NA
PCIE_PERST_B	AV35	A11	PERST	Integrated Endpoint block reset signal	NA

Table 1-13 lists the PCIe edge connector connections for Quad 115.

Table 1-13: **GTX Quad 115 PCIe Edge Connector Connections**

Quad 115 Pin Name	FPGA (U1) Pin	Net Name	PCIe Edge Connector (P1)		FHG1761 Placement
			Pin	Pin Name	
MGTXTXP0_115_AE2	AE2	PCIE_TX3_P	A29	PERp3	GTXE2_CHANNEL_X1Y11
MGTXTXN0_115_AE1	AE1	PCIE_TX3_N	A30	PERn3	GTXE2_CHANNEL_X1Y11
MGTXRXP0_115_AC6	AC6	PCIE_RX3_P	B27	PETp3	GTXE2_CHANNEL_X1Y11
MGTXRXN0_115_AC5	AC5	PCIE_RX3_N	B28	PETn3	GTXE2_CHANNEL_X1Y11
MGTXTXP1_115_AC2	AC2	PCIE_TX2_P	A25	PERp2	GTXE2_CHANNEL_X1Y10
MGTXTXN1_115_AC1	AC1	PCIE_TX2_N	A26	PERn2	GTXE2_CHANNEL_X1Y10
MGTXRXP1_115_AB4	AB4	PCIE_RX2_P	B23	PETp2	GTXE2_CHANNEL_X1Y10
MGTXRXN1_115_AB3	AB3	PCIE_RX2_N	B24	PETn2	GTXE2_CHANNEL_X1Y10
MGTXTXP2_115_AA2	AA2	PCIE_TX1_P	A21	PERp1	GTXE2_CHANNEL_X1Y9
MGTXTXN2_115_AA1	AA1	PCIE_TX1_N	A22	PERn1	GTXE2_CHANNEL_X1Y9
MGTXRXP2_115_AA6	AA6	PCIE_RX1_P	B19	PETp1	GTXE2_CHANNEL_X1Y9
MGTXRXN2_115_AA5	AA5	PCIE_RX1_N	B20	PETn1	GTXE2_CHANNEL_X1Y9
MGTXTXP3_115_W2	W2	PCIE_TX0_P	A16	PERp0	GTXE2_CHANNEL_X1Y8
MGTXTXN3_115_W1	W1	PCIE_TX0_N	A17	PERn0	GTXE2_CHANNEL_X1Y8
MGTXRXP3_115_Y4	Y4	PCIE_RX0_P	B14	PETp0	GTXE2_CHANNEL_X1Y8
MGTXRXN3_115_Y3	Y3	PCIE_RX0_N	B15	PETn0	GTXE2_CHANNEL_X1Y8
MGTREFCLK0P_115_Y8	Y8	NC			MGT_BANK_115
MGTREFCLK0N_115_Y7	Y7	NC			MGT_BANK_115
MGTREFCLK1P_115_AB8	AB8	PCIE_CLK_Q0_P	A13	REFCLK+	MGT_BANK_115
MGTREFCLK1N_115_AB7	AB7	PCIE_CLK_Q0_N	A14	REFCLK-	MGT_BANK_115

Table 1-14 lists the PCIe edge connector connections for Quad 114.

Table 1-14: **GTX Quad 114 PCIe Edge Connector Connections**

Quad 114 Pin Name	FPGA (U1) Pin	Net Name	PCIe Edge Connector (P1)		FHG1761 Placement
			Pin	PCIe Edge Pin Name	
MGTXTXP0_114_AK4	AK4	PCIE_TX7_P	A47	PERp7	GTXE2_CHANNEL_X1Y4
MGTXTXN0_114_AK3	AK3	PCIE_TX7_N	A48	PERn7	GTXE2_CHANNEL_X1Y4
MGTXRXP0_114_AG6	AG6	PCIE_RX7_P	B45	PETp7	GTXE2_CHANNEL_X1Y4
MGTXRXN0_114_AG5	AG5	PCIE_RX7_N	B46	PETn7	GTXE2_CHANNEL_X1Y4
MGTXTXP1_114_AJ2	AJ2	PCIE_TX6_P	A43	PERp6	GTXE2_CHANNEL_X1Y5
MGTXTXN1_114_AJ1	AJ1	PCIE_TX6_N	A44	PERn6	GTXE2_CHANNEL_X1Y5

Table 1-14: **GTX Quad 114 PCIe Edge Connector Connections *(Cont'd)***

Quad 114 Pin Name	FPGA (U1) Pin	Net Name	PCIe Edge Connector (P1)		FHG1761 Placement
			Pin	PCIe Edge Pin Name	
MGTXRXP1_114_AF4	AF4	PCIE_RX6_P	B41	PETp6	GTXE2_CHANNEL_X1Y5
MGTXRXN1_114_AF3	AF3	PCIE_RX6_N	B42	PETn6	GTXE2_CHANNEL_X1Y5
MGTXTXP2_114_AH4	AH4	PCIE_TX5_P	A39	PERp5	GTXE2_CHANNEL_X1Y6
MGTXTXN2_114_AH3	AH3	PCIE_TX5_N	A40	PERn5	GTXE2_CHANNEL_X1Y6
MGTXRXP2_114_AE6	AE6	PCIE_RX5_P	B37	PETp5	GTXE2_CHANNEL_X1Y6
MGTXRXN2_114_AE5	AE5	PCIE_RX5_N	B38	PETn5	GTXE2_CHANNEL_X1Y6
MGTXTXP3_114_AG2	AG2	PCIE_TX4_P	A35	PERp4	GTXE2_CHANNEL_X1Y7
MGTXTXN3_114_AG1	AG1	PCIE_TX4_N	A36	PERn4	GTXE2_CHANNEL_X1Y7
MGTXRXP3_114_AD4	AD4	PCIE_RX4_P	B33	PETp4	GTXE2_CHANNEL_X1Y7
MGTXRXN3_114_AD3	AD3	PCIE_RX4_N	B34	PETn4	GTXE2_CHANNEL_X1Y7
MGTREFCLK0P_114_AD8	AD8	SI5324_OUT_C_P	U24.28 through C32		MGT_BANK_114
MGTREFCLK0N_114_AD7	AD7	SI5324_OUT_C_N	U24.29 through C31		MGT_BANK_114
MGTREFCLK1P_114_AF8	AF8	NC			MGT_BANK_114
MGTREFCLK1N_114_AF7	AF7	NC			MGT_BANK_114

For more information refer to *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 7] and *7 Series FPGAs Integrated Block for PCI Express Product Guide for Vivado Design Suite* (PG054) [Ref 8].

SFP/SFP+ Module Connector

[Figure 1-2, callout 14]

The VC707 board contains a small form-factor pluggable (SFP+) connector and cage assembly P3 that accepts SFP or SFP+ modules. Figure 1-16 shows the SFP+ module connector circuitry.

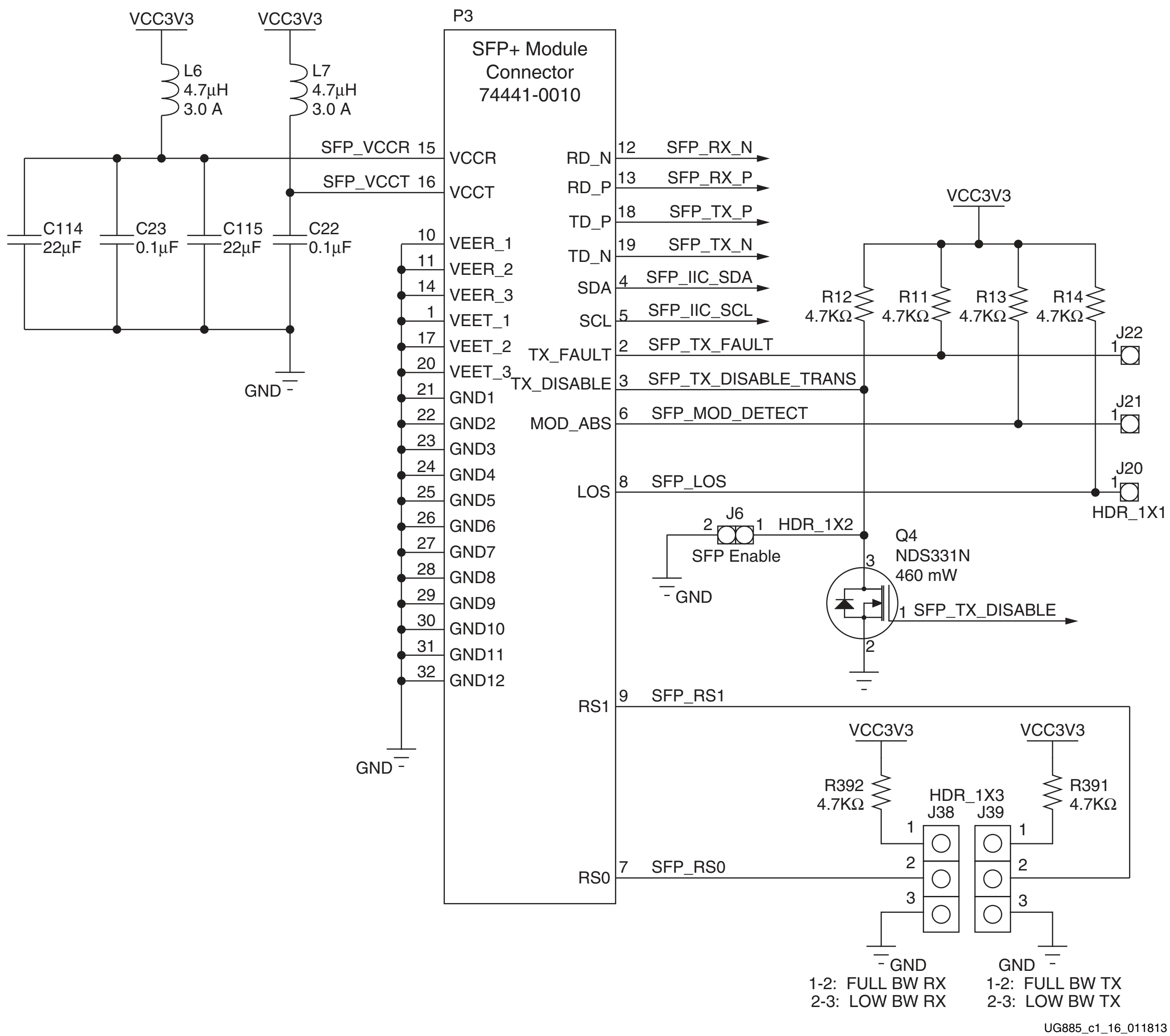

Figure 1-16: **SFP+ Module Connector**

Table 1-15 lists the SFP+ module RX and TX connections to the FPGA.

Table 1-15: **FPGA U1 GTX Bank 113 to SFP+ Module Connections**

FPGA (U1) Pin	Schematic Net Name	SFP+ Module (P3)	
		Pin	Name
AL5	SFP_RX_N	12	RD_N
AL6	SFP_RX_P	13	RD_P
AM4	SFP_TX_P	18	TD_P
AM3	SFP_TX_N	19	TD_N
AP33	SFP_TX_DISABLE_TRANS	3	TX_DISABLE

Table 1-16 lists the SFP+ module control and status connections to the FPGA.

Table 1-16: **SFP+ Module Control and Status**

SFP Control/Status Signal	Board Connection	
SFP_TX_FAULT	Test Point J22	High = Fault
		Low = Normal Operation
SFP_TX_DISABLE	Jumper J6	Off = SFP Disabled
		On = SFP Enabled
SFP_MOD_DETECT	Test Point J21	High = Module Not Present
		Low = Module Present
SFP_RS0	Jumper J38	Jumper Pins 1-2 = Full RX Bandwidth
		Jumper Pins 2-3 = Reduced RX Bandwidth
SFP_RS1	Jumper J39	Jumper Pins 1-2 = Full TX Bandwidth
		Jumper Pins 2-3 = Reduced TX Bandwidth
SFP_LOS	Test Point J20	High = Loss of Receiver Signal
		Low = Normal Operation

10/100/1000 Tri-Speed Ethernet PHY

[Figure 1-2, callout 15]

The VC707 board utilizes the Marvell Alaska PHY device (88E1111) U50 for Ethernet communications at 10, 100, or 1000 Mb/s. The board supports SGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Halo HFJ11-1G01E RJ-45 connector (P4) with built-in magnetics.

On power-up, or on reset, the PHY is configured to operate in SGMII mode with PHY address `0b00111` using the settings shown in Table 1-17. These settings can be overwritten by software commands passed over the MDIO interface.

Table 1-17: **Board Connections for PHY Configuration Pins**

Pin	Connection on Board	Bit[2] Definition and Value	Bit[1] Definition and Value	Bit[0] Definition and Value
CFG0	V_{CC} 2.5V	PHYADR[2] = 1	PHYADR[1] = 1	PHYADR[0] = 1
CFG1	Ground	ENA_PAUSE = 0	PHYADR[4] = 0	PHYADR[3] = 0
CFG2	V_{CC} 2.5V	ANEG[3] = 1	ANEG[2] = 1	ANEG[1] = 1
CFG3	V_{CC} 2.5V	ANEG[0] = 1	ENA_XC = 1	DIS_125 = 1
CFG4	V_{CC} 2.5V	HWCFG_MD[2] = 1	HWCFG_MD[1] = 1	HWCFG_MD[0] = 1
CFG5	PHY_LED_LINK10	DIS_FC = 1	DIS_SLEEP = 1	HWCFG_MD[3] = 1
CFG6	PHY_LED_RX	SEL_BDT = 0	INT_POL = 1	75/50Ω= 0

The Ethernet connections from FPGA U1 to the 88E1111 PHY device are listed in Table 1-18.

Table 1-18: **Ethernet Connections, FPGA to PHY Device**

FPGA (U1) Pin	Net Name	I/O Standard	M88E1111 PHY U50	
			Pin	Name
AK33	PHY_MDIO	LVCMOS18	M1	MDIO
AH31	PHY_MDC	LVCMOS18	L3	MDC
AL31	PHY_INT	LVCMOS18	L1	INT_B
AJ33	PHY_RESET	LVCMOS18	K3	RESET_B
AN2	SGMII_TX_P	N/A (MGT REFCLK INPUT)	A3	SIN_P
AN1	SGMII_TX_N	N/A (MGT REFCLK INPUT)	A4	SIN_N
AM8	SGMII_RX_P	N/A (MGT REFCLK INPUT)	A7	SOUT_P
AM7	SGMII_RX_N	N/A (MGT REFCLK INPUT)	A8	SOUT_N

SGMII GTX Transceiver Clock Generation

[Figure 1-2, callout 16]

An Integrated Circuit Systems ICS844021I chip (U2) generates a high-quality, low-jitter, 125 MHz LVDS clock from a 25 MHz crystal (X3). This clock is sent to FPGA U1, Bank 113 GTX transceiver (clock pins AH8 (P) and AH7 (N)) driving the SGMII interface. Series AC coupling capacitors are present to allow the clock input of the FPGA to set the common mode voltage. Figure 1-17 shows the Ethernet SGMII clock source.

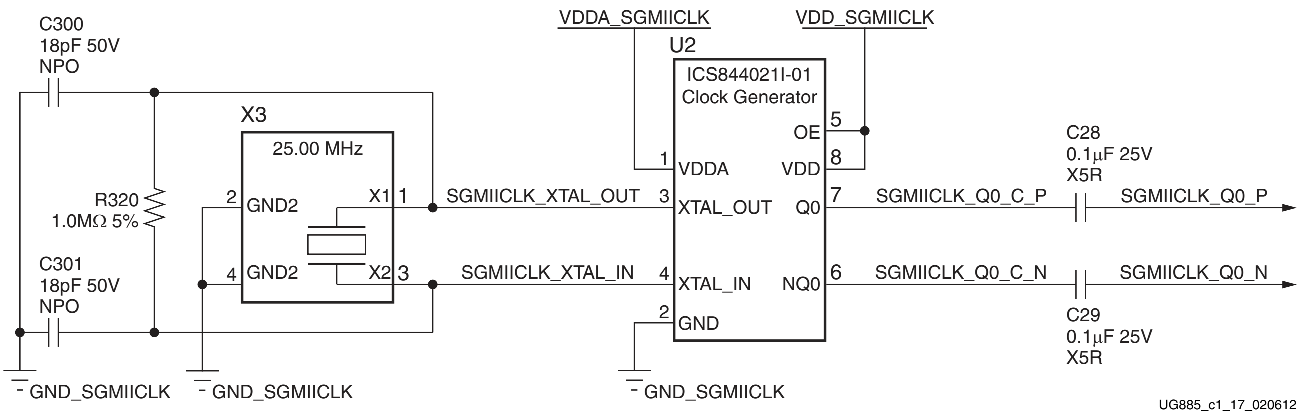

Figure 1-17: **Ethernet 125 MHz SGMII GTX Clock**

References

Details about the tri-mode Ethernet MAC core are provided in *LogiCORE IP Tri-Mode Ethernet MAC Product Guide for Vivado Design Suite* (PG051) [Ref 9] and in the *LogiCORE IP Tri-Mode Ethernet MAC v4.5 User Guide* (UG138) [Ref 13].

The product brief for the Marvell 88E1111 Alaska Gigabit Ethernet Transceiver can be found at the Marvell website [Ref 21].

The data sheet can be obtained under NDA with Marvell. Contact information is at the Marvell website [Ref 21].

For more information about the ICS844021 device, go to the Integrated Device Technology website [Ref 22] and search for part number **ICS844021**.

USB-to-UART Bridge

[Figure 1-2, callout 17]

The VC707 board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U44) which allows a connection to a host computer with a USB port. The USB cable is supplied in the VC707 Evaluation Kit (Type-A end to host computer, Type mini-B end to VC707 board connector J17). The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the VC707 board.

Xilinx UART IP is expected to be implemented in the FPGA logic. The FPGA supports the USB-to-UART bridge using four signal pins: Transmit (TX), Receive (RX), Request to Send (RTS), and Clear to Send (CTS).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, TeraTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the VC707 board.

The USB Connector Pin Assignments and Signal Definitions between J17 and U44 are listed in Table 1-19.

Table 1-19: **USB Connector J17 Pin Assignments and Signal Definitions**

USB Connector (J17)		Net Name	Description	CP2103GM (U44)	
Pin	**Name**			**Pin**	**Name**
1	VBUS	USB_UART_VBUS	+5V VBUS Powered	7	REGIN
				8	VBUS
2	D_N	USB_D_N	Bidirectional differential serial data (N-side)	4	D –
3	D_P	USB_D_P	Bidirectional differential serial data (P-side)	3	D +
4	GND	USB_UART_GND	Signal ground	2	GND1
				29	CNR_GND

Table 1-20 shows the USB connections between the FPGA and the UART.

Table 1-20: **FPGA to UART Connections**

FPGA (U1)				Schematic Net Name	CP2013 Device (U12)		
Pin	**Function**	**Direction**	**IOSTANDARD**		**Pin**	**Function**	**Direction**
AR34	RTS	Output	LVCMOS18	USB_CTS	22	CTS	Input
AT32	CTS	Input	LVCMOS18	USB_RTS	23	RTS	Output
AU36	TX	Output	LVCMOS18	USB_RX	24	RXD	Input
AU33	RX	Input	LVCMOS18	USB_TX	25	TXD	Output

Refer to the Silicon Labs website for technical information on the CP2103GM and the VCP drivers [Ref 20].

HDMI Video Output

[Figure 1-2, callout 18]

The VC707 board provides a High-Definition Multimedia Interface (HDMI™) video output using the Analog Devices ADV7511KSTZ-P HDMI transmitter (U48). The HDMI output is provided on a Molex 500254-1927 HDMI type-A connector (P2). The ADV7511 is wired to support 1080P 60 Hz YCbCr and RGB video modes through 36-bit input data mapping.

The VC707 board supports the following HDMI device interfaces:

- 36 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK
- Interrupt Out Pin to FPGA
- I^2C
- SPDIF

Figure 1-18 shows the HDMI codec circuit.

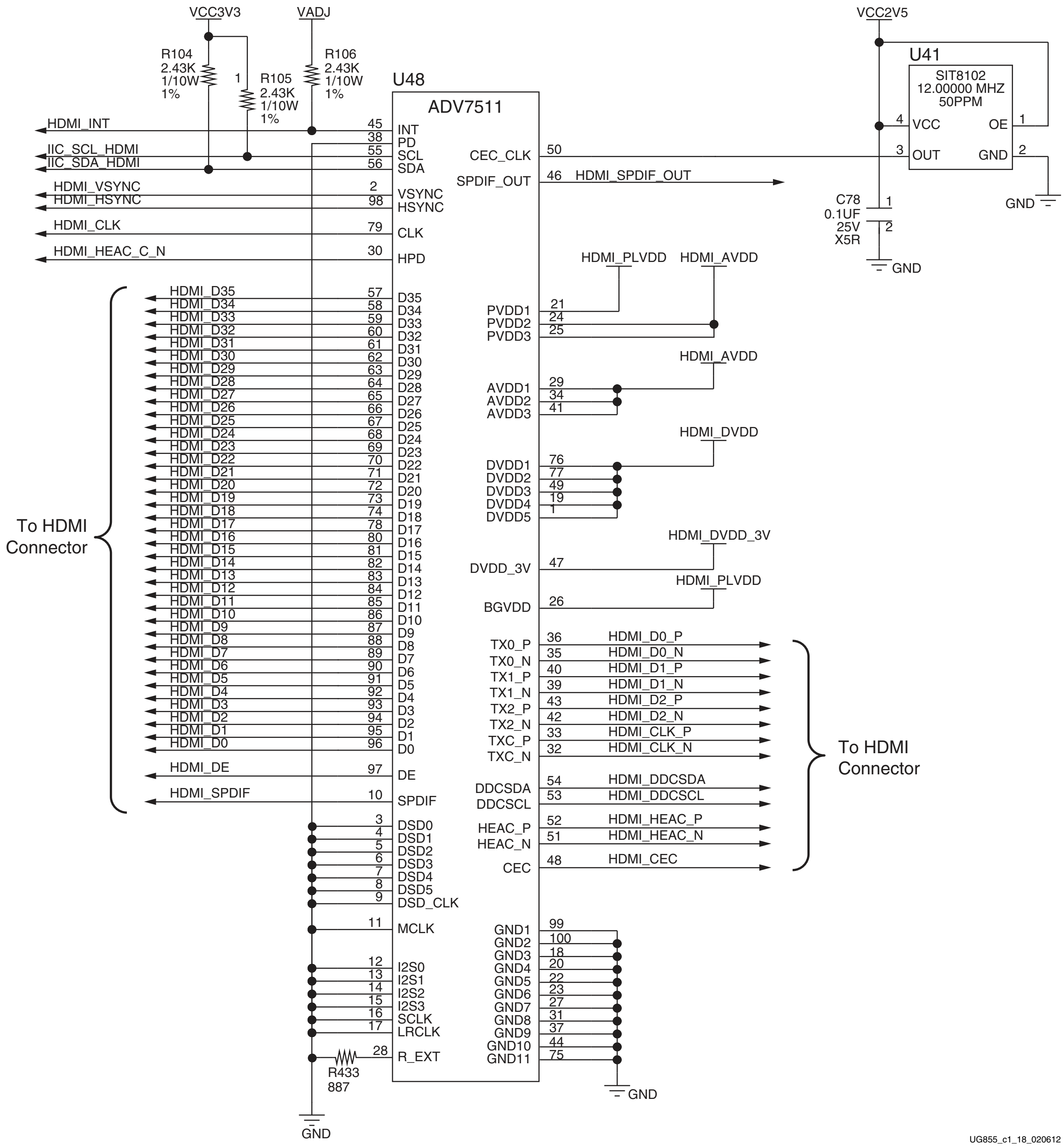

Figure 1-18: **HDMI Codec Circuit**

Table 1-21 lists the connections between the codec and the FPGA.

Table 1-21: **FPGA to HDMI Codec Connections (ADV7511)**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	ADV7511 (U48)	
			Pin Number	Pin Name
AM22	HDMI_D0	LVCMOS18	96	D0
AL22	HDMI_D1	LVCMOS18	95	D1
AJ20	HDMI_D2	LVCMOS18	94	D2
AJ21	HDMI_D3	LVCMOS18	93	D3
AM21	HDMI_D4	LVCMOS18	92	D4
AL21	HDMI_D5	LVCMOS18	91	D5
AK22	HDMI_D6	LVCMOS18	90	D6
AJ22	HDMI_D7	LVCMOS18	89	D7
AL20	HDMI_D8	LVCMOS18	88	D8
AK20	HDMI_D9	LVCMOS18	87	D9
AK23	HDMI_D10	LVCMOS18	86	D10
AJ23	HDMI_D11	LVCMOS18	85	D11
AN21	HDMI_D12	LVCMOS18	84	D12
AP22	HDMI_D13	LVCMOS18	83	D13
AP23	HDMI_D14	LVCMOS18	82	D14
AN23	HDMI_D15	LVCMOS18	81	D15
AM23	HDMI_D16	LVCMOS18	80	D16
AN24	HDMI_D17	LVCMOS18	78	D17
AY24	HDMI_D18	LVCMOS18	74	D18
BB22	HDMI_D19	LVCMOS18	73	D19
BA22	HDMI_D20	LVCMOS18	72	D20
BA25	HDMI_D21	LVCMOS18	71	D21
AY25	HDMI_D22	LVCMOS18	70	D22
AY22	HDMI_D23	LVCMOS18	69	D23
AY23	HDMI_D24	LVCMOS18	68	D24
AV24	HDMI_D25	LVCMOS18	67	D25
AU24	HDMI_D26	LVCMOS18	66	D26
AW21	HDMI_D27	LVCMOS18	65	D27
AV21	HDMI_D28	LVCMOS18	64	D28
AT24	HDMI_D29	LVCMOS18	63	D29
AR24	HDMI_D30	LVCMOS18	62	D30

Table 1-21: **FPGA to HDMI Codec Connections (ADV7511)** ***(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	ADV7511 (U48)	
			Pin Number	Pin Name
AU21	HDMI_D31	LVCMOS18	61	D31
AT21	HDMI_D32	LVCMOS18	60	D32
AW22	HDMI_D33	LVCMOS18	59	D33
AW23	HDMI_D34	LVCMOS18	58	D34
AV23	HDMI_D35	LVCMOS18	57	D35
AP21	HDMI_DE	LVCMOS18	97	DE
AR23	HDMI_SPDIF	LVCMOS18	10	SPDIF
AU23	HDMI_CLK	LVCMOS18	79	CLK
AT22	HDMI_VSYNC	LVCMOS18	2	VSYNC
AU22	HDMI_HSYNC	LVCMOS18	98	HSYNC
AM24	HDMI_INT	LVCMOS18	45	INT
AR22	HDMI_SPDIF_OUT	LVCMOS18	46	SPDIF_OUT

Table 1-22 lists the connections between the codec and the HDMI connector P2.

Table 1-22: **ADV7511 to HDMI Connector Connections**

ADV7511 (U48)	Net Name	HDMI Connector P2 Pin
36	HDMI_D0_P	7
35	HDMI_D0_N	9
40	HDMI_D1_P	4
39	HDMI_D1_N	6
43	HDMI_D2_P	1
42	HDMI_D2_N	3
33	HDMI_CLK_P	10
32	HDMI_CLK_N	12
54	HDMI_DDCSDA	16
53	HDMI_DDCSCL	15
52	HDMI_HEAC_P	14
51	HDMI_HEAC_N	19
48	HDMI_CRC	13

Information about the ADV7511 is available on the Analog Devices website [Ref 23]. Search for the term **ADV7511KSTZ-P**.

LCD Character Display (16 x 2)

[Figure 1-2, callout 19]

A 2-line by 16-character display is provided on the VC707 board (Figure 1-19).

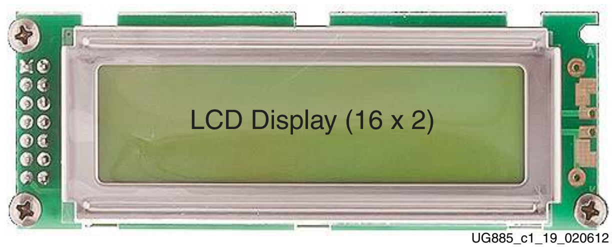

Figure 1-19: **LCD Display**

The character display runs at 5.0V and is connected to the FPGA's 1.8V HP bank 15 through a TI TXS0108E 8-bit bidirectional voltage level translator (U33). Figure 1-20 shows the LCD interface circuit.

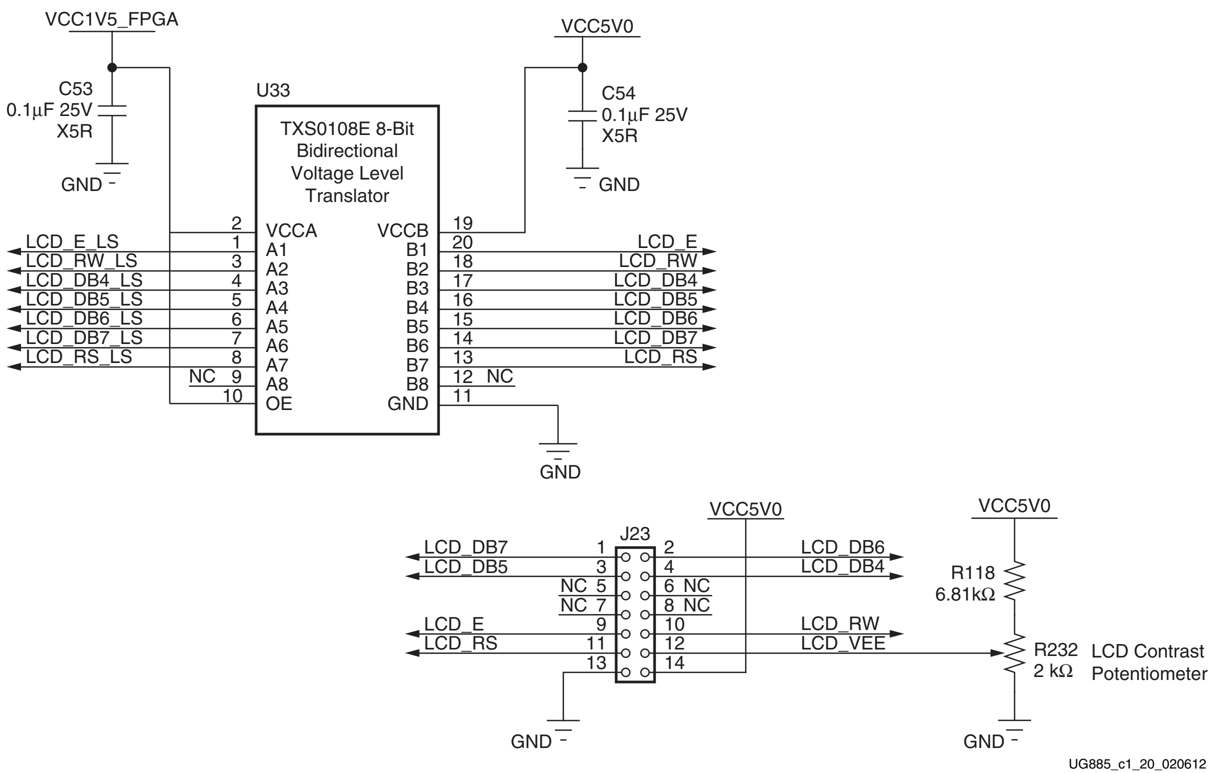

Figure 1-20: **LCD Interface Circuit**

The VC707 board base board uses a male Samtec MTLW-107-07-G-D-265 2x7 header (J23) with 0.025-inch square posts on 0.100-inch centers for connecting to a Samtec SLW-107-01-L-D female socket on the LCD display panel assembly. The LCD header shown in Figure 1-21. When the LCD is not installed, the J31 header pins listed in Table 1-23 are available for use as GPIO.

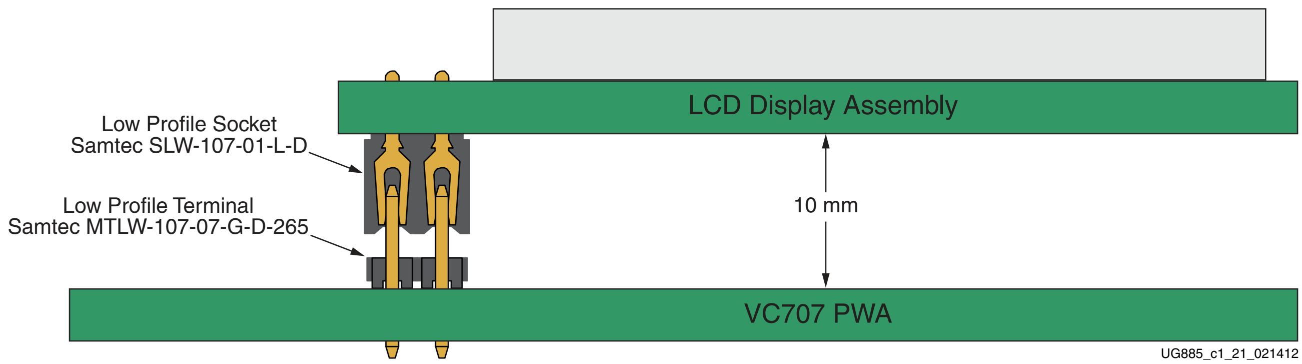

Figure 1-21: **LCD Header Details**

Table 1-23 lists the connections between the FPGA and the LCD header.

Table 1-23: **FPGA to LCD Header Connections**

FPGA (U1) Pin	Net Name	I/O Standard	LCD Header Pin (J31)
AT42	LCD_DB4_LS	LVCMOS18	4
AR38	LCD_DB5_LS	LVCMOS18	3
AR39	LCD_DB6_LS	LVCMOS18	2
AN40	LCD_DB7_LS	LVCMOS18	1
AR42	LCD_RW_LS	LVCMOS18	10
AN41	LCD_RS_LS	LVCMOS18	11
AT40	LCD_E_LS	LVCMOS18	9

References

The data sheet for the Displaytech S162DBABC LCD can be found at the Displaytech website [Ref 24]. Choose the **S162D** model full spec download arrow.

I^{2}C Bus

[Figure 1-2, callout 20]

The VC707 board implements a single I^{2}C port on the FPGA (IIC_SDA_MAIN, IIC_SDA_SCL), which is routed through a 1-to-8 channel I^{2}C bus switch (U52). The bus switch can operate at speeds up to 400 kHz.

The bus switch I^{2}C address is `0x74` (`0b1110100`) and must be addressed and configured to select the desired downstream device.

The VC707 board I^2C bus topology is shown in Figure 1-22.

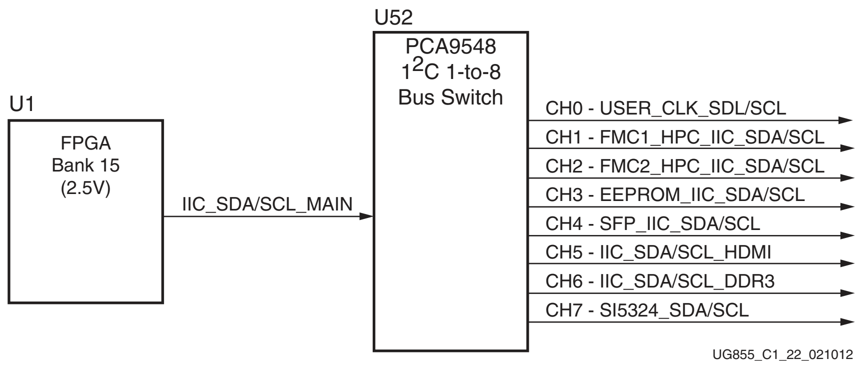

Figure 1-22: **I^2C Bus Topology**

User applications that communicate with devices on one of the downstream I^2C buses must first set up a path to the desired bus through the U52 bus switch at I^2C address `0x74` (`0b1110100`). Table 1-24 lists the address for each bus.

Table 1-24: **I^2C Bus Addresses**

I^2C Device	I^2C Switch Position	I^2C Address
PCA9548	NA	`0b1110100`
Si570 Clock	0	`0b1011101`
FMC1 HPC	1	`0bXXXXX00`
FMC2 HPC	2	`0bXXXXX00`
M24C08 EEPROM	3	`0b1010100`
SFP Module	4	`0b1010000`
ADV7512 HDMI	5	`0b0111001`
DDR3 SODIMM	6	`0b1010000, 0b0011000`
Si5324 Clock	7	`0b1101000`

Notes:

1. Use the PCA9458 (U52) at I^2C address `0x74` (`0b1110100`) to setup the path to these buses.

Information about the PCA9548 is available on the TI Semiconductor website [Ref 25].

> ***Caution!*** The PCA9548 U52 RESET_B pin 24 is connected to the FPGA U1 bank 15 pin AY42 via level-shifter U70. The FPGA pin AY42 LVCMOS18 net IIC_MUX_RESET_B_LS must be driven High to enable I2C bus transactions with the devices connected to U52.

Status LEDs

[Figure 1-2, callout 21]

Table 1-25 defines the status LEDs. For user controlled LEDs see User I/O.

Table 1-25: **Status LEDs**

Reference Designator	Signal Name	Color	Description
DS11	PHY_LED_RX	GREEN	Ethernet PHY RX
DS11	PHY_LED_LINK1000	GREEN	Ethernet Link Speed is 1000 Mb/s
DS12	PHY_LED_TX	GREEN	Ethernet PHY TX
DS12	PHY_LED_LINK100	GREEN	Ethernet Link Speed is 100 Mb/s
DS13	PHY_LED_DUPLEX	GREEN	Ethernet Link is Half-duplex
DS13	PHY_LED_LINK10	GREEN	Ethernet Link Speed is 10 Mb/s
DS14	PWRCTL1_VCC4A_PG	GREEN	FMC1 HPC Power Good
DS10	FPGA_DONE	GREEN	FPGA Configured Successfully
DS1	FPGA_INIT_B	GREEN/RED	GREEN: FPGA Initialization Successful, RED: FPGA Initialization in Progress
DS16	VCC12_P_IN	GREEN	12V Power ON
DS17	PWRCTL_PWRGOOD	GREEN	UCD9248 Power Controllers (U42, U43, U64) Power Good
DS18	LINEAR_POWER_GOOD	GREEN	TPS51200 Power Good (U23)

User I/O

[Figure 1-2, callout 22 - 26]

The VC707 board provides the following user and general purpose I/O capabilities:

- Eight user LEDs (callout 22)
  - GPIO_LED_[7-0]: DS9, DS8, DS7, DS6, DS5, DS4, DS3, DS2
- Reset switch and five user pushbuttons (callout 23)
  - CPU_RESET: SW8
  - GPIO_SW_[NESWC]: SW3, SW4, SW5, SW7, SW6
- 8-position user DIP Switch (callout 24)
  - GPIO_DIP_SW[7-0]: SW2
- User rotary switch (callout 25, hidden beneath the LCD)
  - ROTARY_PUSH, ROTARY_INCA, ROTARY_INCB: SW10
- User SMA (callout 26)
  - USER_SMA_GPIO_P, USER_SMA_GPIO_N: J33, J34
- 2 line x 16 character LCD character display (callout 19)
  - If the display is unmounted, connector J23 pins are available as 7 independent GPIOs. The LCD connector J23 details are shown in the LCD Character Display (16 x 2) section.

User LEDs

Figure 1-23 shows the user LED circuits.

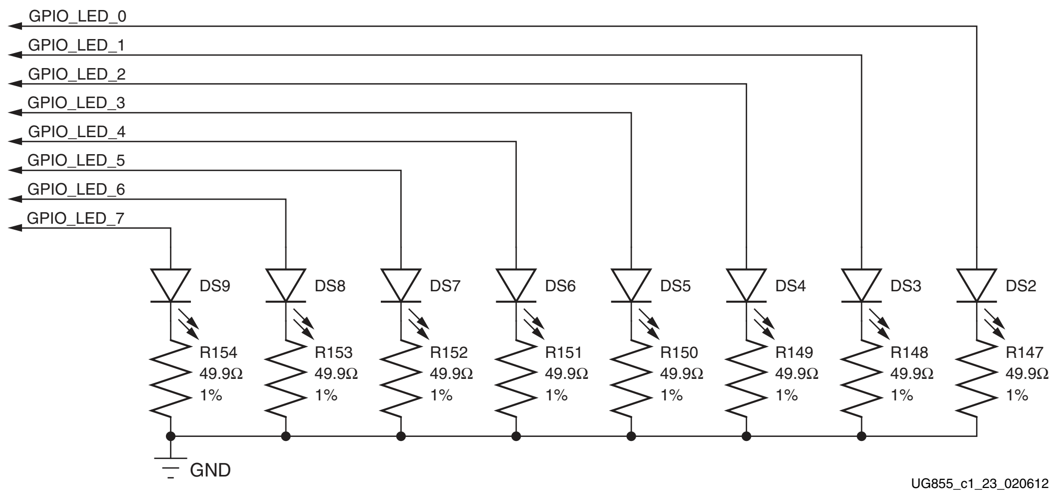

Figure 1-23: **User LEDs**

CPU Reset Pushbutton

Figure 1-24 shows the CPU reset pushbutton switch circuit.

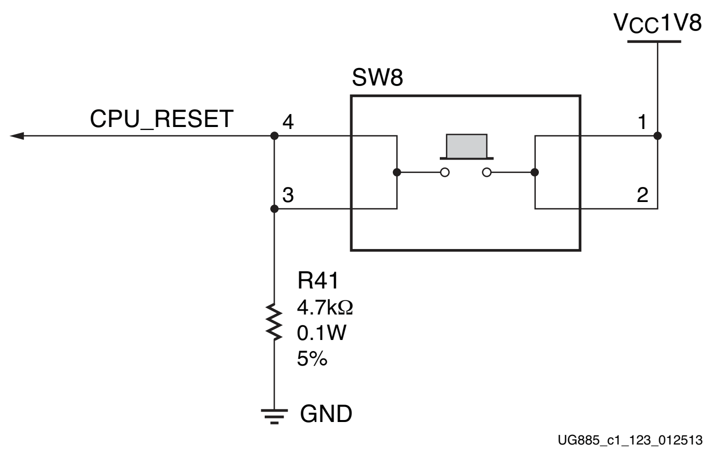

Figure 1-24: **CPU Reset Pushbutton**

User Pushbuttons

Figure 1-25 shows the user pushbutton switch circuits.

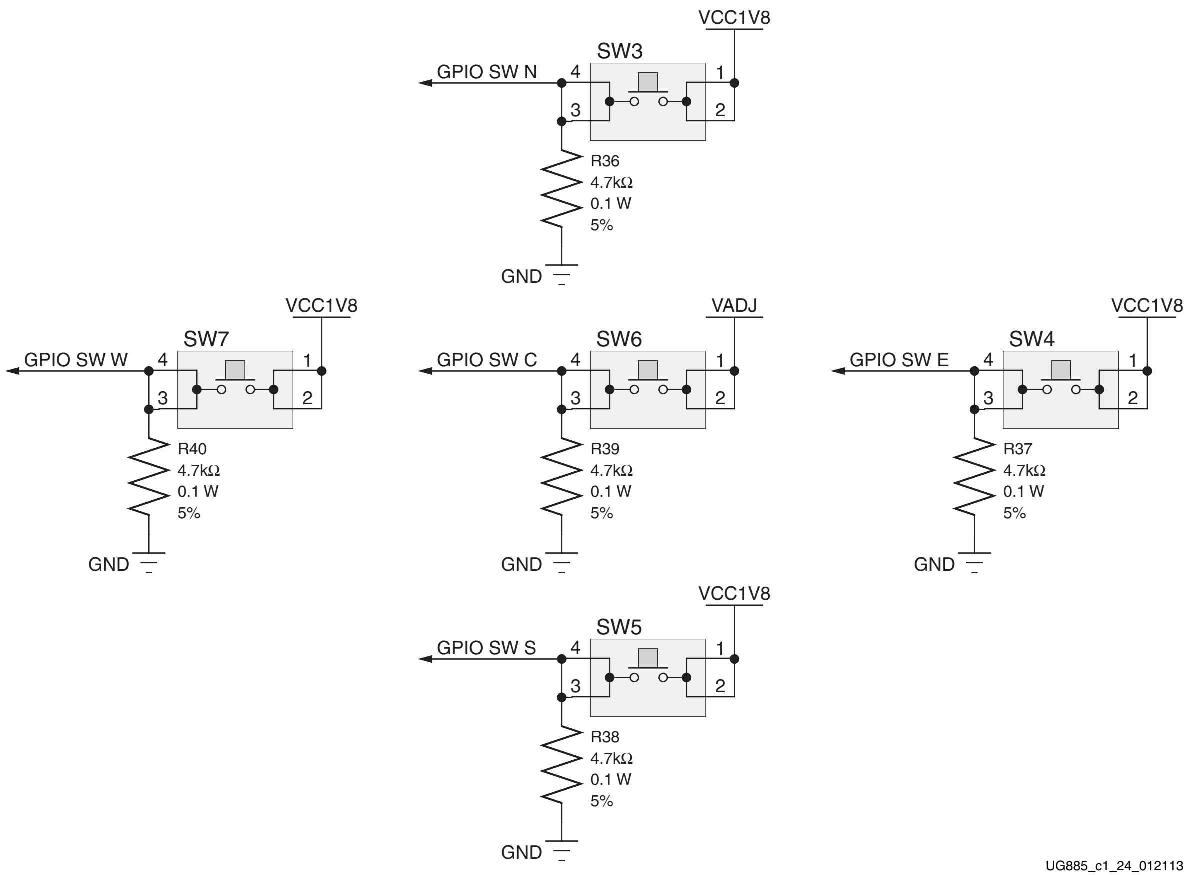

Figure 1-25: **User Pushbuttons**

GPIO DIP Switch Circuit

Figure 1-26 shows the GPIO DIP switch circuit.

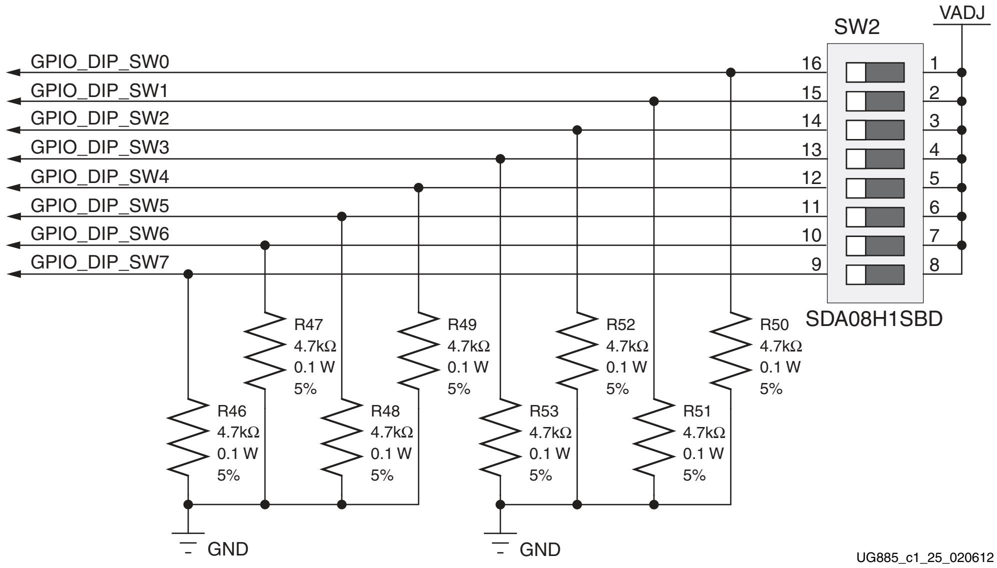

Figure 1-26: **GPIO DIP Switch Circuit**

User Rotary Switch

Figure 1-27 shows the user rotary switch circuit.

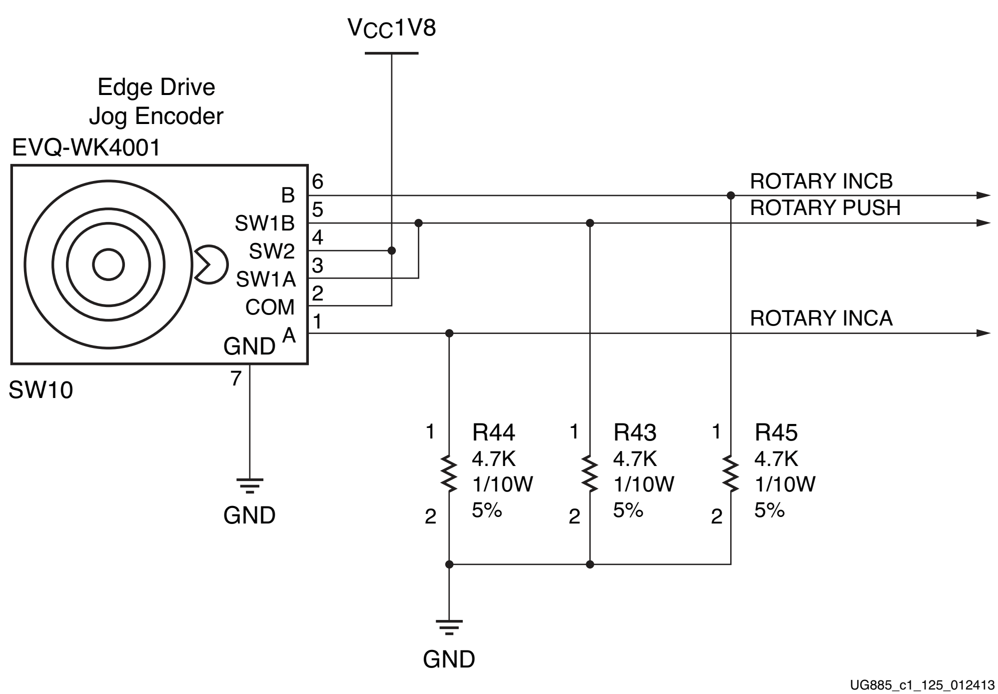

Figure 1-27: **User Rotary Switch**

User SMA

Figure 1-28 shows the user SMA circuit.

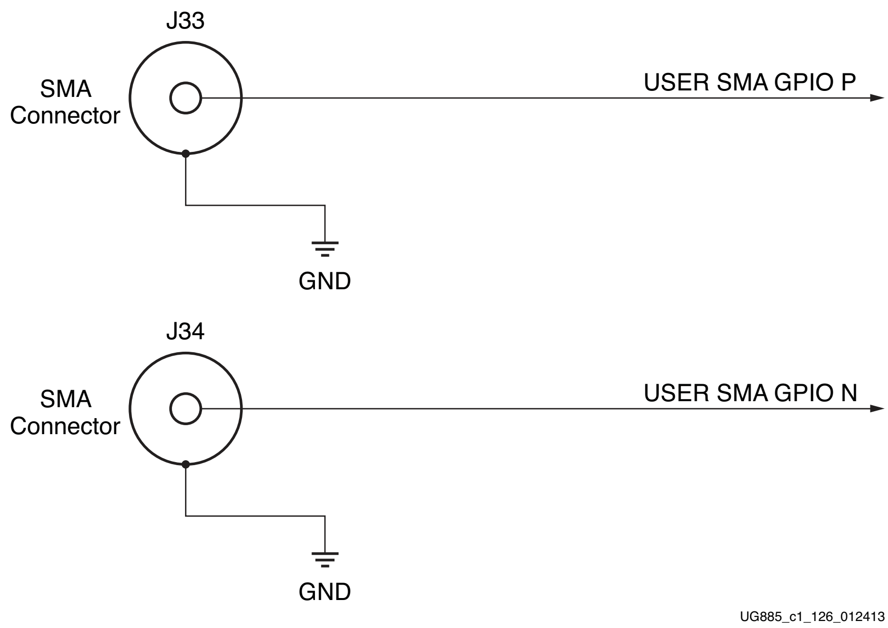

Figure 1-28: **User SMA**

Table 1-26 lists the GPIO Connections to FPGA U1.

Table 1-26: **GPIO Connections to FPGA U1**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	GPIO Pin
Indicator LEDs (Active-High)			
AM39	GPIO_LED_0	LVCMOS18	DS2.2
AN39	GPIO_LED_1	LVCMOS18	DS3.2
AR37	GPIO_LED_2	LVCMOS18	DS4.2
AT37	GPIO_LED_3	LVCMOS18	DS5.2
AR35	GPIO_LED_4	LVCMOS18	DS6.2
AP41	GPIO_LED_5	LVCMOS18	DS7.2
AP42	GPIO_LED_6	LVCMOS18	DS8.2
AU39	GPIO_LED_7	LVCMOS18	DS9.2
CPU Reset Pushbutton Switch			
AV40	CPU_RESET	LVCMOS18	SW8.3
Directional Pushbutton Switches			
AR40	GPIO_SW_N	LVCMOS18	SW3.3
AU38	GPIO_SW_E	LVCMOS18	SW4.3
AP40	GPIO_SW_S	LVCMOS18	SW5.3

Table 1-26: **GPIO Connections to FPGA U1 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	GPIO Pin
AW40	GPIO_SW_W	LVCMOS18	SW7.3
AV39	GPIO_SW_C	LVCMOS18	SW6.3
8-Pole DIP Switch			
AV30	GPIO_DIP_SW0	LVCMOS18	SW2.16
AY33	GPIO_DIP_SW1	LVCMOS18	SW2.15
BA31	GPIO_DIP_SW2	LVCMOS18	SW2.14
BA32	GPIO_DIP_SW3	LVCMOS18	SW2.13
AW30	GPIO_DIP_SW4	LVCMOS18	SW2.12
AY30	GPIO_DIP_SW5	LVCMOS18	SW2.11
BA30	GPIO_DIP_SW6	LVCMOS18	SW2.10
BB31	GPIO_DIP_SW7	LVCMOS18	SW2.9
User Rotary Switch			
AT31	ROTARY_INCB	LVCMOS18	SW10.6
AW31	ROTARY_PUSH	LVCMOS18	SW10.5
AR33	ROTARY_INCA	LVCMOS18	SW10.1
User SMA			
AN31	USER_SMA_GPIO_P	LVCMOS18	J33.1
AP31	USER_SMA_GPIO_N	LVCMOS18	J34.1

Switches

[Figure 1-2, callout 27 - 28]

The VC707 board Evaluation Board includes a power and a configuration switch:

- Power On/Off Slide Switch SW12 (callout 27)
- FPGA_PROG_B SW9, active-Low (callout 28)

Power On/Off Slide Switch SW12

[Figure 1-2, callout 27]

The VC707 board power switch is SW12. Sliding the switch actuator from the Off to On position applies 12V power from J18, a 6-pin mini-fit connector. Green LED DS16 illuminates when the VC707 board power is on. See Power Management for details on the onboard power system.

> ***Caution!*** Do NOT plug a PC ATX power supply 6-pin connector into J18 on the VC707 board. The ATX 6-pin connector has a different pinout than J18. Connecting an ATX 6-pin connector into J18 will damage the VC707 board and void the board warranty.

The VC707 Evaluation Kit provides the adapter cable shown in Figure 1-29 for powering the VC707 board from the ATX power supply 4-pin peripheral connector. The Xilinx part number for this cable is 2600304, and is equivalent to Sourcegate Technologies part number AZCBL-WH-1109-RA4. For information on ordering this cable, see [Ref 27].

Figure 1-29: **ATX Power Supply Adapter Cable**

Figure 1-30 shows the power connector J18, power switch SW12 and indicator LED DS16.

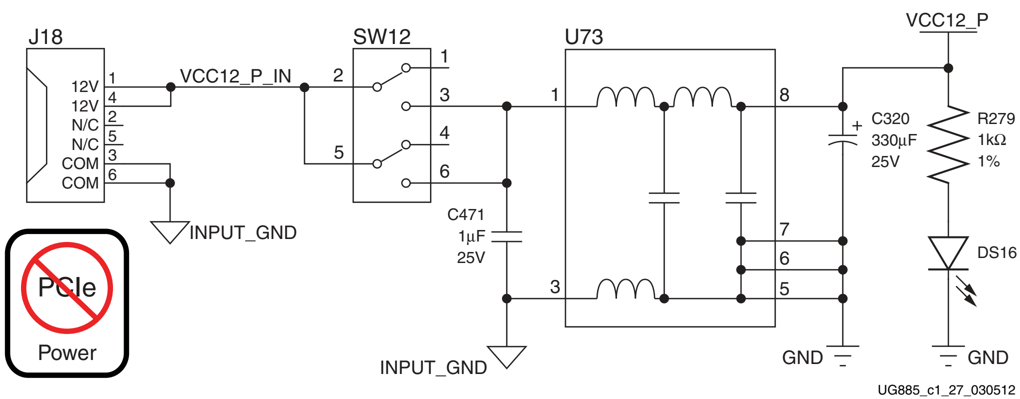

Figure 1-30: **Power On/Off Switch SW15**

FPGA_PROG_B Pushbutton SW9 (Active-Low)

[Figure 1-2, callout 28]

Switch SW9 grounds the FPGA's PROG_B pin when pressed. This action initiates an FPGA reconfiguration. The FPGA_PROG_B signal is connected to FPGA U1 pin AJ11.

See *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3] for further details on configuring the 7 series FPGAs.

Figure 1-31 shows SW9.

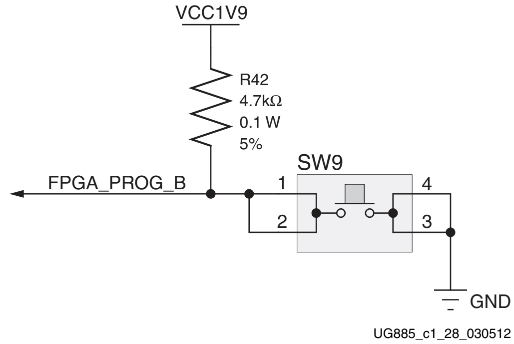

Figure 1-31: **FPGA_PROG_B Pushbutton SW9**

Configuration Mode and Upper Linear Flash Address Switch (SW11)

[Figure 1-2, callout 29]

FPGA Configuration Mode: DIP switch SW11 positions 3, 4, and 5 control which configuration mode is used at power-up or when the PROG pushbutton is pressed.

Linear BPI Flash Upper Addresses: DIP switch SW11 positions 1 and 2 control the setting of address bits FLASH_A25 and FLASH_A24. The mode signals FPGA_M2, _M1 and _M0 are connected to FPGA U1 pins AJ10, AK10 and AL10 respectively. Configuration mode is used at power-up or when the PROG pushbutton is pressed.

Figure 1-32 shows the SW11 circuit.

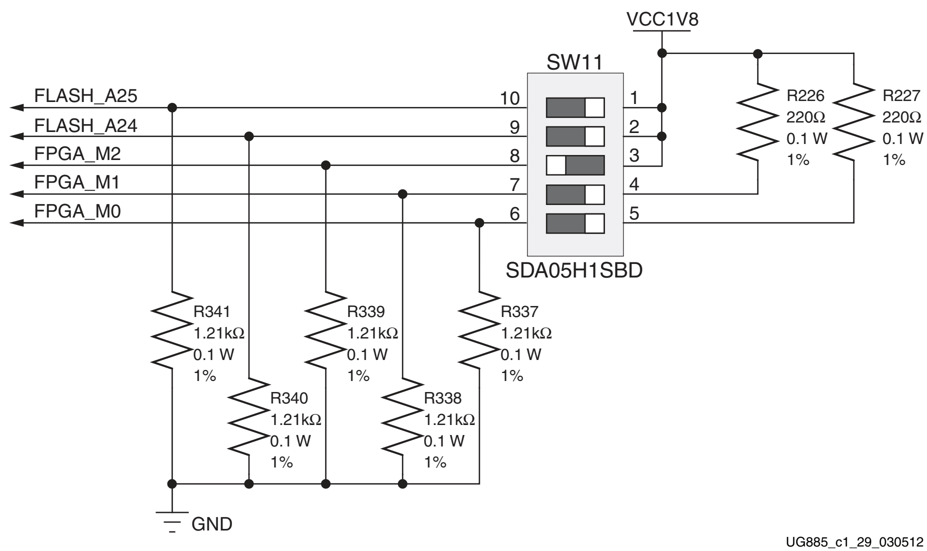

Figure 1-32: **Configuration Mode and Upper Linear Flash Address Switch**

VITA 57.1 FMC1 HPC Connector (Partially Populated)

[Figure 1-2, callout 30]

The VC707 board implements two instances of the FMC HPC VITA 57.1 specification connector. This section discusses the FMC1 HPC J35 connector.

Note: The FMC1 HPC J35 connector is a keyed connector oriented so that a plug-on card faces away from the VC707 board.

The VITA 57.1 FMC standard calls for two connector densities: a high pin count (HPC) and a low pin count (LPC) implementation. A 400 pin 10 x 40 position connector form factor is used for both versions. The HPC version is fully populated with all 400 pins present. The LPC version is partially populated with 160 pins.

The 10 x 40 rows of an FMC HPC connector provides pins for up to:

- 160 single-ended or 80 differential user-defined signals
- 10 GTX transceivers
- 2 GTX clocks
- 4 differential clocks
- 159 ground and 15 power connections

The VC707 board FMC1 HPC connector J35 implements a subset of the maximum signal and clock connectivity capabilities:

- 80 differential user-defined pairs
- 34 LA pairs (LA00-LA33)
- 24 HA pairs (HA00-HA23)
- 22 HB pairs (HB00-HB21)
- 8 GTX transceivers
- 2 GTX clocks
- 2 differential clocks

The FMC1 HPC signals are distributed across GTX Quads 118 and 119. Each Quad has the VCCO voltage connected to VADJ.

Note: The VC707 board VADJ voltage for the FMC1 HPC (J35) connector is determined by the FMC VADJ power sequencing logic described in FMC_VADJ Voltage Control.

VITA 57.1 FMC2 HPC Connector (Partially Populated)

[Figure 1-2, callout 31]

The VC707 board implements two instances of the FMC HPC VITA 57.1 specification connector. This section discusses the FMC2 HPC J37 connector.

Note: The FMC2 HPC J37 connector is a keyed connector oriented so that a plug-on card faces away from the VC707 board.

The FMC standard calls for two connector densities: a High Pin Count (HPC) and a Low Pin Count (LPC) implementation. A 400 pin 10 x 40 position connector form factor is used for both versions. The HPC version is fully populated with all 400 pins present. The LPC version is partially populated with 160 pins.

The 10 x 40 rows of an FMC HPC connector provides pins for up to:

- 160 single-ended or 80 differential user-defined signals
- 10 GTX transceivers
- 2 GTX clocks
- 4 differential clocks
- 159 ground and 15 power connections

The VC707 board FMC2 HPC connector J37 implements a subset of the maximum signal and clock connectivity capabilities:

- 58 differential user-defined pairs (as shipped with the Virtex-7 XC7VX485T-2FFG1761C FPGA installed on the VC707 board, the FMC2 HB00-HB21 bus connections are not supported. Refer to the Virtex-7 FPGA VC707 Evaluation Kit Master Answer Record in Appendix G: References for more information).
- 34 LA pairs (LA00-LA33)
- 24 HA pairs (HA00-HA23)
- 8 GTX transceivers
- 2 GTX clocks
- 2 differential clocks

The FMC2 HPC signals are distributed across GTX Quads 116 and 117. Each Quad has the VCCO voltage connected to VADJ.

Note: The VC707 board VADJ voltage for the FMC2 HPC (J37) connector is determined by the FMC VADJ power sequencing logic described in FMC_VADJ Voltage Control.

Signaling Speed Ratings:

- Single-ended: 9 GHz (18 Gb/s)
- Differential
  - Optimal Vertical: 9 GHz (18 Gb/s)
  - Optimal Horizontal: 16 GHz (32 Gb/s)
  - High Density Vertical: 7 GHz (15 Gb/s)

Mechanical specifications:

- Samtec SEAM/SEAF Series
- 1.27 mm x 1.27 mm (0.050" x 0.050") pitch

The Samtec connector system is rated for signaling speeds up to 9 GHz (18 Gb/s) based on a -3 dB insertion loss point within a two-level signaling environment.

Table 1-27 lists the connections between the FMC1 HPC J35 connector and the FPGA U1.

Table 1-27: **J35 VITA 57.1 FMC HPC Connections**

J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
A2	FMC1_HPC_DP1_M2C_P	(1)	C6	B1	NC		
A3	FMC1_HPC_DP1_M2C_N	(1)	C5	B4	NC		
A6	FMC1_HPC_DP2_M2C_P	(1)	B8	B5	NC		
A7	FMC1_HPC_DP2_M2C_N	(1)	B7	B8	NC		
A10	FMC1_HPC_DP3_M2C_P	(1)	A6	B9	NC		
A11	FMC1_HPC_DP3_M2C_N	(1)	A5	B12	FMC1_HPC_DP7_M2C_P	(1)	E6
A14	FMC1_HPC_DP4_M2C_P	(1)	H8	B13	FMC1_HPC_DP7_M2C_N	(1)	E5
A15	FMC1_HPC_DP4_M2C_N	(1)	H7	B16	FMC1_HPC_DP6_M2C_P	(1)	F8
A18	FMC1_HPC_DP5_M2C_P	(1)	G6	B17	FMC1_HPC_DP6_M2C_N	(1)	F7
A19	FMC1_HPC_DP5_M2C_N	(1)	G5	B20	FMC1_HPC_GBTCLK1_M2C_P	(1)	E10
A22	FMC1_HPC_DP1_C2M_P	(1)	D4	B21	FMC1_HPC_GBTCLK1_M2C_N	(1)	E9
A23	FMC1_HPC_DP1_C2M_N	(1)	D3	B24	NC		
A26	FMC1_HPC_DP2_C2M_P	(1)	C2	B25	NC		
A27	FMC1_HPC_DP2_C2M_N	(1)	C1	B28	NC		
A30	FMC1_HPC_DP3_C2M_P	(1)	B4	B29	NC		
A31	FMC1_HPC_DP3_C2M_N	(1)	B3	B32	FMC1_HPC_DP7_C2M_P	(1)	F4
A34	FMC1_HPC_DP4_C2M_P	(1)	J2	B33	FMC1_HPC_DP7_C2M_N	(1)	F3
A35	FMC1_HPC_DP4_C2M_N	(1)	J1	B36	FMC1_HPC_DP6_C2M_P	(1)	G2
A38	FMC1_HPC_DP5_C2M_P	(1)	H4	B37	FMC1_HPC_DP6_C2M_N	(1)	G1
A39	FMC1_HPC_DP5_C2M_N	(1)	H3	B40	NC		

Table 1-27: **J35 VITA 57.1 FMC HPC Connections *(Cont'd)***

J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
C2	FMC1_HPC_DP0_C2M_P	(1)	E2	D1	PWRCTL1_VCC4B_PG		AL32
C3	FMC1_HPC_DP0_C2M_N	(1)	E1	D4	FMC1_HPC_GBTCLK0_M2C_P	(1)	A10
C6	FMC1_HPC_DP0_M2C_P	(1)	D8	D5	FMC1_HPC_GBTCLK0_M2C_N	(1)	A9
C7	FMC1_HPC_DP0_M2C_N	(1)	D7	D8	FMC1_HPC_LA01_CC_P	LVCMOS18	J40
C10	FMC1_HPC_LA06_P	LVCMOS18	K42	D9	FMC1_HPC_LA01_CC_N	LVCMOS18	J41
C11	FMC1_HPC_LA06_N	LVCMOS18	J42	D11	FMC1_HPC_LA05_P	LVCMOS18	M41
C14	FMC1_HPC_LA10_P	LVCMOS18	N38	D12	FMC1_HPC_LA05_N	LVCMOS18	L41
C15	FMC1_HPC_LA10_N	LVCMOS18	M39	D14	FMC1_HPC_LA09_P	LVCMOS18	R42
C18	FMC1_HPC_LA14_P	LVCMOS18	N39	D15	FMC1_HPC_LA09_N	LVCMOS18	P42
C19	FMC1_HPC_LA14_N	LVCMOS18	N40	D17	FMC1_HPC_LA13_P	LVCMOS18	H39
C22	FMC1_HPC_LA18_CC_P	LVCMOS18	M32	D18	FMC1_HPC_LA13_N	LVCMOS18	G39
C23	FMC1_HPC_LA18_CC_N	LVCMOS18	L32	D20	FMC1_HPC_LA17_CC_P	LVCMOS18	L31
C26	FMC1_HPC_LA27_P	LVCMOS18	J31	D21	FMC1_HPC_LA17_CC_N	LVCMOS18	K32
C27	FMC1_HPC_LA27_N	LVCMOS18	H31	D23	FMC1_HPC_LA23_P	LVCMOS18	P30
C30	FMC1_HPC_IIC_SCL		U52.4	D24	FMC1_HPC_LA23_N	LVCMOS18	N31
C31	FMC1_HPC_IIC_SDA		U52.3	D26	FMC1_HPC_LA26_P	LVCMOS18	J30
C34	GA0 = 0 = GND			D27	FMC1_HPC_LA26_N	LVCMOS18	H30
C35	VCC12_P			D29	FMC1_HPC_TCK_BUF		U19.14
C37	VCC12_P			D30	FMC_TDI_BUF		U19.18
C39	VCC3V3			D31	FMC1_TDO_FMC2_TDI		U27.2
				D32	VCC3V3		
				D33	FMC1_HPC_TMS_BUF		U19.17
				D34	NC		
				D35	GA1 = 0 = GND		
				D36	VCC3V3		
				D38	VCC3V3		
				D40	VCC3V3		

Table 1-27: **J35 VITA 57.1 FMC HPC Connections *(Cont'd)***

J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
E2	FMC1_HPC_HA01_CC_P	LVCMOS18	D35	F1	FMC1_HPC_PG_M2C	LVCMOS18	AN34
E3	FMC1_HPC_HA01_CC_N	LVCMOS18	D36	F4	FMC1_HPC_HA00_CC_P	LVCMOS18	E34
E6	FMC1_HPC_HA05_P	LVCMOS18	G32	F5	FMC1_HPC_HA00_CC_N	LVCMOS18	E35
E7	FMC1_HPC_HA05_N	LVCMOS18	F32	F7	FMC1_HPC_HA04_P	LVCMOS18	F34
E9	FMC1_HPC_HA09_P	LVCMOS18	E32	F8	FMC1_HPC_HA04_N	LVCMOS18	F35
E10	FMC1_HPC_HA09_N	LVCMOS18	D32	F10	FMC1_HPC_HA08_P	LVCMOS18	J36
E12	FMC1_HPC_HA13_P	LVCMOS18	B36	F11	FMC1_HPC_HA08_N	LVCMOS18	H36
E13	FMC1_HPC_HA13_N	LVCMOS18	A37	F13	FMC1_HPC_HA12_P	LVCMOS18	B37
E15	FMC1_HPC_HA16_P	LVCMOS18	B39	F14	FMC1_HPC_HA12_N	LVCMOS18	B38
E16	FMC1_HPC_HA16_N	LVCMOS18	A39	F16	FMC1_HPC_HA15_P	LVCMOS18	C33
E18	FMC1_HPC_HA20_P	LVCMOS18	B34	F17	FMC1_HPC_HA15_N	LVCMOS18	C34
E19	FMC1_HPC_HA20_N	LVCMOS18	A34	F19	FMC1_HPC_HA19_P	LVCMOS18	B32
E21	FMC1_HPC_HB03_P	LVCMOS18	G28	F20	FMC1_HPC_HA19_N	LVCMOS18	B33
E22	FMC1_HPC_HB03_N	LVCMOS18	G29	F22	FMC1_HPC_HB02_P	LVCMOS18	K28
E24	FMC1_HPC_HB05_P	LVCMOS18	K27	F23	FMC1_HPC_HB02_N	LVCMOS18	J28
E25	FMC1_HPC_HB05_N	LVCMOS18	J27	F25	FMC1_HPC_HB04_P	LVCMOS18	H24
E27	FMC1_HPC_HB09_P	LVCMOS18	H23	F26	FMC1_HPC_HB04_N	LVCMOS18	G24
E28	FMC1_HPC_HB09_N	LVCMOS18	G23	F28	FMC1_HPC_HB08_P	LVCMOS18	H25
E30	FMC1_HPC_HB13_P	LVCMOS18	P25	F29	FMC1_HPC_HB08_N	LVCMOS18	H26
E31	FMC1_HPC_HB13_N	LVCMOS18	P26	F31	FMC1_HPC_HB12_P	LVCMOS18	K24
E33	FMC1_HPC_HB19_P	LVCMOS18	L25	F32	FMC1_HPC_HB12_N	LVCMOS18	K25
E34	FMC1_HPC_HB19_N	LVCMOS18	L26	F34	FMC1_HPC_HB16_P	LVCMOS18	N25
E36	FMC1_HPC_HB21_P	LVCMOS18	P22	F35	FMC1_HPC_HB16_N	LVCMOS18	N26
E37	FMC1_HPC_HB21_N	LVCMOS18	P23	F37	FMC1_HPC_HB20_P	LVCMOS18	P21
E39	VADJ			F38	FMC1_HPC_HB20_N	LVCMOS18	N21
				F40	VADJ		

Table 1-27: **J35 VITA 57.1 FMC HPC Connections *(Cont'd)***

J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
G2	FMC1_HPC_CLK1_M2C_P	LVCMOS18	N30	H1	NC		
G3	FMC1_HPC_CLK1_M2C_N	LVCMOS18	M31	H2	FMC1_HPC_PRSNT_M2C_B	LVCMOS18	AM31
G6	FMC1_HPC_LA00_CC_P	LVCMOS18	K39	H4	FMC1_HPC_CLK0_M2C_P	LVCMOS18	L39
G7	FMC1_HPC_LA00_CC_N	LVCMOS18	K40	H5	FMC1_HPC_CLK0_M2C_N	LVCMOS18	L40
G9	FMC1_HPC_LA03_P	LVCMOS18	M42	H7	FMC1_HPC_LA02_P	LVCMOS18	P41
G10	FMC1_HPC_LA03_N	LVCMOS18	L42	H8	FMC1_HPC_LA02_N	LVCMOS18	N41
G12	FMC1_HPC_LA08_P	LVCMOS18	M37	H10	FMC1_HPC_LA04_P	LVCMOS18	H40
G13	FMC1_HPC_LA08_N	LVCMOS18	M38	H11	FMC1_HPC_LA04_N	LVCMOS18	H41
G15	FMC1_HPC_LA12_P	LVCMOS18	R40	H13	FMC1_HPC_LA07_P	LVCMOS18	G41
G16	FMC1_HPC_LA12_N	LVCMOS18	P40	H14	FMC1_HPC_LA07_N	LVCMOS18	G42
G18	FMC1_HPC_LA16_P	LVCMOS18	K37	H16	FMC1_HPC_LA11_P	LVCMOS18	F40
G19	FMC1_HPC_LA16_N	LVCMOS18	K38	H17	FMC1_HPC_LA11_N	LVCMOS18	F41
G21	FMC1_HPC_LA20_P	LVCMOS18	Y29	H19	FMC1_HPC_LA15_P	LVCMOS18	M36
G22	FMC1_HPC_LA20_N	LVCMOS18	Y30	H20	FMC1_HPC_LA15_N	LVCMOS18	L37
G24	FMC1_HPC_LA22_P	LVCMOS18	R28	H22	FMC1_HPC_LA19_P	LVCMOS18	W30
G25	FMC1_HPC_LA22_N	LVCMOS18	P28	H23	FMC1_HPC_LA19_N	LVCMOS18	W31
G27	FMC1_HPC_LA25_P	LVCMOS18	K29	H25	FMC1_HPC_LA21_P	LVCMOS18	N28
G28	FMC1_HPC_LA25_N	LVCMOS18	K30	H26	FMC1_HPC_LA21_N	LVCMOS18	N29
G30	FMC1_HPC_LA29_P	LVCMOS18	T29	H28	FMC1_HPC_LA24_P	LVCMOS18	R30
G31	FMC1_HPC_LA29_N	LVCMOS18	T30	H29	FMC1_HPC_LA24_N	LVCMOS18	P31
G33	FMC1_HPC_LA31_P	LVCMOS18	M28	H31	FMC1_HPC_LA28_P	LVCMOS18	L29
G34	FMC1_HPC_LA31_N	LVCMOS18	M29	H32	FMC1_HPC_LA28_N	LVCMOS18	L30
G36	FMC1_HPC_LA33_P	LVCMOS18	U31	H34	FMC1_HPC_LA30_P	LVCMOS18	V30
G37	FMC1_HPC_LA33_N	LVCMOS18	T31	H35	FMC1_HPC_LA30_N	LVCMOS18	V31
G39	VADJ			H37	FMC1_HPC_LA32_P	LVCMOS18	V29
				H38	FMC1_HPC_LA32_N	LVCMOS18	U29
				H40	VADJ		

Table 1-27: **J35 VITA 57.1 FMC HPC Connections *(Cont'd)***

J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin		J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
J2	NC				K1	NC		
J3	NC				K4	NC		
J6	FMC1_HPC_HA03_P	LVCMOS18	H33		K5	NC		
J7	FMC1_HPC_HA03_N	LVCMOS18	G33		K7	FMC1_HPC_HA02_P	LVCMOS18	E33
J9	FMC1_HPC_HA07_P	LVCMOS18	C38		K8	FMC1_HPC_HA02_N	LVCMOS18	D33
J10	FMC1_HPC_HA07_N	LVCMOS18	C39		K10	FMC1_HPC_HA06_P	LVCMOS18	G36
J12	FMC1_HPC_HA11_P	LVCMOS18	J37		K11	FMC1_HPC_HA06_N	LVCMOS18	G37
J13	FMC1_HPC_HA11_N	LVCMOS18	J38		K13	FMC1_HPC_HA10_P	LVCMOS18	H38
J15	FMC1_HPC_HA14_P	LVCMOS18	E37		K14	FMC1_HPC_HA10_N	LVCMOS18	G38
J16	FMC1_HPC_HA14_N	LVCMOS18	E38		K16	FMC1_HPC_HA17_CC_P	LVCMOS18	C35
J18	FMC1_HPC_HA18_P	LVCMOS18	F39		K17	FMC1_HPC_HA17_CC_N	LVCMOS18	C36
J19	FMC1_HPC_HA18_N	LVCMOS18	E39		K19	FMC1_HPC_HA21_P	LVCMOS18	D37
J21	FMC1_HPC_HA22_P	LVCMOS18	F36		K20	FMC1_HPC_HA21_N	LVCMOS18	D38
J22	FMC1_HPC_HA22_N	LVCMOS18	F37		K22	FMC1_HPC_HA23_P	LVCMOS18	A35
J24	FMC1_HPC_HB01_P	LVCMOS18	H28		K23	FMC1_HPC_HA23_N	LVCMOS18	A36
J25	FMC1_HPC_HB01_N	LVCMOS18	H29		K25	FMC1_HPC_HB00_CC_P	LVCMOS18	J25
J27	FMC1_HPC_HB07_P	LVCMOS18	G26		K26	FMC1_HPC_HB00_CC_N	LVCMOS18	J26
J28	FMC1_HPC_HB07_N	LVCMOS18	G27		K28	FMC1_HPC_HB06_CC_P	LVCMOS18	K23
J30	FMC1_HPC_HB11_P	LVCMOS18	K22		K29	FMC1_HPC_HB06_CC_N	LVCMOS18	J23
J31	FMC1_HPC_HB11_N	LVCMOS18	J22		K31	FMC1_HPC_HB10_P	LVCMOS18	M22
J33	FMC1_HPC_HB15_P	LVCMOS18	M21		K32	FMC1_HPC_HB10_N	LVCMOS18	L22
J34	FMC1_HPC_HB15_N	LVCMOS18	L21		K34	FMC1_HPC_HB14_P	LVCMOS18	J21
J36	FMC1_HPC_HB18_P	LVCMOS18	G21		K35	FMC1_HPC_HB14_N	LVCMOS18	H21
J37	FMC1_HPC_HB18_N	LVCMOS18	G22		K37	FMC1_HPC_HB17_CC_P	LVCMOS18	M24
					K38	FMC1_HPC_HB17_CC_N	LVCMOS18	L24
J39	FMC1_VIO_B_M2C		BANK 36 VCCO		K40	FMC1_VIO_B_M2C		BANK 36 VCCO

Notes:

1. No I/O standards are associated with MGT connections.

Table 1-28 lists the connections between the FMC2 HPC J37 connector and the FPGA U1.

Note: The FMC2 HPC HB00-HB21 pair connections are not available with the XC7VX485T-2FFG1761C FPGA installed on the VC707. Refer to the Virtex-7 FPGA VC707 Evaluation Kit Master Answer Record in Appendix G: References for more information.

Table 1-28: **J37 VITA 57.1 FMC 2 HPC Connections**

J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin		J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
A2	FMC2_HPC_DP1_M2C_P	(1)	N6		B1	NC		
A3	FMC2_HPC_DP1_M2C_N	(1)	N5		B4	NC		
A6	FMC2_HPC_DP2_M2C_P	(1)	L6		B5	NC		
A7	FMC2_HPC_DP2_M2C_N	(1)	L5		B8	NC		
A10	FMC2_HPC_DP3_M2C_P	(1)	J6		B9	NC		
A11	FMC2_HPC_DP3_M2C_N	(1)	J5		B12	FMC2_HPC_DP7_M2C_P	(1)	R6
A14	FMC2_HPC_DP4_M2C_P	(1)	W6		B13	FMC2_HPC_DP7_M2C_N	(1)	R5
A15	FMC2_HPC_DP4_M2C_N	(1)	W5		B16	FMC2_HPC_DP6_M2C_P	(1)	U6
A18	FMC2_HPC_DP5_M2C_P	(1)	V4		B17	FMC2_HPC_DP6_M2C_N	(1)	U5
A19	FMC2_HPC_DP5_M2C_N	(1)	V3		B20	FMC2_HPC_GBTCLK1_M2C_P	(1)	T8
A22	FMC2_HPC_DP1_C2M_P	(1)	M4		B21	FMC2_HPC_GBTCLK1_M2C_N	(1)	T7
A23	FMC2_HPC_DP1_C2M_N	(1)	M3		B24	NC		
A26	FMC2_HPC_DP2_C2M_P	(1)	L2		B25	NC		
A27	FMC2_HPC_DP2_C2M_N	(1)	L1		B28	NC		
A30	FMC2_HPC_DP3_C2M_P	(1)	K4		B29	NC		
A31	FMC2_HPC_DP3_C2M_N	(1)	K3		B32	FMC2_HPC_DP7_C2M_P	(1)	P4
A34	FMC2_HPC_DP4_C2M_P	(1)	U2		B33	FMC2_HPC_DP7_C2M_N	(1)	P3
A35	FMC2_HPC_DP4_C2M_N	(1)	U1		B36	FMC2_HPC_DP6_C2M_P	(1)	R2
A38	FMC2_HPC_DP5_C2M_P	(1)	T4		B37	FMC2_HPC_DP6_C2M_N	(1)	R1
A39	FMC2_HPC_DP5_C2M_N	(1)	T3		B40	NC		

Table 1-28: **J37 VITA 57.1 FMC 2 HPC Connections *(Cont'd)***

J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin		J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
C2	FMC2_HPC_DP0_C2M_P	(1)	N2		D1	PWRCTL1_VCC4B_PG		AL32
C3	FMC2_HPC_DP0_C2M_N	(1)	N1		D4	FMC2_HPC_GBTCLK0_M2C_P	(1)	K8
C6	FMC2_HPC_DP0_M2C_P	(1)	P8		D5	FMC2_HPC_GBTCLK0_M2C_N	(1)	K7
C7	FMC2_HPC_DP0_M2C_N	(1)	P7		D8	FMC2_HPC_LA01_CC_P	LVCMOS18	AF41
C10	FMC2_HPC_LA06_P	LVCMOS18	AD38		D9	FMC2_HPC_LA01_CC_N	LVCMOS18	AG41
C11	FMC2_HPC_LA06_N	LVCMOS18	AE38		D11	FMC2_HPC_LA05_P	LVCMOS18	AF42
C14	FMC2_HPC_LA10_P	LVCMOS18	AB41		D12	FMC2_HPC_LA05_N	LVCMOS18	AG42
C15	FMC2_HPC_LA10_N	LVCMOS18	AB42		D14	FMC2_HPC_LA09_P	LVCMOS18	AJ38
C18	FMC2_HPC_LA14_P	LVCMOS18	AB38		D15	FMC2_HPC_LA09_N	LVCMOS18	AK38
C19	FMC2_HPC_LA14_N	LVCMOS18	AB39		D17	FMC2_HPC_LA13_P	LVCMOS18	W40
C22	FMC2_HPC_LA18_CC_P	LVCMOS18	U36		D18	FMC2_HPC_LA13_N	LVCMOS18	Y40
C23	FMC2_HPC_LA18_CC_N	LVCMOS18	T37		D20	FMC2_HPC_LA17_CC_P	LVCMOS18	U37
C26	FMC2_HPC_LA27_P	LVCMOS18	P32		D21	FMC2_HPC_LA17_CC_N	LVCMOS18	U38
C27	FMC2_HPC_LA27_N	LVCMOS18	P33		D23	FMC2_HPC_LA23_P	LVCMOS18	R38
C30	FMC2_HPC_IIC_SCL		U52.6		D24	FMC2_HPC_LA23_N	LVCMOS18	R39
C31	FMC2_HPC_IIC_SDA		U52.5		D26	FMC2_HPC_LA26_P	LVCMOS18	N33
C34	GA0 = 0 = GND				D27	FMC2_HPC_LA26_N	LVCMOS18	N34
C35	VCC12_P				D29	FMC2_HPC_TCK_BUF		U19.13
C37	VCC12_P				D30	FMC1_TDO_FMC2_TDI		U27.2
C39	VCC3V3				D31	FMC2_TDO_FPGA_TDI		U46.3
					D32	VCC3V3		
					D33	FMC2_HPC_TMS_BUF		U19.16
					D34	NC		
					D35	GA1 = 0 = GND		
					D36	VCC3V3		
					D38	VCC3V3		
					D40	VCC3V3		

Table 1-28: **J37 VITA 57.1 FMC 2 HPC Connections *(Cont'd)***

J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin		J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
E2	FMC2_HPC_HA01_CC_P	LVCMOS18	AD32		F1	FMC2_HPC_PG_M2C	LVCMOS18	AF29
E3	FMC2_HPC_HA01_CC_N	LVCMOS18	AD33		F4	FMC2_HPC_HA00_CC_P	LVCMOS18	AB33
E6	FMC2_HPC_HA05_P	LVCMOS18	Y32		F5	FMC2_HPC_HA00_CC_N	LVCMOS18	AC33
E7	FMC2_HPC_HA05_N	LVCMOS18	Y33		F7	FMC2_HPC_HA04_P	LVCMOS18	AB29
E9	FMC2_HPC_HA09_P	LVCMOS18	AE29		F8	FMC2_HPC_HA04_N	LVCMOS18	AC29
E10	FMC2_HPC_HA09_N	LVCMOS18	AE30		F10	FMC2_HPC_HA08_P	LVCMOS18	AA31
E12	FMC2_HPC_HA13_P	LVCMOS18	AE32		F11	FMC2_HPC_HA08_N	LVCMOS18	AA32
E13	FMC2_HPC_HA13_N	LVCMOS18	AE33		F13	FMC2_HPC_HA12_P	LVCMOS18	AF34
E15	FMC2_HPC_HA16_P	LVCMOS18	AG36		F14	FMC2_HPC_HA12_N	LVCMOS18	AG34
E16	FMC2_HPC_HA16_N	LVCMOS18	AH36		F16	FMC2_HPC_HA15_P	LVCMOS18	AE37
E18	FMC2_HPC_HA20_P	LVCMOS18	AD36		F17	FMC2_HPC_HA15_N	LVCMOS18	AF37
E19	FMC2_HPC_HA20_N	LVCMOS18	AD37		F19	FMC2_HPC_HA19_P	LVCMOS18	AC35
E21	FMC2_HPC_HB03_P	LVCMOS18	AT16		F20	FMC2_HPC_HA19_N	LVCMOS18	AC36
E22	FMC2_HPC_HB03_N	LVCMOS18	AU16		F22	FMC2_HPC_HB02_P	LVCMOS18	AV16
E24	FMC2_HPC_HB05_P	LVCMOS18	BA17		F23	FMC2_HPC_HB02_N	LVCMOS18	AW16
E25	FMC2_HPC_HB05_N	LVCMOS18	BB17		F25	FMC2_HPC_HB04_P	LVCMOS18	AU18
E27	FMC2_HPC_HB09_P	LVCMOS18	AV20		F26	FMC2_HPC_HB04_N	LVCMOS18	AV18
E28	FMC2_HPC_HB09_N	LVCMOS18	AW20		F28	FMC2_HPC_HB08_P	LVCMOS18	AY20
E30	FMC2_HPC_HB13_P	LVCMOS18	AT20		F29	FMC2_HPC_HB08_N	LVCMOS18	BA20
E31	FMC2_HPC_HB13_N	LVCMOS18	AT19		F31	FMC2_HPC_HB12_P	LVCMOS18	AU19
E33	FMC2_HPC_HB19_P	LVCMOS18	AP18		F32	FMC2_HPC_HB12_N	LVCMOS18	AV19
E34	FMC2_HPC_HB19_N	LVCMOS18	AP17		F34	FMC2_HPC_HB16_P	LVCMOS18	AR18
E36	FMC2_HPC_HB21_P	LVCMOS18	AN19		F35	FMC2_HPC_HB16_N	LVCMOS18	AR17
E37	FMC2_HPC_HB21_N	LVCMOS18	AN18		F37	FMC2_HPC_HB20_P	LVCMOS18	AK17
E39	VADJ				F38	FMC2_HPC_HB20_N	LVCMOS18	AL17
					F40	VADJ		

Table 1-28: **J37 VITA 57.1 FMC 2 HPC Connections *(Cont'd)***

J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin		J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
G2	FMC2_HPC_CLK1_M2C_P	LVCMOS18	U39		H1	NC		
G3	FMC2_HPC_CLK1_M2C_N	LVCMOS18	T39		H2	FMC2_HPC_PRSNT_M2C_B	LVCMOS18	AG32
G6	FMC2_HPC_LA00_CC_P	LVCMOS18	AD40		H4	FMC2_HPC_CLK0_M2C_P	LVCMOS18	AF39
G7	FMC2_HPC_LA00_CC_N	LVCMOS18	AD41		H5	FMC2_HPC_CLK0_M2C_N	LVCMOS18	AF40
G9	FMC2_HPC_LA03_P	LVCMOS18	AJ42		H7	FMC2_HPC_LA02_P	LVCMOS18	AK39
G10	FMC2_HPC_LA03_N	LVCMOS18	AK42		H8	FMC2_HPC_LA02_N	LVCMOS18	AL39
G12	FMC2_HPC_LA08_P	LVCMOS18	AD42		H10	FMC2_HPC_LA04_P	LVCMOS18	AL41
G13	FMC2_HPC_LA08_N	LVCMOS18	AE42		H11	FMC2_HPC_LA04_N	LVCMOS18	AL42
G15	FMC2_HPC_LA12_P	LVCMOS18	Y39		H13	FMC2_HPC_LA07_P	LVCMOS18	AC40
G16	FMC2_HPC_LA12_N	LVCMOS18	AA39		H14	FMC2_HPC_LA07_N	LVCMOS18	AC41
G18	FMC2_HPC_LA16_P	LVCMOS18	AJ40		H16	FMC2_HPC_LA11_P	LVCMOS18	Y42
G19	FMC2_HPC_LA16_N	LVCMOS18	AJ41		H17	FMC2_HPC_LA11_N	LVCMOS18	AA42
G21	FMC2_HPC_LA20_P	LVCMOS18	V33		H19	FMC2_HPC_LA15_P	LVCMOS18	AC38
G22	FMC2_HPC_LA20_N	LVCMOS18	V34		H20	FMC2_HPC_LA15_N	LVCMOS18	AC39
G24	FMC2_HPC_LA22_P	LVCMOS18	W32		H22	FMC2_HPC_LA19_P	LVCMOS18	U32
G25	FMC2_HPC_LA22_N	LVCMOS18	W33		H23	FMC2_HPC_LA19_N	LVCMOS18	U33
G27	FMC2_HPC_LA25_P	LVCMOS18	R33		H25	FMC2_HPC_LA21_P	LVCMOS18	P35
G28	FMC2_HPC_LA25_N	LVCMOS18	R34		H26	FMC2_HPC_LA21_N	LVCMOS18	P36
G30	FMC2_HPC_LA29_P	LVCMOS18	W36		H28	FMC2_HPC_LA24_P	LVCMOS18	U34
G31	FMC2_HPC_LA29_N	LVCMOS18	W37		H29	FMC2_HPC_LA24_N	LVCMOS18	T35
G33	FMC2_HPC_LA31_P	LVCMOS18	V39		H31	FMC2_HPC_LA28_P	LVCMOS18	V35
G34	FMC2_HPC_LA31_N	LVCMOS18	V40		H32	FMC2_HPC_LA28_N	LVCMOS18	V36
G36	FMC2_HPC_LA33_P	LVCMOS18	T36		H34	FMC2_HPC_LA30_P	LVCMOS18	T32
G37	FMC2_HPC_LA33_N	LVCMOS18	R37		H35	FMC2_HPC_LA30_N	LVCMOS18	R32
G39	VADJ				H37	FMC2_HPC_LA32_P	LVCMOS18	P37
					H38	FMC2_HPC_LA32_N	LVCMOS18	P38
					H40	VADJ		

Table 1-28: **J37 VITA 57.1 FMC 2 HPC Connections *(Cont'd)***

J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin		J37 FMC 2 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
J2	NC				K1	NC		
J3	NC				K4	NC		
J6	FMC2_HPC_HA03_P	LVCMOS18	AA29		K5	NC		
J7	FMC2_HPC_HA03_N	LVCMOS18	AA30		K7	FMC2_HPC_HA02_P	LVCMOS18	AC30
J9	FMC2_HPC_HA07_P	LVCMOS18	AC31		K8	FMC2_HPC_HA02_N	LVCMOS18	AD30
J10	FMC2_HPC_HA07_N	LVCMOS18	AD31		K10	FMC2_HPC_HA06_P	LVCMOS18	AB31
J12	FMC2_HPC_HA11_P	LVCMOS18	AE34		K11	FMC2_HPC_HA06_N	LVCMOS18	AB32
J13	FMC2_HPC_HA11_N	LVCMOS18	AE35		K13	FMC2_HPC_HA10_P	LVCMOS18	AF31
J15	FMC2_HPC_HA14_P	LVCMOS18	AF35		K14	FMC2_HPC_HA10_N	LVCMOS18	AF32
J16	FMC2_HPC_HA14_N	LVCMOS18	AF36		K16	FMC2_HPC_HA17_CC_P	LVCMOS18	AC34
J18	FMC2_HPC_HA18_P	LVCMOS18	AB36		K17	FMC2_HPC_HA17_CC_N	LVCMOS18	AD35
J19	FMC2_HPC_HA18_N	LVCMOS18	AB37		K19	FMC2_HPC_HA21_P	LVCMOS18	AA34
J21	FMC2_HPC_HA22_P	LVCMOS18	Y35		K20	FMC2_HPC_HA21_N	LVCMOS18	AA35
J22	FMC2_HPC_HA22_N	LVCMOS18	AA36		K22	FMC2_HPC_HA23_P	LVCMOS18	Y37
J24	FMC2_HPC_HB01_P	LVCMOS18	AM16		K23	FMC2_HPC_HA23_N	LVCMOS18	AA37
J25	FMC2_HPC_HB01_N	LVCMOS18	AN16		K25	FMC2_HPC_HB00_CC_P	LVCMOS18	AT17
J27	FMC2_HPC_HB07_P	LVCMOS18	BB19		K26	FMC2_HPC_HB00_CC_N	LVCMOS18	AU17
J28	FMC2_HPC_HB07_N	LVCMOS18	BB18		K28	FMC2_HPC_HB06_CC_P	LVCMOS18	AY18
J30	FMC2_HPC_HB11_P	LVCMOS18	AM18		K29	FMC2_HPC_HB06_CC_N	LVCMOS18	AY17
J31	FMC2_HPC_HB11_N	LVCMOS18	AM17		K31	FMC2_HPC_HB10_P	LVCMOS18	AP20
J33	FMC2_HPC_HB15_P	LVCMOS18	AL19		K32	FMC2_HPC_HB10_N	LVCMOS18	AR19
J34	FMC2_HPC_HB15_N	LVCMOS18	AM19		K34	FMC2_HPC_HB14_P	LVCMOS18	AK19
J36	FMC2_HPC_HB18_P	LVCMOS18	AJ18		K35	FMC2_HPC_HB14_N	LVCMOS18	AK18
J37	FMC2_HPC_HB18_N	LVCMOS18	AJ17		K37	FMC2_HPC_HB17_CC_P	LVCMOS18	AW18
					K38	FMC2_HPC_HB17_CC_N	LVCMOS18	AW17
J39	FMC2_VIO_B_M2C		BANK 32 VCCO		K40	FMC2_VIO_B_M2C		BANK 32 VCCO

Notes:

1. No I/O standards are associated with MGT connections.

Power Management

The VC707 board power distribution diagram is shown in Figure 1-33.

The PCB layout and power system meet the recommended criteria described in *7 Series FPGAs PCB Design Guide* (UG483) [Ref 10].

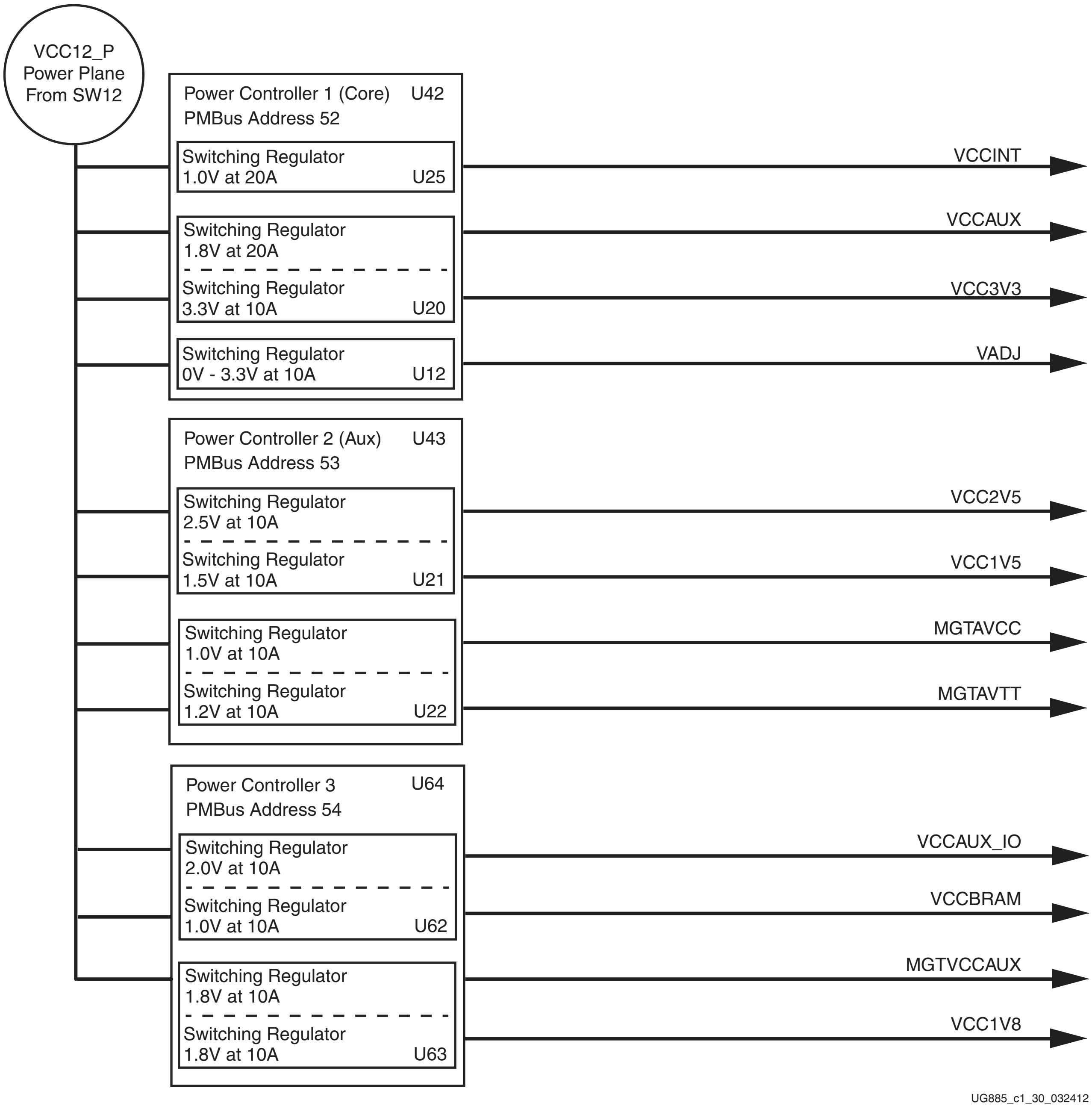

Figure 1-33: **Onboard Power Regulators**

The VC707 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the core and auxiliary voltages listed in Table 1-29.

Table 1-29: **Onboard Power System Devices**

Device Type	Reference Designator	Description	Power Rail Net Name	Power Rail Voltage	Schematic Page
Core voltage controller and regulators					
UCD9248PFC(1)	U42	PMBus Controller (Addr = 52)			46
PTD08A020W	U25	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCINT_FPGA	1.00V	47
PTD08D210W (V_{OUT} A)	U20	Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCCAUX	1.80V	48
PTD08D210W (V_{OUT} B)		Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCC3V3	3.30V	48
PTD08A010W	U12	Adjustable switching regulator 10A, 0.6V to 3.6V	VCC_ADJ	0-3.30V	49
Auxiliary voltage controller and regulators					
UCD9248PFC(2)	U43	PMBus Controller (Addr = 53)			50
PTD08D210W (V_{OUT} A)	U21	Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCC2V5_FPGA	2.50V	51
PTD08D210W (V_{OUT} B)		Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCC1V5_FPGA	1.50V	51
PTD08D210W (V_{OUT} A)	U22	Adjustable switching regulator dual 10A, 0.6Vto 3.6V	MGTAVCC	1.00V	52
PTD08D210W (V_{OUT} B)		Adjustable switching regulator dual 10A, 0.6Vto 3.6V	MGTAVTT	1.20V	52
UCD9248PFC(3)	U64	PMBus Controller (Addr = 54)			53
PTD08D210W (V_{OUT} A)	U62	Dual 10A 0.6V - 3.6V Adj. Switching Regulator	VCCAUX_IO	2.00V	54
PTD08D210W (V_{OUT} B)		Dual 10A 0.6V - 3.6V Adj. Switching Regulator	VCCBRAM	1.00V	54
PTD08D210W (V_{OUT} A)	U63	Dual 10A 0.6V - 3.6V Adj. Switching Regulator	MGTVCCAUX	1.80V	55
PTD08D021W (V_{OUT} B)		Dual 10A 0.6V - 3.6V Adj. Switching Regulator	VCCBRAM	1.00V	55
Linear regulators					
LMZ12002	U71	Fixed Linear Regulator 2A	VCC5V0	5.00V	46
TL1962ADC	U62	Fixed Linear Regulator, 1.5A	VCC1V8	1.80V	46
ADP123	U17	Fixed Linear Regulator, 300mA	VCC_SPI	2.80V	46
ADP123	U18	Fixed Linear Regulator, 300mA	XADC_VCC	1.80V	31

Table 1-29: **Onboard Power System Devices *(Cont'd)***

Device Type	Reference Designator	Description	Power Rail Net Name	Power Rail Voltage	Schematic Page
TPS51200DR	U33	Tracking Regulator, 3A	VTTDDR	0.75V	46

Notes:

1. See Table 1-30.
2. See Table 1-31.
3. See Table 1-34.

Data sheets for the Texas Instruments controller and regulators are available at the Texas Instruments website [Ref 25], and for the Analog Devices ADP123 at [Ref 26].

FMC_VADJ Voltage Control

The FMC_VADJ rail is set to 1.8V. When the VC707 board is powered on, the state of the FMC_VADJ_ON_B signal wired to header J51 is sampled by the TI UCD9248 controller U42. If a jumper is installed on J51 signal FMC_VADJ_ON_B is held low, and the TI controller U42 energizes the FMC_VADJ rail at power on.

Because the rail turn on decision is made at power on time based on the presence of the J51 jumper, removing the jumper at J51 after the board is powered up does not affect the 1.8V power delivered to the FMC_VADJ rail and it remains on.

A jumper installed at J51 is the default setting.

If a jumper is not installed on J51, signal FMC_VADJ_ON_B is high, and the VC707 board does not energize the FMC_VADJ 1.8V at power on. In this mode the user can control when to turn on FMC_VADJ and to what voltage level (1.2V, 1.5V, 1.8V). With FMC_VADJ off, the FPGA still configures and has access to the TI controller PMBUS along with the VADJ_ON_B signal. The combination of these allows the user to develop code to command the FMC_VADJ rail to be set to something other than the default setting of 1.8V. After the new FMC_VADJ voltage level has been programmed into TI controller U42, the VADJ_ON_B signal can be driven low by the user logic and the FMC_VADJ rail comes up at the new FMC_VADJ voltage level. Installing a jumper at J51 after a VC707 board powers up in this mode turns on the FMC_VADJ rail.

Documentation describing PMBUS programming for the UCD9248 digital power controller is available at the Texas Instruments website [Ref 25].

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface. The three onboard TI power controllers (U42 at address 52, U43 at address 53, and U64 at address 54) are wired to the same PMBus. The PMBus connector, J5, is provided for use with the TI USB Interface Adapter PMBus pod (TI part number EVM USB-TO-GPIO), which can be ordered from the TI website [Ref 25], and the associated TI Fusion Digital Power Designer GUI (downloadable from [Ref 25]). This is the simplest and most convenient way to monitor the voltage and current values for the power rail listed in Table 1-30, Table 1-31, and Table 1-32.

In each of these the three tables (one per controller), the Power Good (PG) On Threshold is the set-point at or above which the particular rail is deemed "good". The PG Off Threshold is the set-point at or below which the particular rail is no longer deemed "good". The controller internally OR's these PG conditions together and drives an output PG pin high only if all active rail PG states are "good". The On and Off Delay and rise and fall times are relative to when the board power on-off slide switch SW12 is turned on and off.

Table 1-30 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 52 (U42).

Table 1-30: **Power Rail Specifications for UCD9248 PMBus Controller at Address 52**

Rail Number	Rail Name	Schematic Rail Name	Nominal V_{OUT} (V)	PG On Threshold (V)	PG Off Threshold (V)	On Delay (ms)	Rise Time (ms)	Off Delay (ms)	Fall Time (ms)	Shutdown Threshold[1]		
										V_{OUT} Over Fault (V)	I_{OUT} Over Fault (A)	Temp Over Fault (°C)
1	Rail #1	VCCINT_FPGA	1	0.9	0.85	0	5	10	1	1.15	20	90
2	Rail #2	VCCAUX	1.8	1.62	1.53	0	5	5	1	2.07	10.41	90
3	Rail #3	VCC3V3	3.3	2.97	2.805	0	5	4	1	3.795	10.41	90
4	Rail #4	VADJ	1.8	1.62	1.53	0	5	3	1	2.07	10.41	90

Notes:

1. The values defined in these columns are the voltage, current, and temperature thresholds that cause the regulator to shut down if the value is exceeded.

Table 1-31 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 53 (U43).

Table 1-31: **Power Rail Specifications for UCD9248 PMBus Controller at Address 53**

Rail Number	Rail Name	Schematic Rail Name	Nominal V_{OUT} (V)	PG On Threshold (V)	PG Off Threshold (V)	On Delay (ms)	Rise Time (ms)	Off Delay (ms)	Fall Time (ms)	Shutdown Threshold[1]		
										V_{OUT} Over Fault (V)	I_{OUT} Over Fault (A)	Temp Over Fault (°C)
1	Rail #1	VCC2V5_FPGA	2.5	2.25	2.125	0	5	1	1	2.875	10.41	90
2	Rail #2	VCC1V5	1.5	1.35	1.275	0	5	0	1	1.725	10.41	90
3	Rail #3	MGTAVCC	1	0.9	0.85	0	5	7	1	1.45	10.41	90
4	Rail #4	MGTAVTT	1.2	1.08	1.02	0	5	8	1	1.38	10.41	90

Notes:

1. The values defined in these columns are the voltage, current, and temperature thresholds that causes the regulator to shut down if the value is exceeded.

Table 1-32 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 54 (U64).

Table 1-32: **Power Rail Specifications for UCD9248 PMBus Controller at Address 54**

Rail Number	Rail Name	Schematic Rail Name	Nominal V_{OUT} (V)	PG On Threshold (V)	PG Off Threshold (V)	On Delay (ms)	Rise Time (ms)	Off Delay (ms)	Fall Time (ms)	Shutdown Threshold[1]		
										V_{OUT} Over Fault (V)	I_{OUT} Over Fault (A)	Temp Over Fault (°C)
1	Rail #1	VCCAUX_IO	2	1.8	1.7	0	5	2	1	2.3	10.41	90
2	Rail #2	VCC_BRAM	1	0.9	0.85	0	5	9	1	1.15	10.41	90
3	Rail #3	MGTVCCAUX	1.8	1.62	1.53	0	5	7	1	2.07	10.41	90
4	Rail #4	VCC1V8_FPGA	1.8	1.62	1.53	0	5	5	1	2.07	10.41	90

Notes:

1. The values defined in these columns are the voltage, current, and temperature thresholds that cause the regulator to shut down if the value is exceeded.

FPGA Cooling Fan Operation

The FPGA cooling fan control circuit has its PWM signal wired to a dual-use FPGA Bank 15 pin BA37. After configuration, this pin is expected to be toggled by user-provided fan speed control IP to control fan speed.

FPGA U1 pin BA37 is alternately an unused BPI flash memory address pin (A28). During FPGA configuration in BPI mode, the BPI flash memory address lines are driven. The BA37 pin is held low during BPI configuration and thus the fan PWM signal is not active. The FPGA U1 cooling fan is off during the FPGA BPI configuration process.

After configuration is complete, the dual-use FPGA pin BA37 is available for use by user-provided fan speed control IP.

References

More information about the power system components used by the VC707 board are available from the Texas Instruments digital power website [Ref 25].

PCIe Form Factor Board TI Power System Cooling

If the power modules on the VC707 board are operating at moderate to high current levels (due to a customer design), the modules can generate substantial heat, which can cause them to shut down without warning. The power module shutdown then turns off the FPGA on the development board. Refer to the Virtex-7 FPGA VC707 Evaluation Kit Master Answer Record in Appendix G: References for more information.

XADC Analog-to-Digital Converter

7 series FPGAs provide an analog front end XADC block. The XADC block includes a dual 12-bit, 1 MSPS analog-to-digital convertor (ADC) and on-chip sensors. See *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 11] for details on the capabilities of the analog front end. Figure 1-34 shows the XADC block diagram.

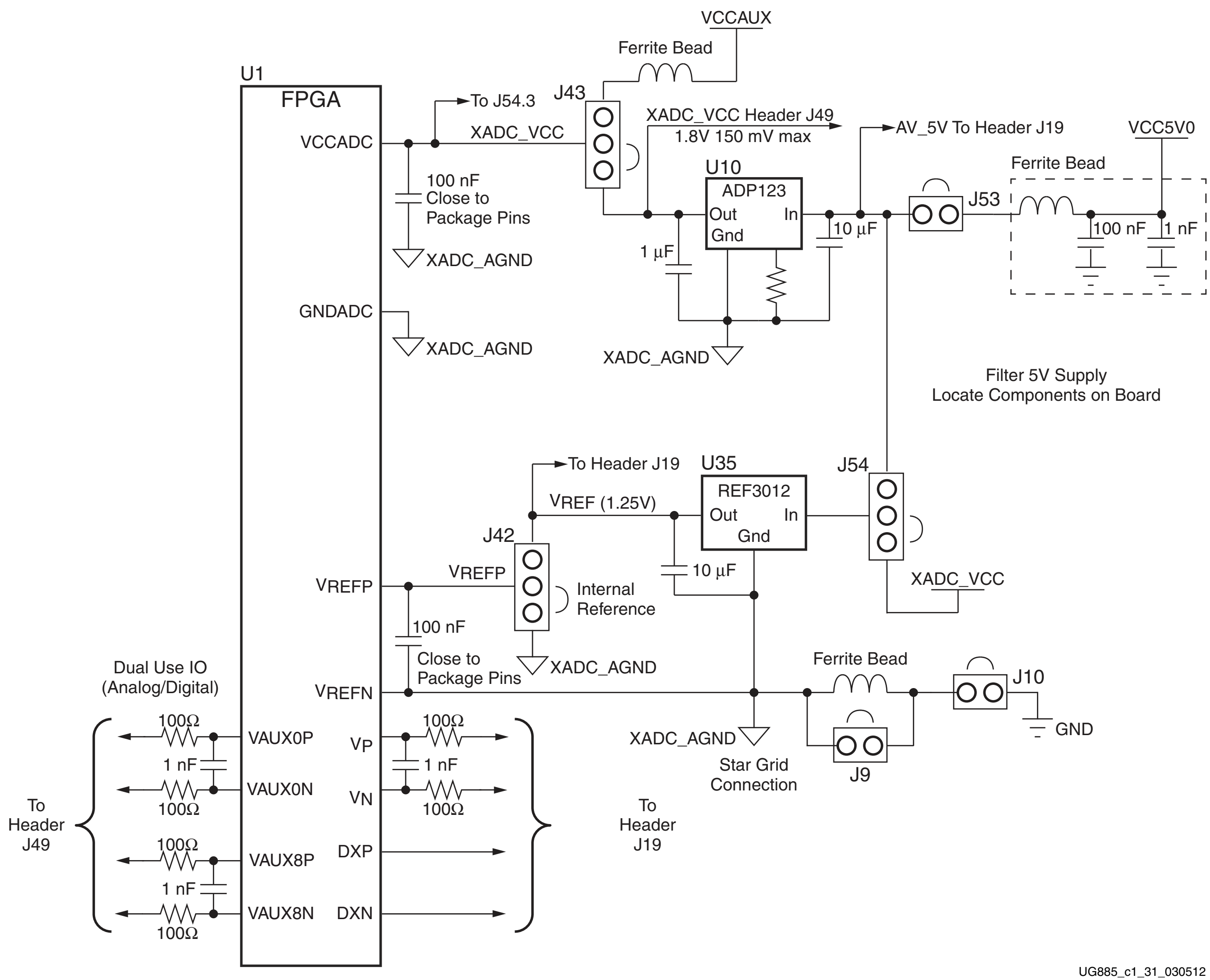

Figure 1-34: **XADC Block Diagram**

The VC707 board supports both the internal FPGA sensor measurements and the external measurement capabilities of the XADC. Internal measurements of the die temperature, VCCINT, VCCAUX, and VCCBRAM are available. The VC707 board VCCINT and VCCBRAM are provided by a common 1.0 V supply.

Jumper J42 can be used to select either an external differential voltage reference (VREF) or on-chip voltage reference for the analog-to-digital converter.

For external measurements an XADC header (J19) is provided. This header can be used to provide analog inputs to the FPGA's dedicated VP/VN channel, and to the VAUXP[0]/VAUXN[0], VAUXP[8]/VAUXN[8] auxiliary analog input channels. Simultaneous sampling of Channel 0 and Channel 8 is supported.

A user-provided analog signal multiplexer card can be used to sample additional external analog inputs using the 4 GPIO pins available on the XADC header as multiplexer address lines. Figure 1-35 shows the XADC header connections.

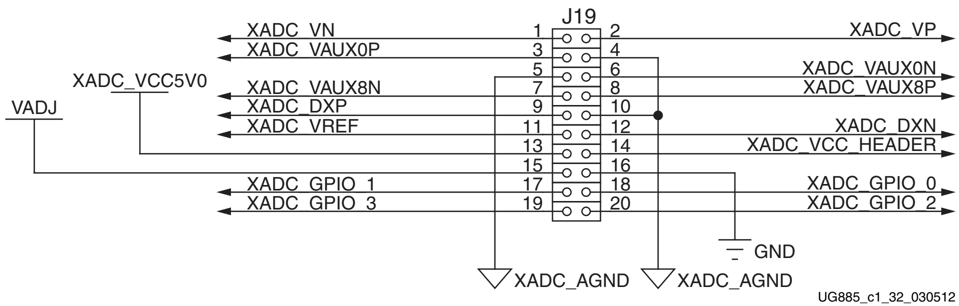

Figure 1-35: **XADC Header (J19)**

Table 1-33 describes the XADC header J19 pin functions.

Table 1-33: **XADC Header J19 Pinout**

Net Name	J19 Pin Number	Description
VN, VP	1, 2	Dedicated analog input channel for the XADC.
XADC_VAUX0P, N	3, 6	Auxiliary analog input channel 0. Also supports use as I/O inputs when anti-alias capacitor is not present.
XADC_VAUX8N, P	7, 8	Auxiliary analog input channel 8. Also supports use as I/O inputs when anti-alias capacitor is not present.
DXP, DXN	9, 12	Access to thermal diode.
XADC_AGND	4, 5, 10	Analog ground reference.
XADC_VREF	11	1.25V reference from the board.
XADC_VCC5V0	13	Filtered 5V supply from board.
XADC_VCC_HEADER	14	Analog 1.8V supply for XADC.
VADJ	15	VCCO supply for bank which is the source of DIO pins.
GND	16	Digital Ground (board) Reference
XADC_GPIO_3, 2, 1, 0	19, 20, 17, 18	Digital I/O. These pins should come from the same bank. These I/Os should not be shared with other functions because they are required to support 3-state operation.

Configuration Options

The FPGA on the VC707 board can be configured by the following methods:

- Master BPI (uses the Linear BPI Flash).
- JTAG (uses the USB-to-JTAG Bridge or Download cable). See USB JTAG for more information

See *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3] for further details on configuration modes.

The method used to configure the FPGA is controlled by the mode pin (M2, M1, M0) settings selected through DIP switch SW11. Table 1-34 lists the supported mode switch settings.

Table 1-34: **Mode Switch SW11 Settings**

Mode Pins (M2, M1, M0)	Configuration Mode
010	Master BPI
101	JTAG

Figure 1-36 shows mode switch SW13.

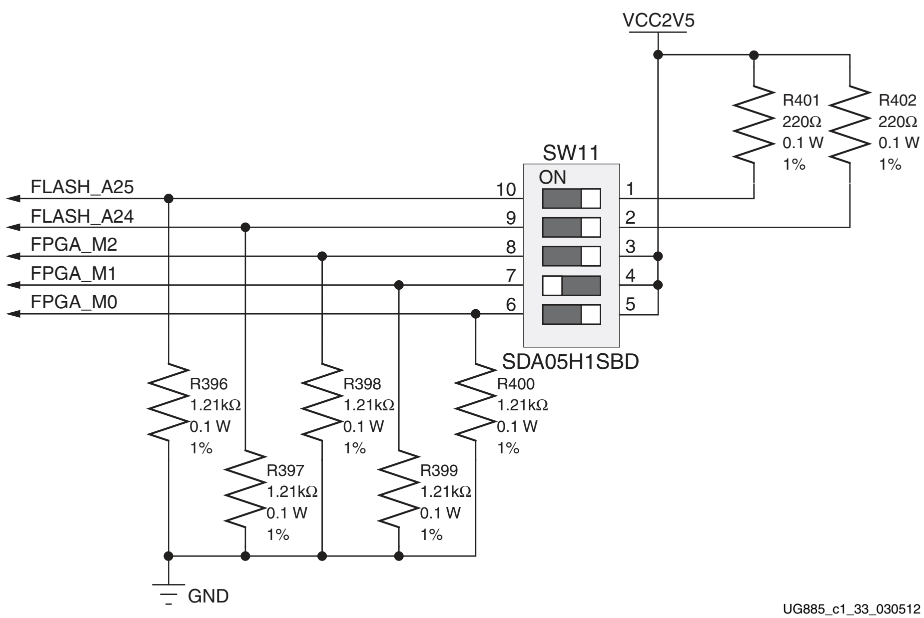

Figure 1-36: **Mode Switch**

The mode pins settings on SW11 determine if the Linear BPI Flash is used for configuring the FPGA. DIP switch SW11 also provides the upper two address bits for the Linear BPI Flash and can be used to select one of multiple stored configuration bitstreams. Figure 1-37 shows the connectivity between the onboard nonvolatile Flash devices used for configuration and the FPGA.

To obtain the fastest configuration speed an external 80 MHz oscillator is wired to the EMCCLK pin of the FPGA. This allows users to create bitstreams that configure the FPGA over the 16-bit datapath from the Linear BPI Flash memory at a maximum synchronous read rate of 80 MHz.

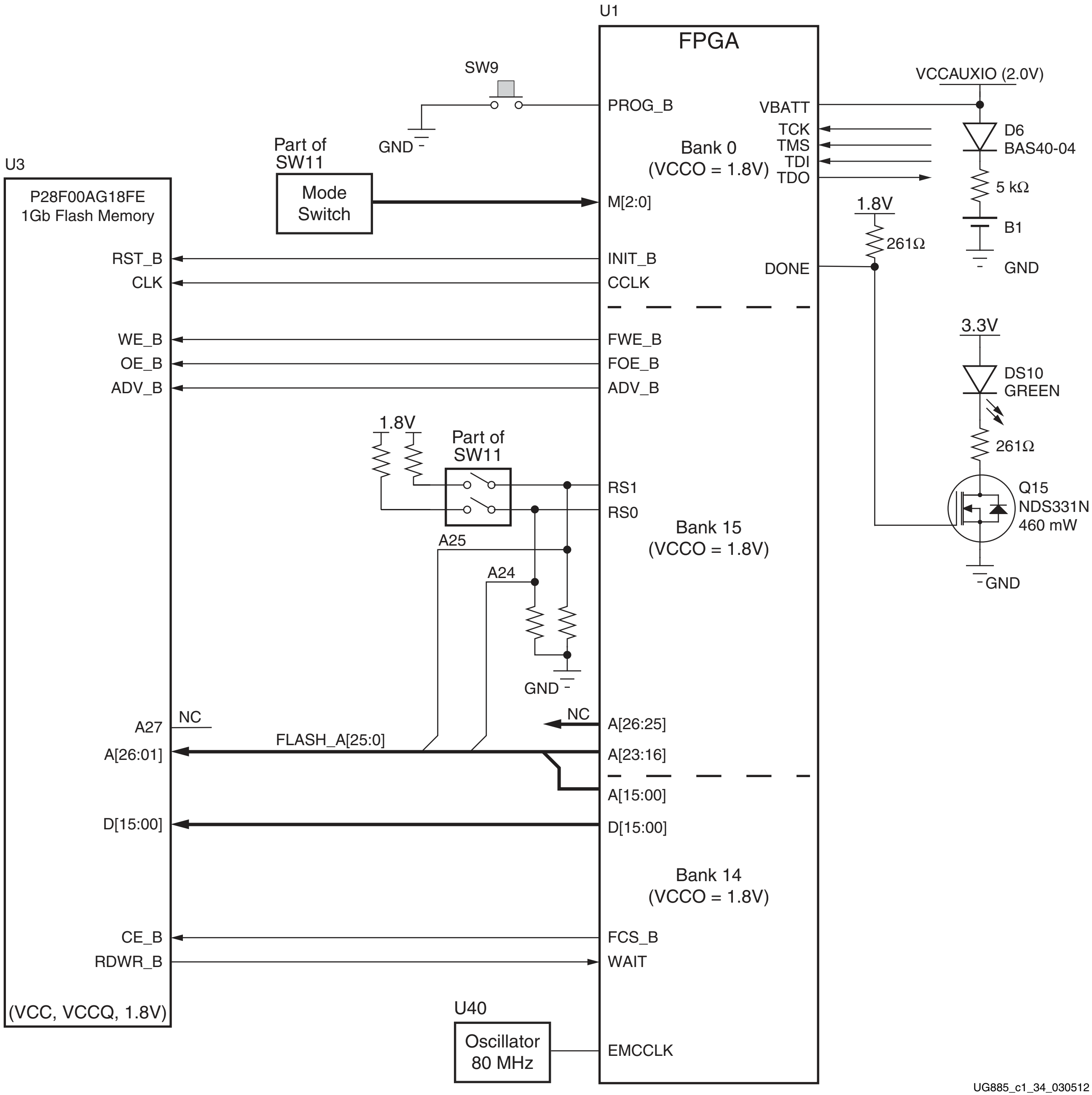

Figure 1-37: **VC707 Board Configuration Circuit**

Default Switch and Jumper Settings

GPIO DIP Switch SW2

See Figure 1-2 Item 24 for location of SW2. Default settings are shown in Figure A-1 and details are listed in Table A-1.

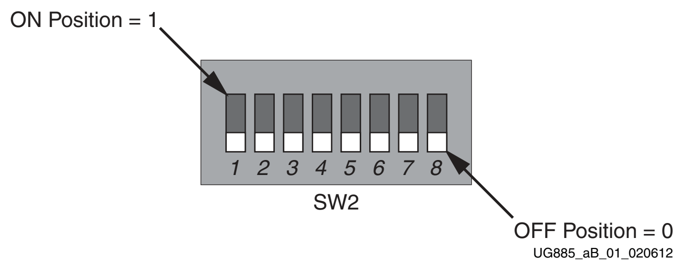

Figure A-1: **SW2 Default Settings**

Table A-1: **SW2 Default Switch Settings**

Position	Function	Default
1	GPIO_DIP_SW0	Off
2	GPIO_DIP_SW1	Off
3	GPIO_DIP_SW2	Off
4	GPIO_DIP_SW3	Off
5	GPIO_DIP_SW4	Off
6	GPIO_DIP_SW5	Off
7	GPIO_DIP_SW6	Off
8	GPIO_DIP_SW7	Off

Configuration DIP Switch SW11

See Figure 1-2 Item 29 for location of SW11. Default settings are shown in Figure A-2 and details are listed in Table A-2.

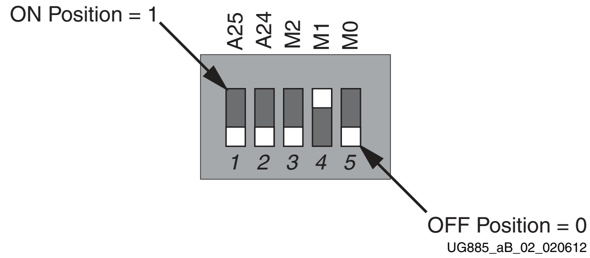

Figure A-2: **SW11 Default Settings**

The default mode setting M[2:0] = `010` selects Master BPI configuration at board power-on.

Table A-2: **SW11 Default Switch Settings**

Position	Function		Default
1	FLASH_A25	A25	Off
2	FLASH_A24	A24	Off
3	FPGA_M2	M0	Off
4	FPGA_M1	M1	On
5	FPGA_M0	M3	Off

Default Jumper Settings

See Figure A-3 for locations of jumpers listed in Table A-3.

Table A-3: **Default Jumper Settings**

Callout	Jumper	Function	Default Jumper Position	Schematic 0381418 Page Number
1	J6	SFP Enable	None	31
2	J9	XADC GND ferrite filter bypass jumper	None	40
3	J10	XADC GND-to-XADC_AGND jumper	1–2	40
4	J11	TI Controller U42 Addr 52 Reset jumper	None	46
5	J12	TI Controller U43 Addr 53 Reset jumper	None	50
6	J13	USB Mini-B Connector J2 VBUS	None	44
7	J14	USB SMBC U8 CLKOUT selector	None	44
8	J38	SFP RX Rate: 1-2 = Full BW Rate, 2-3 = Low BW Rate	1–2	31
9	J39	SFP TX Rate: 1-2 = Full BW Rate, 2-3 = Low BW Rate	1–2	31
10	J42	XADC external 1.2V or internal VREFP selector	1–2	40

Table A-3: **Default Jumper Settings *(Cont'd)***

Callout	Jumper	Function	Default Jumper Position	Schematic 0381418 Page Number
11	J43	XADC VCC Select Header	2–3	40
12	J44	USB Mini-B Connector J2 GND jumper	None	44
13	J45	USB SMBC U8 VBUS	1–2	44
14	J49	PCIe Bus Width Select Header	1-2	30
15	J50	TI Controller U64 Addr 54 Reset jumper	None	53
16	J51	FMC_VADJ_ON_B jumper	1–2	46
17	J53	XADC VCC5V0-to-XADC_VCC5V0 jumper	1–2	40
18	J54	XADC REF3012 U35 V_{IN} Select	1–2	40

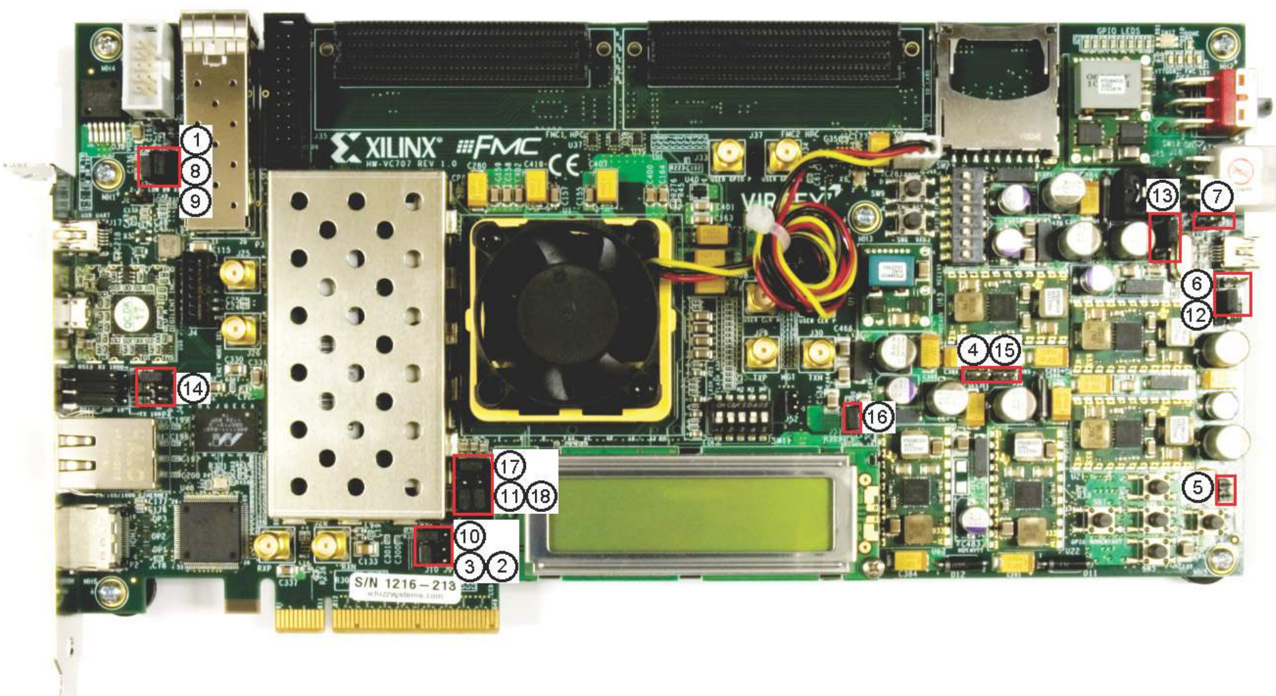

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Figure A-3: **VC707 Board Jumper Header Locations**

Appendix B

VITA 57.1 FMC Connector Pinouts

Figure B-1 shows the pinout of the FMC1 HPC connector J35 and the FMC2 HPC connector J37. For more information, see VITA 57.1 FMC1 HPC Connector (Partially Populated).

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

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Figure B-1: **FMC1 and FMC2 HPC Connector Pinout**

Xilinx Constraints File

The VC707 board Xilinx design constraints (XDC) file template provides for designs targeting the VC707 board. Net names in the constraints correlate with net names on the latest VC707 board schematic. Users must identify the appropriate pins and replace the net names listed here with net names in the user RTL. See *Vivado Design Suite User Guide Using Constraints* (UG903) [Ref 12]for more information.

The FMC connectors J35 and J37 are connected to 1.8V V_{cco} banks. Because each user's FMC card implements customer-specific circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

Refer to the Virtex-7 FPGA VC707 Evaluation Kit product page (www.xilinx.com/vc707), Docs & Designs tab, for the latest versions of the FPGA xdc constraint file.

Board Setup

Installing VC707 Board in a PC Chassis

Installation of the VC707 board inside a computer chassis is required when developing or testing PCI Express functionality.

When the VC707 board is used inside a computer chassis (that is, plugged in to the PCIe® slot), power is provided from the ATX power supply 4-pin peripheral connector through the ATX adapter cable shown in Figure D-1 to J18 on the VC707 board. The Xilinx part number for this cable is 2600304.

Figure D-1: **ATX Power Supply Adapter Cable**

To install the VC707 board in a PC chassis:

1. On the VC707 board, remove all six rubber feet and standoffs. The standoffs and feet are affixed to the board by screws on the top side of the board. Remove all six screws.
2. Power down the host computer and remove the power cord from the PC.
3. Open the PC chassis following the instructions provided with the PC.
4. Select a vacant PCIe expansion slot and remove the expansion cover (at the back of the chassis) by removing the screws on the top and bottom of the cover.
5. Plug the VC707 board into the PCIe connector at this slot.
6. Re-attach the two screws securing the card mounting bracket on the VC707 board.

   Note: The VC707 board is taller than standard PCIe cards. Ensure that the height of the card is free of obstructions.
7. Connect the ATX power supply to the VC707 board using the ATX power supply adapter cable as shown in Figure D-1:
   a. Plug the 6-pin 2 x 3 Molex connector on the adapter cable into J18 on the VC707 board.
   b. Plug the 4-pin 1 x 4 peripheral power connector from the ATX power supply into the 4-pin adapter cable connector.
8. Slide the VC707 board power switch SW12 to the ON position. The PC can now be powered on.

Board Specifications

Dimensions

Height: 5.5 inch (14.0 cm)

Thickness (±5%): 0.062 inch (0.1575 cm)

Length: 10.5 inch (26.7 cm)

Note: The VC707 board height exceeds the standard 4.376 inch (11.15 cm) height of a PCI Express card.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: –25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Appendix F

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

See the Virtex-7 FPGA VC707 Evaluation Kit Master Answer Record (AR 45382) for information on the CE requirements for the PC test environment.

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

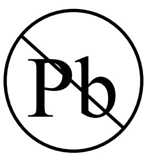
EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

In August of 2005, the European Union (EU) implemented the EU WEEE Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU requiring Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.



This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix G

Additional Resources

Xilinx Resources

- For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.
- For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the VC707 board and its documentation is available on these websites:

Virtex-7 FPGA VC707 Evaluation Kit

Virtex-7 FPGA VC707 Evaluation Kit documentation

Virtex-7 FPGA VC707 Evaluation Kit Answer Record (AR 45382)

These Xilinx documents provide supplemental material useful with this guide:

1. *7 Series FPGAs Overview* (DS180)
2. *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics* (DS183)
3. *7 Series FPGAs Configuration User Guide* (UG470)
4. *7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
5. *7 Series FPGAs Memory Resources User Guide* (UG473)
6. *LogiCORE IP AXI Universal Serial Bus 2.0 Device Product Guide for Vivado Design Suite* (PG137)
7. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
8. *7 Series FPGAs Integrated Block for PCI Express Product Guide for Vivado Design Suite* (PG054)
9. *LogiCORE IP Tri-Mode Ethernet MAC Product Guide for Vivado Design Suite* (PG051)
10. *7 Series FPGAs PCB Design Guide* (UG483)
11. *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide* (UG480)
12. *Vivado Design Suite User Guide Using Constraints* (UG903)
13. *LogiCORE IP Tri-Mode Ethernet MAC v4.5 User Guide* (UG138)
14. *7 Series FPGAs Packaging and Pinout Product Specifications User Guide* (UG475)

15. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
16. *AMS101 Evaluation Card User Guide (*UG886)

These external websites provide supplemental material useful with this guide:

17. Micron Technology, Inc.
(MT8JTF12864HZ-1G6G1, PC28F00AG18FE)
18. Standard Microsystems Corporation
(USB3320)
19. SiTime
(SiT9102)
20. Silicon Labs
(Si570, Si5324C)
21. Marvell Semiconductor and Marvell Semiconductor Alaska Gigabit Ethernet PHYS Transceivers
(88E1111)
22. Integrated Device Technology
(ICS844021I)
23. Analog Devices
(ADV7511KSTZ-P)
24. DisplayTech
(S162DBABC LCD)
25. Texas Instruments: Texas Instruments, Texas Instruments Fusion Tools Documentation, and Texas Instruments Digital Power & Interface Solutions
(UCD9248PFC, PTD08A010W, PTD08A020W, PTD08D021W, LMZ12002, TL1962ADC, TPS51200DR, PCA9548))
26. Analog Devices
(ADP123)
27. The Xilinx ATX cable part number 2600304 is manufactured by Sourcegate Technologies and is equivalent to the Sourcegate Technologies part number AZCBL-WH-11009. Sourcegate only manufactures the latest revision, which is currently A4. To order, contact Aries Ang, aries.ang@sourcegate.net, +65 6483 2878 for price and availability. This is a custom cable and cannot be ordered from the Sourcegate website.