LPC47N267

100 Pin LPC Super I/O with X-Bus Interface

PRODUCT FEATURES

Data Brief

- 3.3 Volt Operation (5V tolerant)
- Programmable Wakeup Event Interface (IO_PME# Pin)
- SMI Support (IO_SMI# Pin)
- GPIOs (29)
- Four IRQ Input Pins
- X-Bus Interface
  - Supports up to 4 external components
  - Supports I/O cycles (No Memory Support)
  - 8-Bit Data Transfer
  - 16-Bit Address Qualification
  - Write Protection for each component
- XNOR Chain
- PC99 and ACPI 1.0b Compliant
- 100-pin STQFP Package
- Intelligent Auto Power Management
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Supports One Floppy Drive Directly
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - Swap Drives A and B
  - Non-Burst Mode DMA Option
  - 48 Base I/O Address, 15 IRQ and 3 DMA Options
  - Forceable Write Protect and Disk Change Controls
- Floppy Disk Available on Parallel Port Pins (ACPI Compliant)
- Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Serial Ports
  - Two Full Function Serial Ports
  - High Speed NS16C550 Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
- Infrared Communications Controller
  - IrDA v1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - 2 IR Ports
  - 96 Base I/O Address, 15 IRQ Options and 3 DMA Options
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode IBM PC/XT, PC/AT, and PS/2 Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 192 Base I/O Address, 15 IRQ and 3 DMA Options
- LPC Bus Host Interface
  - Multiplexed Command, Address and Data Bus
  - 8-Bit I/O Transfers
  - 8-Bit DMA Transfers
  - 16-Bit Address Qualification
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PCI nCLKRUN Support
  - Power Management Event (IO_PME#) Interface Pin
- Mechanical Package
  - 100 pin STQFP (12mm x 12mm body size)

ORDER NUMBER(S): LPC47N267-MN FOR 100 PIN, STQFP PACKAGE

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General Description

The SMSC LPC47N267 is a 3.3V PC 99 and ACPI 1.0 compliant Super I/O Controller. The LPC47N267 implements an LPC interface, a pin reduced ISA interface, for supported I/O and DMA cycles. In addition, this part includes an X-Bus interface that may be accessed through the LPC interface for supported I/O cycles (memory cycles are not supported by this device). The X-Bus interface supports as many as four external components and it offers three different modes of operation for interfacing with these components. The X-Bus interface has an added “Write Protect” feature that ensures that the Base Address and disable bit for each component can only be set by the BIOS to prevent corruption by any virus software. This part also includes 29 GPIO pins.

The LPC47N267 incorporates SMSC’s true CMOS 765B floppy disk controller, advanced digital data separator, 16-byte data FIFO, two 16C550 compatible UARTs, one Multi-Mode parallel port with ChiProtect circuitry plus EPP and ECP support and one floppy direct drive support. The LPC47N267 does not require any external filter components, is easy to use and offers lower system cost and reduced board area. The LPC47N267 is software and register compatible with SMSC’s proprietary 82077AA core.

The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures and provides data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC’s patented data separator technology allowing for ease of testing and use. The LPC47N267 supports both 1Mbps and 2Mbps data rates and vertical recording operation at 1Mbps Data Rate.

The LPC47N267 also features a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI nCLKRUN support, relocatable configuration ports and three DMA channel options.

Both on-chip UARTs are compatible with the NS16C550. One UART includes additional support for a Serial Infrared Interface that complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats (used by Sharp and other PDAs), as well as Consumer IR.

The parallel port is compatible with IBM PC/AT architectures, as well as IEEE 1284 EPP and ECP. The parallel port ChiProtect circuitry prevents damage caused by an attached powered printer when the LPC47N267 is not powered.

The LPC47N267 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. The LPC47N267 also features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the FDC, parallel port, and UARTs.

The LPC47N267 supports the ISA Plug-and-Play Standard (Version 1.0a) and provides the recommended functionaity to support Windows ‘95/’98 and PC99. The I/O Address, DMA Channel and Hardware IRQ of each device in the LPC47N267 may be reprogrammed through the internal configuration registers. There are 192 I/O address location options, a Serialized IRQ interface, and three DMA channels.

Block Diagram

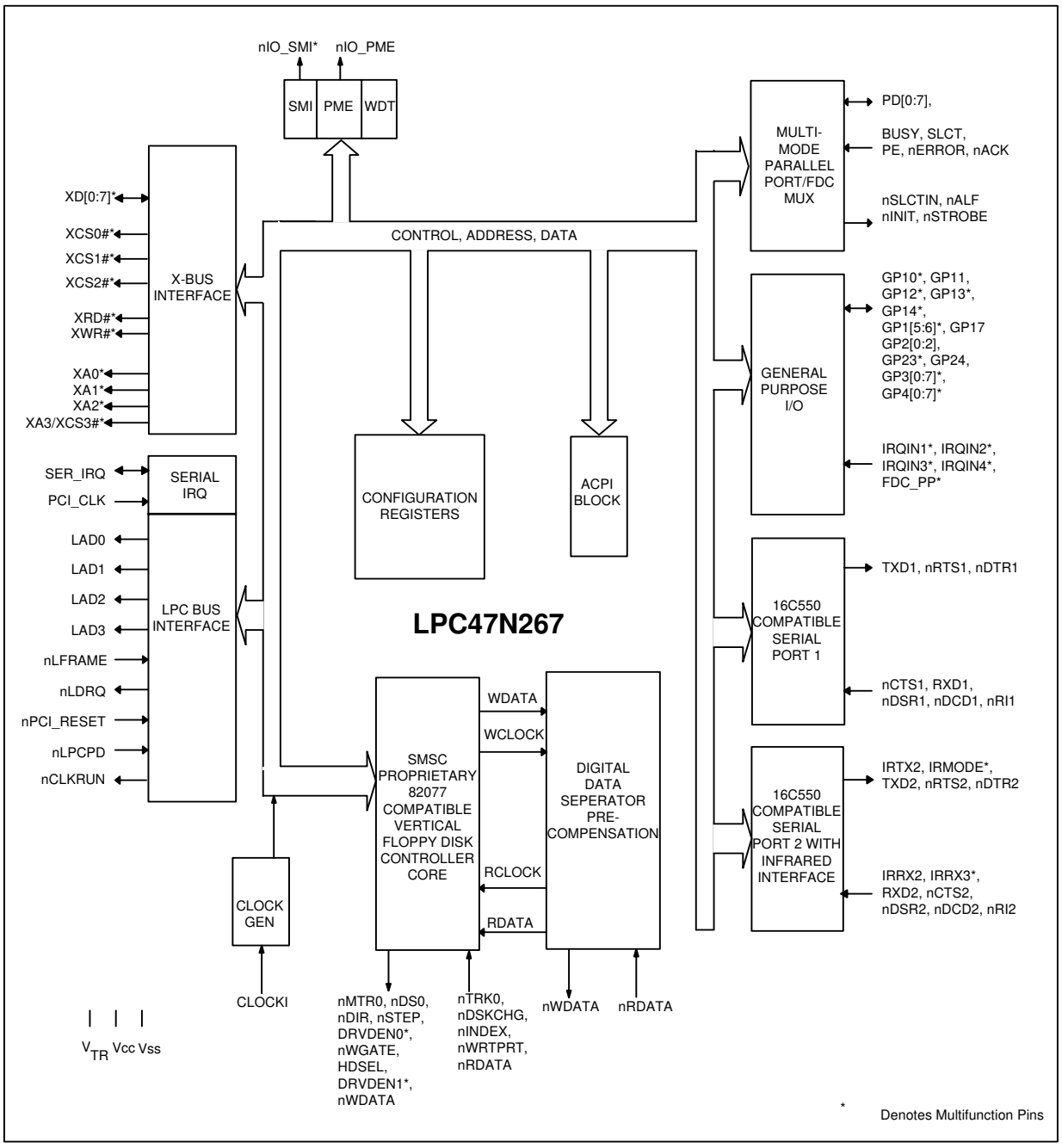

Figure 1 LPC47N267 Block Diagram

PRODUCT PREVIEW

Package Outline

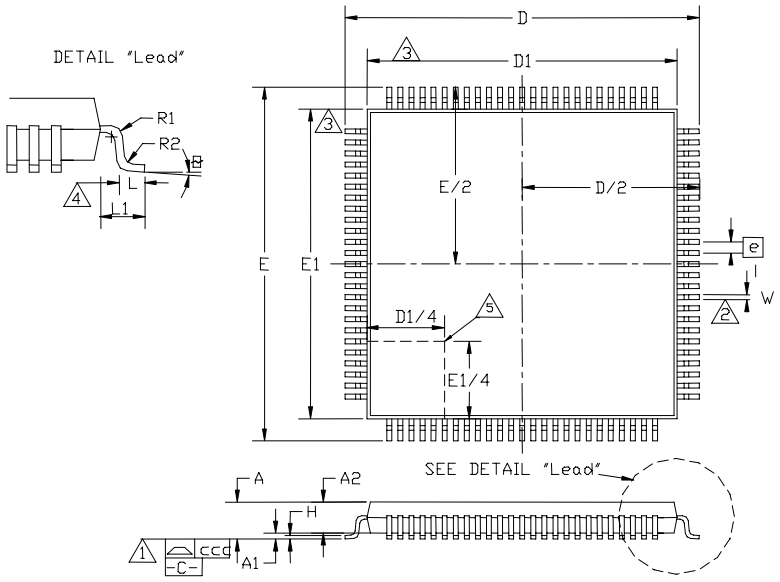

Figure 2 100 Pin STQFP, 12X12X1.4 Body, 2.0 MM Footprint

Table 1 100 Pin STQFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	13.80	14.00	14.20	X Span
D/2	6.90	7.00	7.10	1/2 X Span Measure from Centerline
D1	11.80	12.00	12.20	X body Size
E	13.80	14.00	14.20	Y Span
E/2	6.90	7.00	7.10	1/2 Y Span Measure from Centerline
E1	11.80	12.00	12.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e	0.40 Basic			Lead Pitch
q	0^o	3.5^o	7^o	Lead Foot Angle
W	0.13	0.16	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	.0762	Coplanarity *(Assemblers)*
ccc	~	~	0.08	Coplanarity *(Test House)*
ddd	~	~	0.035	True Position Spread (Bent Leads)

Notes:

[1] Controlling Unit: millimeter

[2] Minimum space between protrusion and an adjacent lead is .007 mm.

[3] Details of pin 1 identifier are optional but must be located within the zone indicated

[4]Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

[5]Shoulder widths must conform to JEDEC MS-026 dimension 'S' of a minimum of 0.20mm