Ordering number : ENA2131

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LC822973 — CMOS LSI TV Image Viewer LSI

Overview

This LSI is TV image viewer. A 16Mbit SDRAM is built-in as image frame buffers, on which an external CPU is able to draw the images, then another part of this LSI displays the SDRAM images on TV in NTSC/PAL after video data encoding. This LSI equips H/V scaling circuit to scale up QVGA size image to VGA to display on the TV screen, for instance.

The main features of this LSI are specified as below.

Features

- NTSC/PAL video encoder is integrated.
  - Various format support
    - ITU-R601 (13.5MHz/NTSC&PAL) SQ (12.27MHz/NTSC, 14.75MHz/PAL)
      - NTSC-J, M/PAL-B, D, G, H, I/PAL-M, N
  - Various image adjustment
    - Y signal: brightness and contrast adjustment
    - C signal:U gain, V gain, HUE and Burst amplitude adjustment
  - Trap filter
    - Trap filters locate on the Y signal pass to reduce cross color interference. The trap strength is adjustable by register setup.
  - Built-in color bar
    - This is for system test and level adjustment.
  - 10 bit DAC with 75Ω driver
    - A high accuracy video DAC of 10bit is built-in. Its DAC output is able to be connected to TV input or any image devices, thanks for its 75Ω driver built-in.
- It mounts 16Mbit SDRAM to store multiple VGA size images. Since it has the arbitration function built-in, the access timing from CPU for drawing can be used without any care of real-time access condition for TV display. VGA 30fps performance can be achieved with appropriate setting of system clock, the burst size of SDRAM, scaling ratio etc.

Continued to the next page.

* I^2C Bus is a trademark of Philips Corporation.

SANYO Semiconductor Co., Ltd.
http://www.sanyosemi.com/en/network/

Continued from the previous page.

- The OSD function is installed. OSD images consist of binary pixel data to display over the original image. The Alfa-blend display is also available.
- Scaling from ×1 up to ×4 in two independent directions, horizontally and vertically, is available. 256 step arbitrary enlargement is given by register settings. The image rotation is available when writing as well.
- The high-speed clock for SDRAM is generated internally by built-in PLL.
- CPU-IF with 8/9/16/18/24 bit width data transfer is available.
- Built-in VIDEO-IF supports receiving video rate image input with Hsync/Vsync/Dotclcok signals. It accepts various digital image formats of 18bit-RGB666, 16bit-RGB565, 16bit-YUV422, 8bit-YUV422, 8bit-YUV422 (BT656) and so on. In addition, it accepts both interlace and non-interlace format.
- The Autoview function executes automatic writing/reading sequence. Once all the relevant commands are set, then this function properly updates the image banks to write and to read. This bank arbitration avoids well the tearing image (reading outruns writing).
- The FilckerFreeFilter effectively decreases the line flicker, a substantial phenomena of the interlace method.
- High performance C-signal band-limit filter is built-in. The thorny ‘dot crawl’ is thus decreased.
- CGMS-A/WSS data multiple functions are built-in.
- The I/O voltage of the CPU/Video interface is 1.6V-3.4V.
- Macrovision™ Encoding (Revision 7.1.L1 in NTSC and PAL standards for Composite video output applications) are built-in. (LC822973-04VM-E only)*

* This device is Protected by U.S. patents 5, 583, 936; 6, 516, 132; 6, 836, 549; and 7, 050, 698; and other intellectual property rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision. Reverse engineering or disassembly is prohibited. This Device can only be sold or distributed to Authorized Buyers.

DC characteristics/AC characteristics

Absolute Maximum Ratings at DV_{SS} = 0V

Parameter		Symbol	Conditions	Ratings	unit
Supply voltage		DV_{DD}15 max		-0.3 to 1.8	V
		DV_{DD}IO max		-0.3 to 3.96	V
Input voltage		V_IIO		-0.3 to 3.96 *1	V
Output voltage		V_OIO		-0.3 to DV_{DD}IO+0.3	V
Operation surrounding temperature		Topg		-30 to 85	°C
Storage temperature		Tstg		-55 to 125	°C
Soldering temperature	Hand soldering		For 3 seconds	350	°C
	Reflow		For 10 seconds	255	°C
In/Out current		I_I15, I_O15		±20 *2	mA
		I_IIO, I_OIO			

*1 Input voltage of I/O basic cell in case of without P-ch protection diode.
*2 per 1 cell of I/O basic cell

Permissible Operation Range at Ta = -30 to 85°C, DV_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage	DV_{DD}15		1.35	1.5	1.65	V
	DV_{DD}IO *3		2.5	3.0	3.4	V
	DV_{DD}IO *4		1.6	1.8	2.0	V
	DV_{DD}3		2.7	3.0	3.4	V
	AV_{DD}3		2.7	3.0	3.4	V
	AV_{DD}15		1.35	1.5	1.65	V
Input range	V_{IN}IO		0		DV_{DD}IO	V

*3 at supply = 3.0V (Typical)
*4 at supply = 1.8V (Typical)

I/O pin capacity at $V_{DD}3 = DV_{DD}IO = V_I15 = V_IIO = DV_{SS} = 0V$, Ta = -30 to 85°C

Parameter	Symbol	Conditions	min	typ	max	unit
Input pin	C_{IN}	f = 1MHz			10	pF
Output pin	C_{OUT}				10	pF
I/O pin	$C_{I/O}$				10	pF

DC characteristics

I/O level / $V_{SS} = 0V$, $DV_{DD}IO$ = 2.5 to 3.4V, Ta = -30 to 85°C

Parameter		Symbol	Conditions	Applied pin *5	min	typ	max	unit
Input level	H	$V_{IH}IO$	CMOS	(1) (2)	2.0			V
	L	$V_{IL}IO$					$0.3DV_{DD}IO$	V
	H	$V_{IH}IO$	CMOS schmit	(3)	2.0			V
	L	$V_{IL}IO$					$0.3DV_{DD}IO$	V
Output level	H	$V_{OH}IO$	I_{OH} = -4mA	(2) (4)	$DV_{DD}IO$-0.4			V
	L	$V_{OL}IO$	I_{OL} = 4mA				0.4	V
	H			(5)				V
	L	$V_{OL}IO$	I_{OL} = 4mA				0.4	V
Input leak current		I_{IL}	$V_I = DV_{DD}3, DV_{SS}$	(1) (2) (3)	-10		+10	µA
Output leak current		I_{OZ}	High impedance	(4) (5)	-10		+10	µA

*5 The applied pins correspond to the following names.

I/O level / $V_{SS} = 0V$, $DV_{DD}IO$ = 1.6 to 2.0V, Ta = -30 to 85°C

Parameter		Symbol	Conditions	Applied pin *6	min	typ	max	unit
Input level	H	$V_{IH}IO$	CMOS	(1) (2)	$0.7DV_{DD}IO$			V
	L	$V_{IL}IO$					$0.25DV_{DD}IO$	V
	H	$V_{IH}IO$	CMOS schmit	(3)	$0.75DV_{DD}IO$			V
	L	$V_{IL}IO$					$0.2DV_{DD}IO$	V
Output level	H	$V_{OH}IO$	I_{OH} = -4mA	(2) (4)	$DV_{DD}IO$-0.4			V
	L	$V_{OL}IO$	I_{OL} = 4mA				0.4	V
	H			(5)				V
	L	$V_{OL}IO$	I_{OL} = 4mA				0.4	V
Input leak current		I_{IL}	$V_I = DV_{DD}3, DV_{SS}$	(1) (2) (3)	-10		+10	µA
Output leak current		I_{OZ}	High impedance	(4) (5)	-10		+10	µA

*6 The applied pins correspond to the following names.

(INPUT)

(1) ... CKI, A0, CS, CONF3-CONF0, MODE2-MODE0

(2) ... D15-D0, DB17, DB16

(3) ... XRST, CS, RD, WR, SCL, SDA

(OUTPUT)

(2) ... D15-D0

(4) ... INT, MON

(5) ... SDA (Open Drain)

DAC characteristics

The characteristics of DAC (10bitDAC) for video that features this LSI are illustrated.

Zero scale output voltage	within 0V±15mV
Full scale output voltage	within 1.00V±80mV
Maximum conversion speed	30MHz
Linear line error	within±4LSB (VQFN84 [-10B] : within±4.5LSB)
Differential linear line error	within±1LSB
Voltage reference level	1.20±20mV

(Ta = +25°C)

Current consumption

*at the time of $DV_{DD}3 = DV_{DD}IO$ = 3V and $DV_{DD}15$ = 1.5V and $AV_{DD}3$ = 3V and $AV_{DD}15$ = 1.5V and MCLK50MHz

* at the time of still picture (640×480) + OSD1 All screens + OSD2 All screens

Parameter	min	typ	max	unit
$AV_{DD}15$ (PLL operation current)		0.5	1	mA
$DV_{DD}15$ (core operation current)		10	15	mA
$AV_{DD}3$ (DAC operation current)*		35	35	mA
$DV_{DD}IO$ (IO operation current)		2	5	mA
$DV_{DD}3$ (SDRAM operation current)		8	13	mA
Standby current (clock input on)			300	µA
Standby current (input clock off)**			100	µA
Standby current (input clock off + SDRAM/SRAM off)**		6	18	µA

* ‘typ’ here implies only that DACOUT always outputs its maximum current.

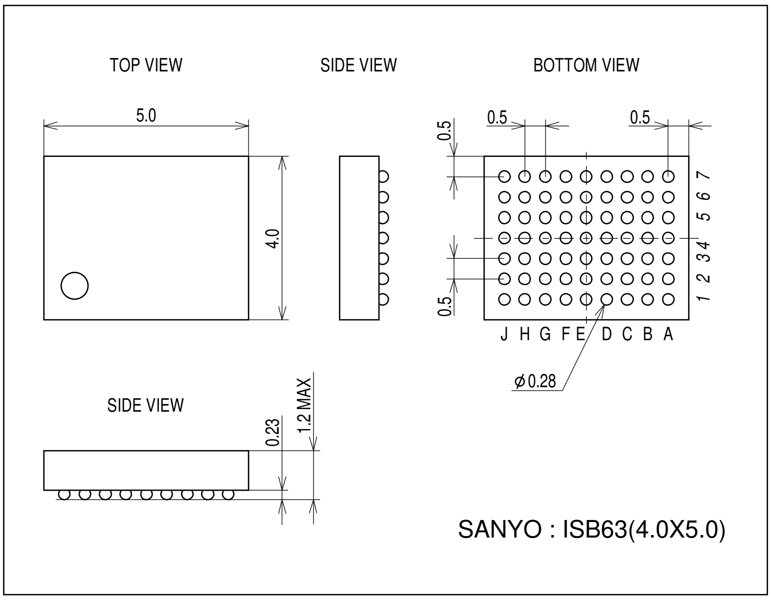
** Under the condition of tying input pin levels to H or L.

Standby current is at the condition of room temperature (+25°C)

Package Dimensions

unit : mm (typ)

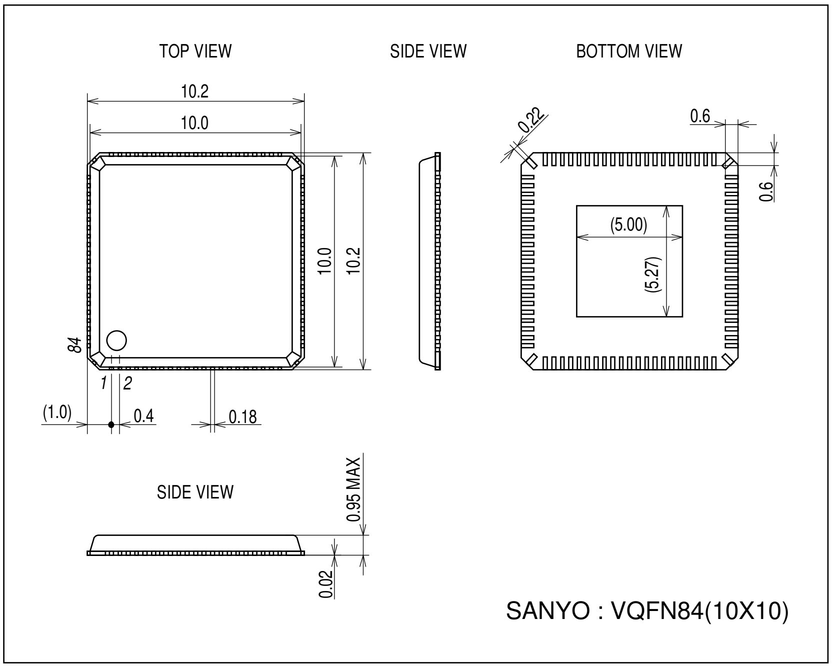
3442



Package Dimensions

unit : mm (typ)

3443

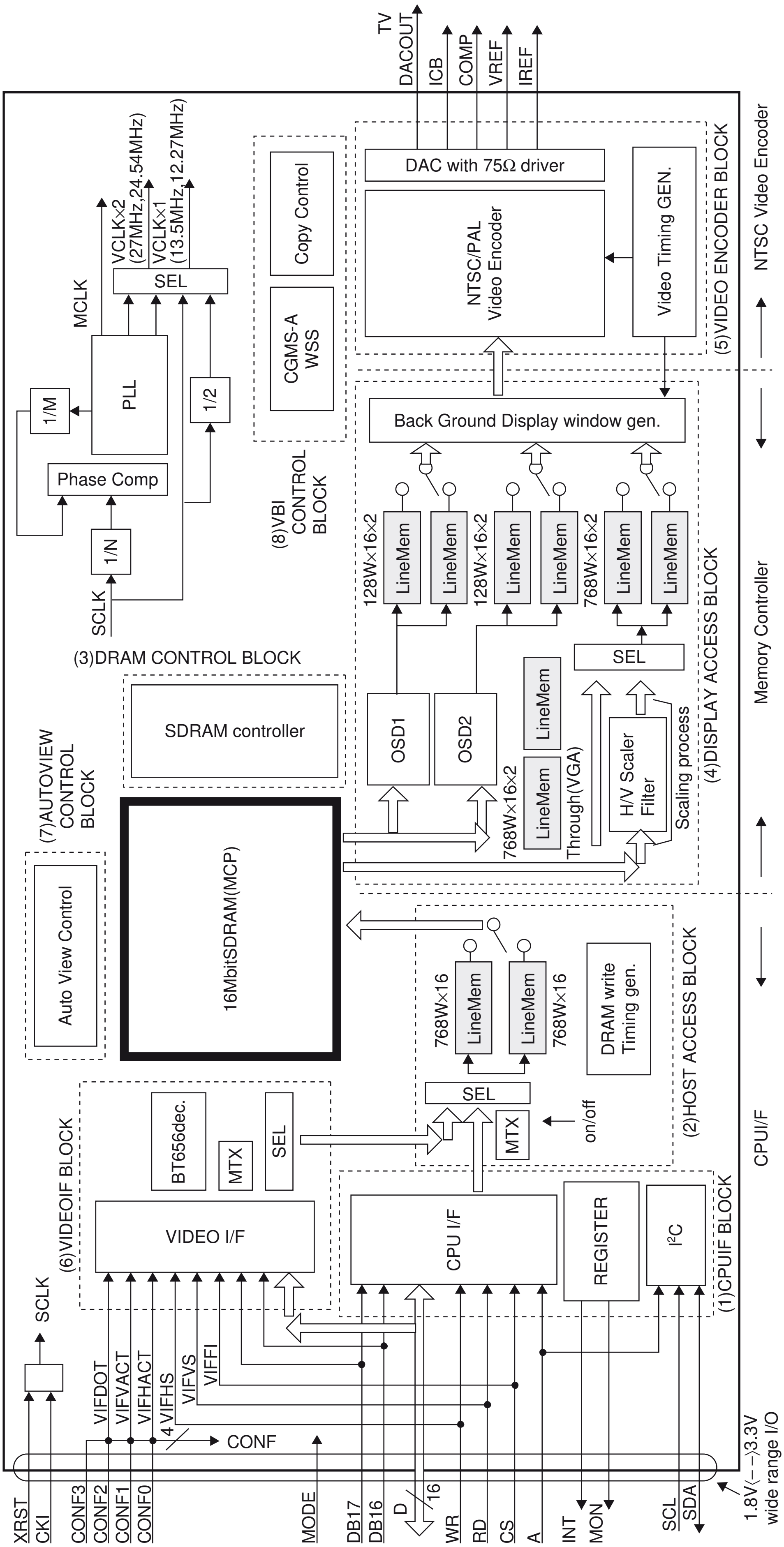


Structure

Outline Specification

Item	Outline
NTSC/PAL video encoder	Multi rate and multi format video encoder that supports NTSC/PAL and ITU-601/SQ (square pixel).
DAC	10bit-1chD/A converter that integrates 7Ω driver. Can be connected to TV directly without OP-amp or buffer.
CPU I/F	Support 8/9/16/18/24bit bus (D, WR, RD, CS, A0) of I80 type.
Video I/F	It corresponds to 5 format of RGB565, RGB666, YUV422 (8bit), YUV422 (8bit_BT656mode), and YUV422 (16bit). The writing operation is executed based on Sync signals.
Memory controller	Controls built-in (MCP) 16MbitSDRAM. Owns arbitration function and CPU access (drawing) is possible as needed.
Matrix (CPU I/F)	Performs RGB → YUV conversion at the time of CPU → memory writing.
Matrix (Video I/F)	Performs RGB → YUV conversion at the time of video port → memory writing.
PLL	Generates high-speed clock for SDRAM.
OSD	A reading binary image from SDRAM is displayed in TV. Because the Alfa blend function is installed, it is possible to select four stages by blend register.
Scaling function	×4 scaling processing at maximum is executed for reading image from SDRAM. Can be set to H and V direction independently.
Autoview function	The issue of the command of each screen is unnecessary. Writing/reading control in the image area (two bank or3 bank) set beforehand is executed automatically.
V-blanking period.	Can insert CGMS-A/WSS code into V-blanking period.
I/O	CMOS interface
Operation temperature	-30°C to 85°C
Package	ISB63 4mm × 5mm VQFN84 10mm × 10mm
Power voltage (IO)	$DV_{DD}IO$ (1.6V - 3.4V) for ex. : 1.8V (1.6V - 2.0V), 3.0V (2.5V - 3.4V)
Power voltage (digital core)	1.5V (1.35V - 1.65V)
Power voltage (PLL)	1.5V (1.35V - 1.65V)
Power voltage (for stacked SDRAM)	3.0V (2.7V - 3.4V)
Power voltage (DAC analog part)	3.0V (2.7V - 3.4V)

Structure Block



This LSI consists of 9 function blocks in the structure block above.

(1) CPU interface (CPUIF BLOCK)
The parameter setup such as mode setup/image area setup/video encoder characteristic of this LSI is possible via bus from CPU. The image data writing to SDRAM achieves image port writing command that is in the same command class as regular register and the same command class and keep writing continuously. This is a double bank buffer structure and is able to write drawing data for 1 line without WAIT control.

(2) Host access (HOST ACCESS BLOCK)
The image writing is fulfilled from CPU interface for SDRAM.
This obtains line buffer in double bank buffer and the writing is carried out to SDRAM as accessing from CPU. It also mounts 90, 180, 270 degrees rotation writing and writing function with matrix conversion processing besides regular writing.

(3) SDRAM control (DRAM CONTROL BLOCK)
This LSI is MCP (multi chip) structure and has 16Mbit SDRAM built-in. This is the memory controller that controls writing from CPU, reading for real-time display to video encoder and refresh processing for this memory.

(4) Reading control for display (DISPLAY ACCESS BLOCK)
This is the SDRAM reading processing part that controls transferring real-time image data to NTSC/PAL video encoder.
This consists of scaling part that performs enlargement processing for image data that was read from SDRAM and the buffer controlling part that provides video signal continuously to video encoder. The background processing circuit that inserts fixed level is mounted in the buffer control part besides display window (image from SDRAM).

(5) Video encoder (VIDEO ENCODER BLOCK)
This supports both NTSC/PAL methods. All timing signals that are necessary for video signal are generated in this block. This operates as a sync master and generates transfer request of real-time image data for DISPLAY ACCESS BLOCK.

(6) Video interface (VIDEOIF BLOCK)
It is an interface part for the video rate writing. It writes based on a video sync signal and the dot clock. In case of RGB format (RGB565, RGB666 etc.), the image is input to the host access part by processing the matrix at valid period. The BT656 decoding is done if necessary at the YUV format. it supports both non-interlace and interlace format. When the video interface is used, the data bus (D15 - D0) is treated as a dedicated image bus. The command issue and the register access are executed with the I^2C bus. It has the I^2C bus control part in CPU interface part.

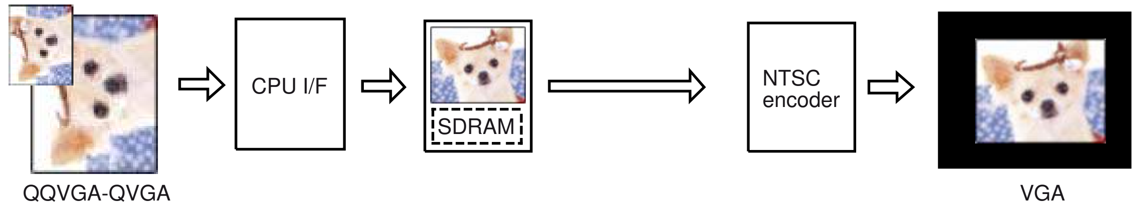
(7) Automatic image viewing (AUTOVIEW CONTROL BLOCK)
Automatic writing/reading sequence is executed by alternating the pre-defined image banks. Thus clean images without the scan passing (tearing image) are displayed. Consecutive image data transfer follows after one time command and parameter setting.

(8) VBI control (VBI CONTROL BLOCK)
The CGMS-A/WSS data is inserted. It has AUX function for the copy protect control etc.

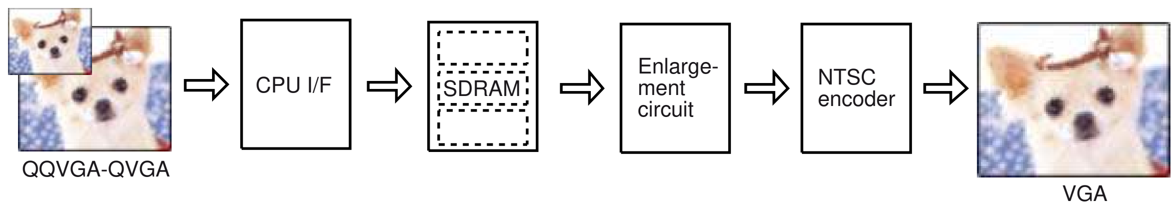
(9) Others
To combine drawing from CPU and real-time request (continuous video signal is provided to NTSC/PAL video encoder), SDRAM needs to be operated with high-speed clock. The high-speed master clock (MCLK) is created and supported by using PLL for input clock (CKI).

General Operation

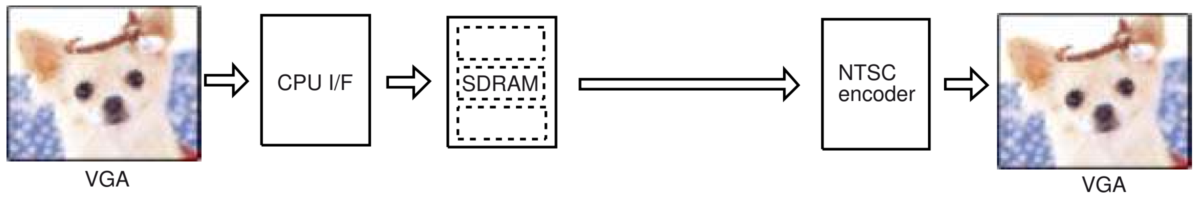
[Operation 1.]
The rotation processing is performed at the time of SDRAM writing. As a result, a vertically long image of small size such as QQVGA, QVGA, etc. is rotated 90 degrees and it is possible to display on TV (VGA size image).



[Operation 2.]
The enlargement processing can be realized by filter processing that utilized line memory for reading data from SDRAM. The small size image such as QQVGA and QVGA can be displayed on TV screen fully (VGA size). An enlargement ratio can be set optionally (2×(n+1)/256, n: 128 to 255). If the displayed image after enlargement is smaller than VGA size, other than target image can be set to background level (brightness/color setup possible).
This operation can be combined with the above rotation function.



[Operation 3.]
The enlargement processing can be bypassed if writing image size from CPU fits VGA image size exactly. Degradation of broad area level due to filter processing can be prevented.



[Moving image processing]
This LSI is the system that supports moving image that made writing from CPU and competitive operation of TV display (real-time reading from SDRAM) possible by using high-speed clock operation.
The moving image performance (supportable frame rate) improves by raising SDRAM clock frequency through PLL setup. However, the current consumption increases significantly.

Corresponding video format

The video format that NTSC/PAL video encoder corresponds is described in the following tables.

((NTSC))

Mode	ITU-601	SQ
Dot clock	13.500MHz	12.2727MHz
Dot/line	858	780
Horizontal valid period	720	640
Vertical cycle	525 lines/frames	
Vertical frequency	59.94Hz (field)	
Vertical blanking period	21 lines (line1-line21, line263-line284)	
Burst mask period	9 lines (line1-line9, line264-line272)	

((PAL))

Mode	ITU-601	SQ
Dot clock	13.500MHz	14.750MHz
Dot/ line	864	944
Horizontal valid period	720	768
Vertical cycle	625 lines/frames	
Vertical frequency	50Hz (field)	
Vertical blanking period	25 lines (line623-line22, line311-line335)	
Burst mask period	9 lines (line623-line6, line310-line318)	

*The video encoder is the component signal processing for Y and C of 8 bit each as an internal processing. The dot clock in the table above corresponds to the sampling clock at the time of 16bit processing of Y+C. To simplify post filter, the video encoder processing performs ×2 oversampling. Therefore, the operation clock in video encoder part is double of dot clock (27MHz, 24.54MHz, 29.5MHz, etc.).

Pin Description

	Pin name	Pol.	Dir	Description of function	at reset	Pin
	CKI	-	I	Master clock	-	1
	XRST	L	I	Master reset, Low active	-	1
	DB17	-	I	(bit17) extended bit. use at 18bit mode.	-	1
	DB16	-	I	(bit16) extended bit. use at 18bit mode	-	1
	D[15:0]/ VIFVD[15:0]	-	I/O	Data bus, needs pull-up resistance externally (unnecessary if either device always drives bus). This bus is sharing for the VIDEOIF.	-	16
	A0/ (IDSEL)	-	I	Address/ (IDSEL at VIDEOIF).	-	1
	RD/ (VIFVS)	L	I	Read pulse/ (Vsync in at VIDEOIF).	-	1
	WR/ (VIFHS)	L	I	Write pulse/ (Hsync in at VIDEOIF).	-	1
	CS/ (VIFFI)	L	I	Chip select/ (Field index in at VIDEOIF).	-	1
	INT	L	O	Interrupt	"0"	1
	MON	H	O	Monitor	"0"	1
	USEVIF	H	I	Set "H" in case of VIDEOIF mode. The command issue is via I^2C bus.	-	1
	SDA	-	I/O	SDA for I^2C bus.	-	1
	SCL	-	I	SCL for I^2C bus.	-	1
analog DAC	DACOUT	Ana	O	DAC output	-	1
analog DAC	IOB	Ana	O	DAC_IOB pin	-	1
analog DAC	COMP	Ana	O	DAC_COMP pin	-	1
analog DAC	VREF	Ana	O	DAC_VREF pin	-	1
	IREF	Ana	O	DAC_IREF pin	-	1
analog PLL	VCNT	Ana	I	VCNT pin	-	1
	MODE[2:0]	-	I	For test *	-	3
	CONF3	-	I	To decide input format	-	1
	CONF2 / (VIFDOT)	-	I	To decide input format / (Dotclock in at VIDEOIF)	-	1
	CONF1 / (VIFVACT)	-	I	To decide input format / (V-valid period flag in at VIDEOIF)	-	1
	CONF0 / (VIFHACT)	-	I	To decide input format / (H-valid period flag in at VIDEOIF)	-	1
	DV_{DD}15	Pow	-	DV_{DD} for digital core (1.5V part)	-	4 (6)
	DV_{DD}IO	Pow	-	DV_{DD} for digital I/O part	-	4 (7)
	DV_{DD}3	Pow	-	DV_{DD} for stacked SDRAM (it's controlled by internal switch cell)	-	3 (4)
	AV_{DD}3	Pow	-	AV_{DD} for DAC analog (analog 3V)	-	1
	AV_{DD}15	Pow	-	AV_{DD} for PLL analog (analog 1.5V)	-	1
	DV_{SS}	Pow	-	GND for digital part	-	6 (13)
	AV_{SS}	Pow	-	GND for analog part	-	2
	Total					63 (76)

* MODE pins are for testing.
They should be fixed to "L" normally.

Pin assignment (ISB63/VQFN84/[SQFP100])

Ball [ISB]	Pin [VQFN]	Reference [SQFP]	Pin name	I/O	Application	
-	-	1	NC	-		
-	-	2	NC	-		
H5	1	3	DV_{SS}	P	Digital GND	
G6	2	4	SDA	B	I^{2}C data / maintain open at CPUIF mode	
H7	3	5	SCL	I	I^{2}C clock / connect to GND at CPUIF mode.	
F4	4	6	$DV_{DD}15$	P	V_{DD} (digital core)	
F6	5	7	CONF3	I	For format setting at CPUIF (bit3). connect to GND at VIDEOIF mode.	
G7	6	8	CONF2/ (VIFDOT)	I	For format setting at CPUIF (bit2). / Dotclock in at VIDEOIF mode.	
F5	7	9	CONF1/ (VIFVACT)	I	For format setting at CPUIF (bit1). / V-valid flag in at VIDEOIF mode.	
F7	8	10	CONF0/ (VIFHACT)	I	For format setting at CPUIF (bit0). / H-valid flag in at VIDEOIF mode.	
E2	9	11	$DV_{DD}3$	P	V_{DD} (for stacked SDRAM)	
H5	10	12	DV_{SS}	P	Digital GND	
E7	11	13	CKI	I	System clock input	
E6	12	14	$DV_{DD}IO$	P	V_{DD} (Digital IO)	
E4	13	15	XRST	I	System reset ("L"==reset)	
D7	14	16	INT	O	INT signal ("L"==interrupt generation)	
E5	15	17	MON	O	Monitor pin.	
H5	16	18	DV_{SS}	P	Digital GND	
C7	17	19	A0/ (IDSEL)	I	Address/ID address select at VIDEOIF mode. (0 : 8'b0100_000_r, 1 : 8'b0100_001_r).	
D6	18	20	CS/ (VIFFI)	I	/CS signal/field index at VIDEOIF mode.	
B7	19	21	$DV_{DD}15$	P	V_{DD} (digital core)	
H5	20	22	DV_{SS}	P	Digital GND	
-	-	23	NC	-		
-	-	|	|	-		
-	-	27	NC	-		
C6	21	28	DB17	I	bit17 for 18bit data transfer format.	
A7	22	29	DB16	I	bit16 for 17bit data transfer format.	
E6	23	30	$DV_{DD}IO$	P	V_{DD} (Digital IO)	
B6	24	31	D15/ (VIFVD15)	B	CPU data bus/Video data bus. (MSB)	
A6	25	32	D14/ (VIFVD14)	B	|	
C5	26	33	D13/ (VIFVD13)	B	|	
B5	27	34	D12/ (VIFVD12)	B	|	
A5	28	35	D11/ (VIFVD11)	B	|	
D5	29	36	D10/ (VIFVD10)	B	|	
D4	30	37	D9/ (VIFVD9)	B	|	
A4	31	38	D8/ (VIFVD8)	B	|	
B4	32	39	D7/ (VIFVD7)	B	|	
C4	33	40	WR/ (VIFHS)	I	/WR pulse/Hsync at VIDEOIF mode.	
A3	34	41	RD/ (VIFVS)	I	/RD pulse/Vsync at VIDEOIF mode.	
E3	35	42	$DV_{DD}15$	P	V_{DD} (digital core)	
B3	36	43	DV_{SS}	P	Digital GND	
A2	37	44	$DV_{DD}IO$	P	V_{DD} (Digital IO)	
C3	38	45	D6/ (VIFVD6)	B	CPU data bus/Video data bus.	
D3	39	46	D5/ (VIFVD5)	B	|	
B2	40	47	D4/ (VIFVD4)	B	|	
A1	41	48	D3/ (VIFVD3)	B	|	
C2	42	49	D2/ (VIFVD2)	B	CPU data bus/Video data bus.	

* The product version are ISB63 and VQFN84. SQFP100 is a package for our evaluation (reliability test).

Continued to the next page.

Continued from the previous page.

Ball [ISB]	Pin [VQFN]	Reference [SQFP]	Pin name	I/O	Application	
-	-	50	NC	-		
-	-	|	|	-		
-	43	54	NC	-		
-	44	55	NC	-		
D2	45	56	DV_{SS}	P	Digital GND	
B1	46	57	D1/ (VIFVD1)	B	CPU data bus/Video data bus.	
C1	47	58	D0/ (VIFVD0)	B	CPU data bus/Video data bus. (LSB)	
E3	48	59	DV_{DD}15	P	V_{DD} (digital core)	
F1	49	60	DV_{DD}IO	P	V_{DD} (Digital IO)	
D1	50	61	DV_{SS}	P	Digital GND	
E1	51	62	DV_{DD}3	P	V_{DD} (for stacked SDRAM)	
D1	52	63	DV_{SS}	P	Digital GND	
D1	53	64	DV_{SS}	P	Digital GND	
F1	54	65	DV_{DD}IO	P	V_{DD} (Digital IO)	
F2	55	66	DV_{SS}	P	Digital GND	
G1	56	67	DV_{DD}3	P	V_{DD} (for stacked SDRAM)	
G2	57	68	DV_{SS}	P	Digital GND	
H1	58	69	DV_{DD}15	P	V_{DD} (digital core)	
G1	59	70	DV_{DD}3	P	V_{DD} (for stacked SDRAM)	
F2	60	71	DV_{SS}	P	Digital GND	
-	-	72	NC	-		
-	-	|	|	-		
-	61	76	NC	-		
-	62	77	NC	-		
-	63	78	NC	-		
-	64	79	NC	-		
J1	65	80	AV_{DD}3	P	AV_{DD} (DAC analog : 3V part)	
	66		AV_{DD}3	P	AV_{DD} (DAC analog : 3V part)	
H2	67	81	AV_{SS}1	P	GND (analog for DAC)	
G3	68	82	VREF	Ana	DAC_VREF pin	
J2	69	83	COMP	Ana	DAC_COMP pin	
H3	70	84	IREF	Ana	DAC_IREF pin	
F3	71	85	IOB	Ana	DAC_IOB pin	
J3	72	86	DACOUT	Ana	DAC_ video output	
F1	73	87	DV_{DD}IO	P	V_{DD} (Digital IO)	
J4	74	88	MODE2	I	mode setting (bit2), should be fixed "L"	
H4	75	89	MODE1	I	mode setting (bit1), should be fixed "L"	
G4	76	90	MODE0	I	mode setting (bit0), should be fixed "L"	
J5	77	91	USEVIF	I	To use VIDEOIF mode ("H":select VIDEOIF)	
F4	78	92	DV_{DD}15	P	V_{DD} (digital core)	
H5	79	93	DV_{SS}	P	Digital GND	
J6	80	94	AV_{DD}15	P	AV_{DD} (PLL analog : 1.5V part)	
G5	81	95	AV_{SS}2	P	GND(PLL analog)	
H6	82	96	VCNT	Ana	VCNT pin for PLL	
J7	83	97	DV_{DD}IO	P	V_{DD} (Digital IO)	
-	84	98	NC	-		
-	-	99	NC	-		
-	-	100	NC	-		

* The product version are ISB63 and VQFN84. SQFP100 is a package for our evaluation (reliability test).

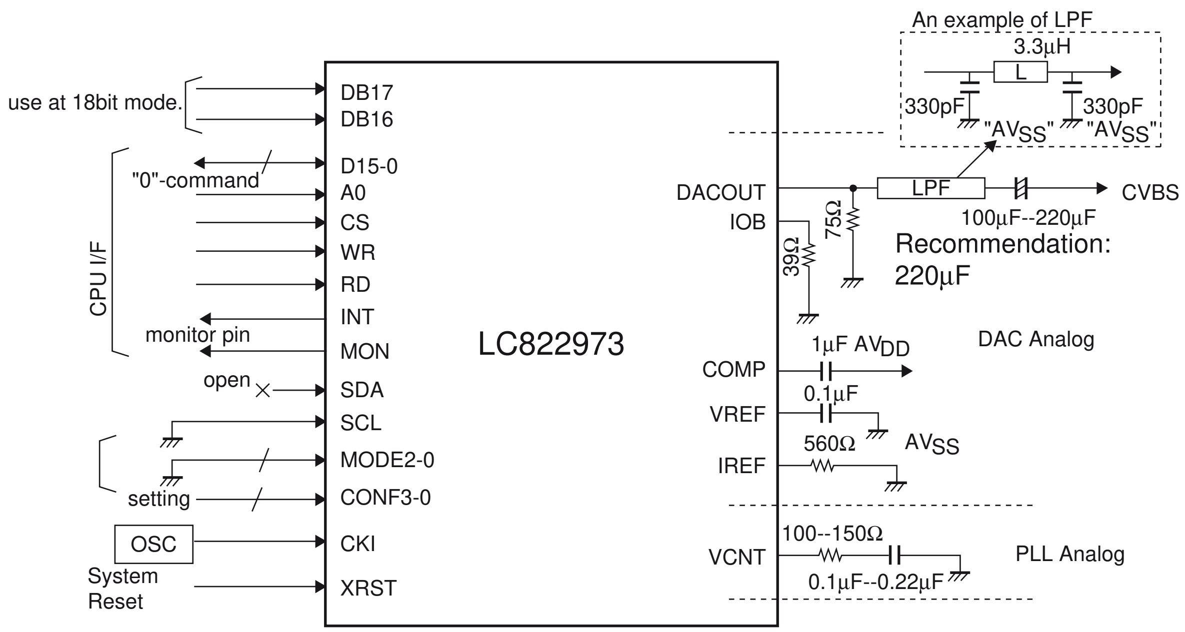
Pin Layout (ISB63)

A1 marking

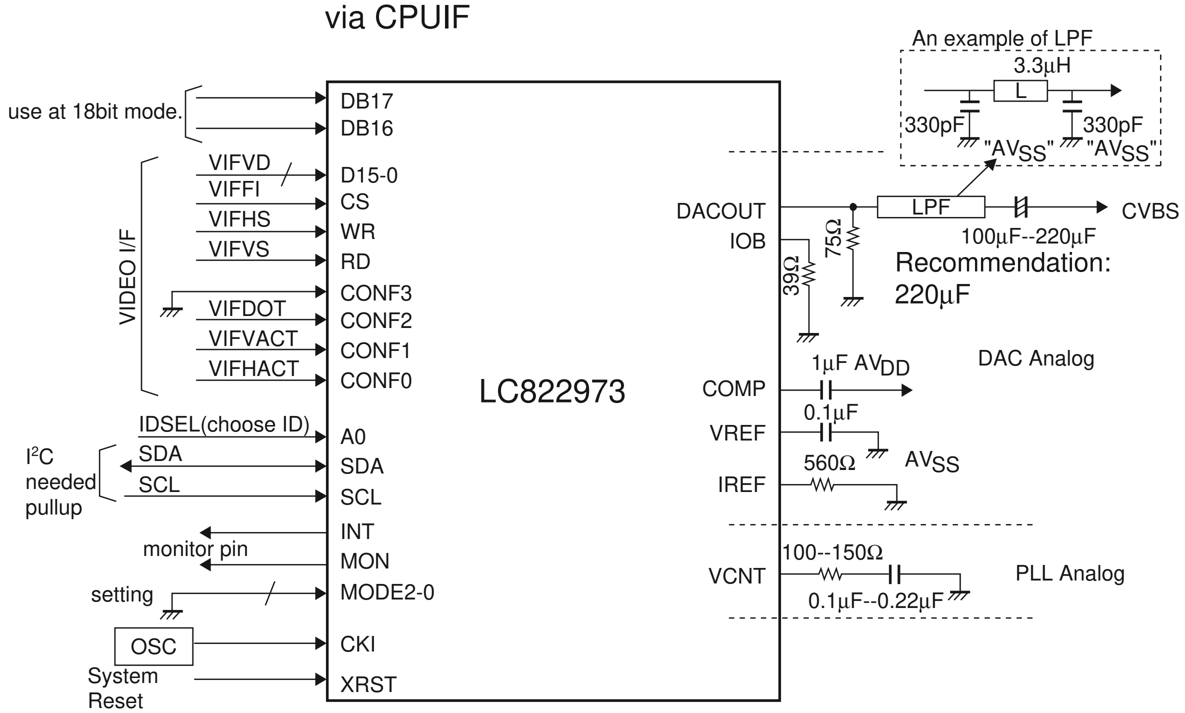
	1	2	3	4	5	6	7
A	D3	DV_{DDIO}	RD	D8	D11	D14	DB16
B	D1	D4	DV_{SS}	D7	D12	D15	DV_{DD15}
C	D0	D2	D6	WR	D13	DB17	A0
D	DV_{SS}	DV_{SS}	D5	D9	D10	CS	INT
E	DV_{DD3}	DV_{DD3}	DV_{DD15}	XRST	MON	DV_{DDIO}	CKI
F	DV_{DDIO}	DV_{SS}	IOB	DV_{DD15}	CONF1	CONF3	CONF0
G	DV_{DD3}	DV_{SS}	VREF	MODE0	AV_{SS2}	SDA	CONF2
H	DV_{DD15}	AV_{SS1}	IREF	MODE1	DV_{SS}	VCNT	SCL
J	AV_{DD3}	COMP	DACOUT	MODE2	USEVIF	AV_{DD15}	DV_{DDIO}

Top View

Peripheral Circuit Example



via CPUIF



via VIDEOIF

* The MODE2:0 pins are for test use, so please tie them "L".
* Please do not leave input pins OPEN.

* Above figure shows in case of 27MHz (24.54MHz) clock input.
  When the dot clock is generated with PLL (.e.g.: CKI==26MHz), it is necessary to change in PLL loop filter's constant. Please refer to " 7.12. Consideration of 26.0MHz clock input" paragraph for details.

Writing image format (via CPU I/F)

The hardware adopts 24/18/16/9/8bit RGB format and YUV422 format of 24/18/16/9/8 as a CPU writing via CPU-I/F. Input format is determined by CONF[3:0] pins.

The RGB → YUV matrix processing operates automatically when RGB input is formatted.

CONF[3:0]		0	1		2	3		4		5		6		7		8	
Data		RGB565	YUV422		RGB666									RGB565			
Transfer Format		16bit (×1)	16bit (×1)		18bit (×1)	18bit (×2)		18bit (×2)		18bit (×2)		18bit (×2)		16bit (×2)		16bit (×2)	
trans num		1	1	2	1	1	2	1	1	2	2	1	2	1	2	1	2
DB17	17	-	-	-	R5	-	-	-	-	-	-	-	-	-	-	-	-
DB16	16	-	-	-	R4	-	-	-	-	-	-	-	-	-	-	-	-
D[15]	15	R5	Ya7	Yb7	R3	R5	B1	R5	R3	R5	G2	-	-	R5	G2	-	-
D[14]	14	R4	Ya6	Yb6	R2	R4	B0	R4	R2	R4	G1	-	-	R4	G1	-	-
D[13]	13	R3	Ya5	Yb5	R1	R3	-	-	R1	R3	G0	-	-	R3	G0	-	-
D[12]	12	R2	Ya4	Yb4	R0	R2	-	-	R0	R2	B5	-	-	R2	B5	-	-
D[11]	11	R1	Ya3	Yb3	G5	R1	-	-	G5	R1	B4	-	-	R1	B4	-	-
D[10]	10	G5	Ya2	Yb2	G4	R0	-	-	G4	R0	B3	-	-	G5	B3	-	-
D[9]	9	G4	Ya1	Yb1	G3	G5	-	-	G3	G5	B2	-	-	G4	B2	-	-
D[8]	8	G3	Ya0	Yb0	G2	G4	-	-	G2	G4	B1	R5	G2	G3	B1	-	-
D[7]	7	G2	U7	V7	G1	G3	-	-	G1	G3	B0	R4	G1	-	-	R5	G2
D[6]	6	G1	U6	V6	G0	G2	-	-	G0	-	-	R3	G0	-	-	R4	G1
D[5]	5	G0	U5	V5	B5	G1	-	-	B5	-	-	R2	B5	-	-	R3	G0
D[4]	4	B5	U4	V4	B4	G0	-	-	B4	-	-	R1	B4	-	-	R2	B5
D[3]	3	B4	U3	V3	B3	B5	-	-	B3	-	-	R0	B3	-	-	R1	B4
D[2]	2	B3	U2	V2	B2	B4	-	-	B2	-	-	G5	B2	-	-	G5	B3
D[1]	1	B2	U1	V1	B1	B3	-	-	B1	-	-	G4	B1	-	-	G4	B2
D[0]	0	B1	U0	V0	B0	B2	-	-	B0	-	-	G3	B0	-	-	G3	B1

For CONF==2:RGB666_18bit mode, R5 and R4 correspond DB17 and DB16 pins, respectively.
Otherwise, please connect DB17, 16 pins to GND.

CONF[3:0]		9		10		11			12			13			14			15		
Data		RGB888				RGB666						RGB888								
Transfer Format		24bit (×2)		24bit (×2)		18bit (×3)			18bit (×3)			24bit (×3)			24bit (×3)			24bit (×3)		
trans num		1	2	1	2	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3
DB17	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DB16	16	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D[15]	15	R7	B7	R7	G7	R5	G5	B5	-	-	-	Ra7	Ba7	Gb7	Ra7	Ga7	Ba7	-	-	-
D[14]	14	R6	B6	R6	G6	R4	G4	B4	-	-	-	Ra6	Ba6	Gb6	Ra6	Ga6	Ba6	-	-	-
D[13]	13	R5	B5	R5	G5	R3	G3	B3	-	-	-	Ra5	Ba5	Gb5	Ra5	Ga5	Ba5	-	-	-
D[12]	12	R4	B4	R4	G4	R2	G2	B2	-	-	-	Ra4	Ba4	Gb4	Ra4	Ga4	Ba4	-	-	-
D[11]	11	R3	B3	R3	G3	R1	G1	B1	-	-	-	Ra3	Ba3	Gb3	Ra3	Ga3	Ba3	-	-	-
D[10]	10	R2	B2	R2	G2	R0	G0	B0	-	-	-	Ra2	Ba2	Gb2	Ra2	Ga2	Ba2	-	-	-
D[9]	9	R1	B1	R1	G1	-	-	-	-	-	-	Ra1	Ba1	Gb1	Ra1	Ga1	Ba1	-	-	-
D[8]	8	R0	B0	R0	G0	-	-	-	-	-	-	Ra0	Ba0	Gb0	Ra0	Ga0	Ba0	-	-	-
D[7]	7	G7	-	-	B7	-	-	-	-	-	-	Ga7	Rb7	Bb7	Rb7	Gb7	Bb7	R7	G7	B7
D[6]	6	G6	-	-	B6	-	-	-	-	-	-	Ga6	Rb6	Bb6	Rb6	Gb6	Bb6	R6	G6	B6
D[5]	5	G5	-	-	B5	-	-	-	R5	G5	B5	Ga5	Rb5	Bb5	Rb5	Gb5	Bb5	R5	G5	B5
D[4]	4	G4	-	-	B4	-	-	-	R4	G4	B4	Ga4	Rb4	Bb4	Rb4	Gb4	Bb4	R4	G4	B4
D[3]	3	G3	-	-	B3	-	-	-	R3	G3	B3	Ga3	Rb3	Bb3	Rb3	Gb3	Bb3	R3	G3	B3
D[2]	2	G2	-	-	B2	-	-	-	R2	G2	B2	Ga2	Rb2	Bb2	R2	Gb2	Bb2	R2	G2	B2
D[1]	1	G1	-	-	B1	-	-	-	R1	G1	B1	Ga1	Rb1	Bb1	Rb1	Gb1	Bb1	R1	G1	B1
D[0]	0	G0	-	-	B0	-	-	-	R0	G0	B0	Ga0	Rb0	Bb0	Rb0	Gb0	Bb0	R0	G0	B0

* 16bit or 8bit command area is to be sent within heavy-lined area. CONF==5, 6, 7, 8, 11, 12, and 15 correspond 8bit command data, and the 16bit parameter register needs double transfer.

* Hatched area shows unused pins. "L" level is always output, so please keep them open.

* For CONF==14:24bit (×3) format, a dummy write of 0×0 data is required every time after sending all the frame data.

* For CONF==1:16bit-YUV422 format, RGB to YUV matrix conversion can be enabled by register setting, SYSCTL1 (bit5) MTXON, which is useful for the mixed format system of RGB565 and YUV422.

Writing image format (via VIDEO I/F)

Writing from video IF corresponds to various entry formats such as YUV422 (8bit), YUV422 (8bitBT656decode), YUV422 (16bit), RGB565 (16bit), and RGB666 (18bit).
When video IF is used, the USEVIF pin is set to "H". The VIFFMT register is set and a necessary input format is decided at the same time. In this LSI, internal processing is YUV system.
The RGB → YUV matrix processing operates automatically when RGB is input.

USEVIF		1										
VIFFMT[3:0]		0		1		2		3		4	5	6
Data Format		YUV422				RGB565				YUV422	RGB565	RGB666
BT656decode		No		Yes		No						
Transfer Format		16bit (×2)		16bit (×2)		16bit (×2)		16bit (×2)		16bit (×1)	16bit (×1)	18bit (×1)
Trans num		1	2	1	2	1	2	1	2	1	1	1
DB17	17	-	-	-	-	-	-	-	-	-	-	R5
DB16	16	-	-	-	-	-	-	-	-	-	-	R4
D15/VIFVD15	15	-	-	-	-	-	-	-	-	Y7	R5	R3
D14/VIFVD14	14	-	-	-	-	-	-	-	-	Y6	R4	R2
D13/VIFVD13	13	-	-	-	-	-	-	-	-	Y5	R3	R1
D12/VIFVD12	12	-	-	-	-	-	-	-	-	Y4	R2	R0
D11/VIFVD11	11	-	-	-	-	-	-	-	-	Y3	R1	G5
D10/VIFVD10	10	-	-	-	-	-	-	-	-	Y2	G5	G4
D9/VIFVD9	9	-	-	-	-	-	-	-	-	Y1	G4	G3
D8/VIFVD8	8	-	-	-	-	-	-	-	-	Y0	G3	G2
D7/VIFVD7	7	U7/V7	Y7	U7/V7	Y7	R5	G2	G2	R5	U7/V7	G2	G1
D6/VIFVD6	6	U6/V6	Y6	U6/V6	Y6	R4	G1	G1	R4	U6/V6	G1	G0
D5/VIFVD5	5	U5/V5	Y5	U5/V5	Y5	R3	G0	G0	R3	U5/V5	G0	B5
D4/VIFVD4	4	U4/V4	Y4	U4/V4	Y4	R2	B5	B5	R2	U4/V4	B5	B4
D3/VIFVD3	3	U3/V3	Y3	U3/V3	Y3	R1	B4	B4	R1	U3/V3	B4	B3
D2/VIFVD2	2	U2/V2	Y2	U2/V2	Y2	G5	B3	B3	G5	U2/V2	B3	B2
D1/VIFVD1	1	U1/V1	Y1	U1/V1	Y1	G4	B2	B2	G4	U1/V1	B2	B1
D0/VIFVD0	0	U0/V0	Y0	U0/V0	Y0	G3	B1	B1	G3	U0/V0	B1	B0

USEVIF		1									
VIFFMT[3:0]		7		8		9			10		
Data Format		RGB666							RGB888		
BT656decode		No									
Transfer Format		18bit (×2)		18bit (×2)		18bit (×3)			24bit (×3)		
Trans num		1	2	1	2	1	2	3	1	2	3
DB17	17	-	-	-	-	-	-	-	-	-	-
DB16	16	-	-	-	-	-	-	-	-	-	-
D15/VIFVD15	15	R5	B1	R5	R3	-	-	-	-	-	-
D14/VIFVD14	14	R4	B0	R4	R2	-	-	-	-	-	-
D13/VIFVD13	13	R3	-	-	R1	-	-	-	-	-	-
D12/VIFVD12	12	R2	-	-	R0	-	-	-	-	-	-
D11/VIFVD11	11	R1	-	-	G5	-	-	-	-	-	-
D10/VIFVD10	10	R0	-	-	G4	-	-	-	-	-	-
D9/VIFVD9	9	G5	-	-	G3	-	-	-	-	-	-
D8/VIFVD8	8	G4	-	-	G2	-	-	-	-	-	-
D7/VIFVD7	7	G3	-	-	G1	-	-	-	R7	G7	B7
D6/VIFVD6	6	G2	-	-	G0	-	-	-	R6	G6	B6
D5/VIFVD5	5	G1	-	-	B5	R5	G5	B5	R5	G5	B5
D4/VIFVD4	4	G0	-	-	B4	R4	G4	B4	R4	G4	B4
D3/VIFVD3	3	B5	-	-	B3	R3	G3	B3	R3	G3	B3
D2/VIFVD2	2	B4	-	-	B2	R2	G2	B2	R2	G2	B2
D1/VIFVD1	1	B3	-	-	B1	R1	G1	B1	R1	G1	B1
D0/VIFVD0	0	B2	-	-	B0	R0	G0	B0	R0	G0	B0

* The width of the bus at video IF is decided by the register setting. (USEVIF=="H").
All the image ports are set to the input at video IF. Please connect an unused bit with GND (It shows "-" in the table).

Command

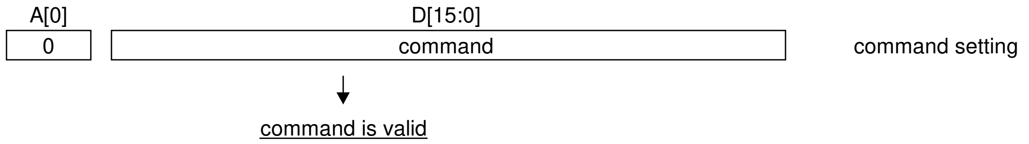
Command Type/Register Map

There are two types of command. One is to be able to operate by a command itself and the other needs a parameter.
In case of writing a command, A0 should be set to 0 and A0 should be set to 1 in case of writing or reading a parameter.
If other command is executed before setting a parameter, the command that is in the middle of setting is cancelled.

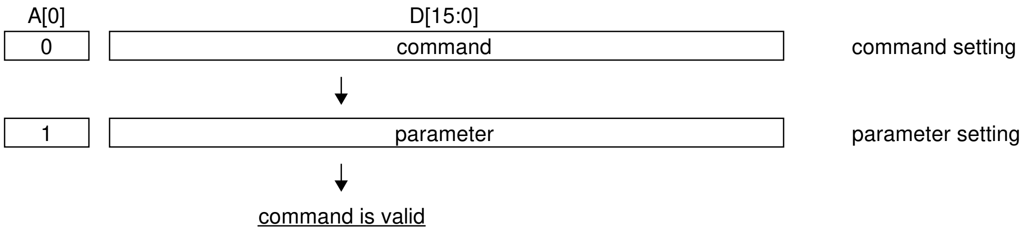
Other than 9bit interface

How to set command

〈Command that doesn't need a parameter〉



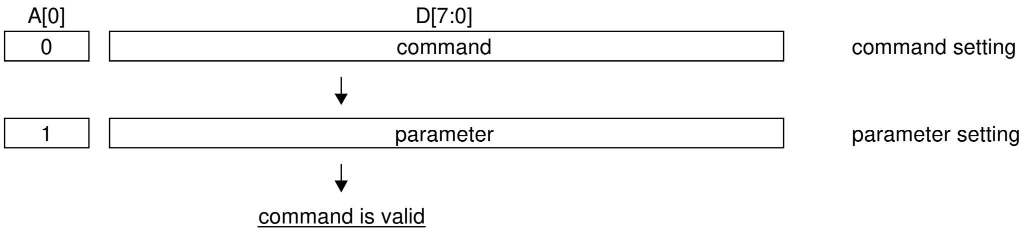
〈Command that needs a parameter〉



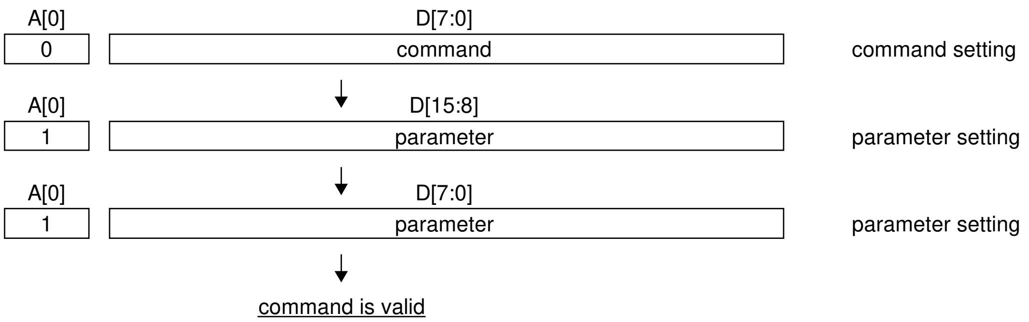
8bit/9bit interface

How to set command

〈Command that doesn't need a parameter〉



〈Command that needs a parameter〉



* 9bit transfer CONF="5", 8bit transfer CONF="7"/CONF="11" : data bus[15:8] should be used.
* 9bit transfer CONF="6", 8bit transfer CONF="8"/CONF="12"/CONF="15" : data bus[7:0] should be used.

I²C access

When video I/F is used (USEVIF==1), the register access from the host uses the I²C bus.
One sending data size of the I²C bus is 8bit.
Additionally, I²C is not applicable the concept of the address (A0==0: the command and A0==1: parameter) used with parallel CPUIF.
Therefore, a special access way is necessary as follows respectively.

Stand-alone command : not need parameter--IMGWRITE,IMGREADGO etc.)

write "00" into the target address

[target address]+["00"]

(normal write : need 1word parameter)

write sequentially "upper byte" → "lower byte" into target address.

address is "upper : normal address×2" , "lower : normal address×2+1" in case of I²C.

[target address(upper)]+["writing data for upper byte"]
[target address(lower)]+["writing data for lower byte"]

*Please keep the order "upper byte → lower byte".

When the host accessing is finished, internal transfer with word align will start.

(normal read : need 1word parameter)

read sequentially "upper byte" → "lower byte" from target address.

address is "upper : normal address×2" , "lower : normal address×2+1" in case of I²C.

[target address(upper)]+["reading data for upper byte"]
[target address(lower)]+["reading data for lower byte"]

The read order from upper byte or lower byte doesn't especially have regulations.
Only one byte accessing is also possible.

(image writing command : AUTOVIEWON,IMGWRITE,OSDWRITE etc.)

write via special image port (IMGPORT : 0×FD).

After issuing the image writing command, the data writing is necessary in accurate the order. (upper → lower → upper → lower...)

On the other hand, the data writing operation from the host is unnecessary because the automatic writing is done with a pin (image data/dot clock) at video IF.

[target address]+["00"] ← Issue AUTOVIEWON command etc.
[IMGPORT address]+["data writing for upper byte : at 1st pixel"]
[IMGPORT address]+["data writing for lower byte : at 1st pixel"]
[IMGPORT address]+["data writing for upper byte : at 2nd pixel"]
|||||
[IMGPORT address]+["data writing for upper byte : at Nth pixel"]
[IMGPORT address]+["data writing for lower byte : at Nth pixel"]

(image reading command : IMGREAD)

read via special image port (IMGPORT : 0×FD).

The access order is same as parallel CPU IF : IMGREADGO → IMGREAD → image reading.

[IMGREADGO]+["00"] ← Issue IMGREADGO command.
[IMGREAD]+["00"] ← Issue IMGREAD command.
[IMGPORT address]+["reading target pixel's upper byte"]
[IMGPORT address]+["reading target pixel's lower byte"]

Please keep the order "upper byte → lower byte".

Because the I²C bus is low-speed, status read after IMGREADGO command is unnecessary.

(status read :)

Status and a usual register are distinguished referring to the A0 address at parallel IF.

On the other hand, it corresponds in a special address in I²C.

(STAT upper : STATUP : 0×FE, STAT lower : STATDN : 0×FF).

[STATUP address]+["reading upper byte of STATUS register"]
[STATDN address]+["reading upper byte of STATUS register"]

The read order from upper byte or lower byte doesn't especially have regulations.
Only one byte accessing is also possible.

List of Command (A0==0)

The following tables are memory maps for 16bitCPU bus with 16bit width parameters.
I^2C takes Big ENDIAN system.
upper byte : I^2C_address = Add × 2
lower byte : I^2C_address = Add × 2 + 1

No	Add	Command name	Function	length	Description
1	0×01	CLKCONT	Clock control	1word	VCLK_MODE, PLLON, DACON, DRAM sleep, Mode setting at VIDEOIF
2	0×02	DIV_M	PLL control	1word	1/M (12bit)
3	0×03	DIV_N	PLL control	1word	1/N (12bit)
4	0×04	DIV_P	PLL control	1word	1/P (8bit), S0--S3
5	0×05	reserved	-	-	-
6	0×06	INT	Interrupt	1word	INT factor *) this can be issued during memory writing
7	0×07	INTEN	Interrupt	1word	INT factor clear *) this can be issued during memory writing
8	0×08	SYSCTL1	System setup	1word	Scaler and Matrix ON/OFF, scan direction, display OFF, filter setup, enhancer setup, etc.
9	0×09	SYSCTL2	System setup	1word	Transfer mode setup, V sync setup, etc.
10	0×0a	SYSCTL3	System setup	1word	Polarity, system control, etc. (others, spare)
11	0×0b	MEMSET1	MEMCTL setup	1word	SDRAM burst length, latency, mode, etc.
12	0×0c	MEMSET2	MEMCTL setup	1word	SDRAM refresh interval
13	0×0d	MEMSET3	MEMCTL setup	1word	SDRAM initial sequence setup
14	0×0e	IMGWRITE	CPU drawing	-	CPU → SDRAM Writing
15	0×0f	IMGREADGO	Image reading	-	SDRAM → CPU Reading start
16	0×10	IMGREAD	Image reading	1word	SDRAM → CPU Reading (acquiring data)
17	0×11	IMGABORT	Drawing end	-	CPU drawing forced termination
18	0×12	SCALE	Scale up	1word	Scaling image ratio setup
19	0×13	reserved	-	-	-
20	0×14	reserved	-	-	-
21	0×15	WFBHLEN	Coordinate setup	1word	SDRAM address length for CPU drawing (H)
22	0×16	WFBVLEN	Coordinate setup	1word	SDRAM address length for CPU drawing (V)
23	0×17	WFBHSTART	Coordinate setup	1word	horizontal start point for SDRAM writing
24	0×18	WFBVSTART	Coordinate setup	1word	vertical start point for SDRAM writing
25	0×19	RFBHOFST	Coordinate setup	1word	Real-time reading SDRAM address offset (H)
26	0×1a	RFBVOFST	Coordinate setup	1word	Real-time reading SDRAM address offset (V)
27	0×1b	DSPHOFST	Coordinate setup	1word	Real-time reading display position offset (H)
28	0×1c	DSPVOFST	Coordinate setup	1word	Real-time reading display position offset (V)
29	0×1d	DSPHLEN	Coordinate setup	1word	Real-time reading display position length (H)
30	0×1e	DSPVLEN	Coordinate setup	1word	Real-time reading display position length (V)
31	0×1f	BGCOLOR1	Background color	1word	Background color Y signal (use only low 8bit)
32	0×20	BGCOLOR2	Background color	1word	Background color UV signal (U: upper, V: lower)
33	0×21	ENCMODE	VENC setup	1word	Operation mode, filter switch, interlace setup
34	0×22	ENCGAIN1	VENC setup	1word	Level setup, bright, contrast
35	0×23	ENCGAIN2	VENC setup	1word	Level setup, color gain
36	0×24	ENCBST1	VENC setup	1word	Burst gain setup
37	0×25	ENCBST2	VENC setup	1word	Burst phase setup
38	0×26	ENCBBPLT	VENC setup	1word	Blueback pallet setup
39	0×27	ENCRHVAL	Video timing	1word	Horizontal valid period signal to the memory controller adjustment
40	0×28	ENCHBLK	Video timing	1word	Horizontal Blanking period adjustment
41	0×29	ENCVBLK	Video timing	1word	Vertical Blanking period adjustment
42	0×2a	VERSION	Other	1word	Version register
43	0×2b	TESTMODE	For test	1word	-
44	0×2c	OSDCONT_1	OSD1 setup	1word	SDRAM burst length,OSD1 ON/OFF, etc.

Continued to the next page.

Continued from the previous page.

No	Add	Command name	Function	length	Description
45	0×2d	OSDWFBHSTART	OSD1, 2 setup	1word	SDRAM address offset for OSD drawing (H)
46	0×2e	OSDWFBVSTART	OSD1, 2 setup	1word	SDRAM address offset for OSD drawing (V)
47	0×2f	OSDWFBHLEN	OSD1, 2 setup	1word	SDRAM address length for OSD drawing (H)
48	0×30	OSDWFBVLEN	OSD1, 2 setup	1word	SDRAM address length for OSD drawing (V)
49	0×31	OSDRFBHOFST_1	OSD1 setup	1word	SDRAM reading address (H) offset for OSD1
50	0×32	OSDRFBVOFST_1	OSD1 setup	1word	SDRAM reading address (V) offset for OSD1
51	0×33	OSDHOFST_1	OSD1 setup	1word	display position offset (H) for OSD1
52	0×34	OSDVOFST_1	OSD1 setup	1word	display position offset (V) for OSD1
53	0×35	OSDHLEN_1	OSD1 setup	1word	display position length (H) for OSD1
54	0×36	OSDVLEN_1	OSD1 setup	1word	display position length (V) for OSD1
55	0×37	OSDCONT_2	OSD2 setup	1word	burst length (SDRAM), OSD2 ON/OFF, etc.
56	0×38	OSDRFBHOFST_2	OSD2 setup	1word	SDRAM reading address offset (H) for OSD2
57	0×39	OSDRFBVOFST_2	OSD2 setup	1word	SDRAM reading address offset (V) for OSD2
58	0×3a	OSDHOFST_2	OSD2 setup	1word	display position offset (H) for OSD2
59	0×3b	OSDVOFST_2	OSD2 setup	1word	display position offset (V) for OSD2
60	0×3c	OSDHLEN_2	OSD2 setup	1word	display position length (H) for OSD2
61	0×3d	OSDVLEN_1	OSD2 setup	1word	display position length (V) for OSD2
62	0×3e	OSDCOLOR_Y	OSD1,2 setup	1word	OSD Y adjustment (Up: OSD1/Down: OSD2)
63	0×3f	OSDCOLOR_U	OSD1,2 setup	1word	OSD U adjustment (Up: OSD1/Down: OSD2)
64	0×40	OSDCOLOR_V	OSD1,2 setup	1word	OSD V adjustment (Up: OSD1/Down: OSD2)
65	0×41	OSDWRITE	OSD drawing	-	CPUOSD → SDRAM DRAW
66	0×42	OSDABORT	OSD drawing	-	CPUOSD → DRAW ABORT
67	0×43	VIFSYS	VIDEOIF setup	1word	Data ordering, sync polarity, internal valid flag on/off etc.
68	0×44	VIFHACTSTA	VIDEOIF setup	1word	Internal valid flag (start position of H-flag)
69	0×45	VIFHACTEND	VIDEOIF setup	1word	Internal valid flag (end position of H-flag)
70	0×46	VIFVACTSTA	VIDEOIF setup	1word	Internal valid flag (start position of V-flag)
71	0×47	VIFVACTEND	VIDEOIF setup	1word	Internal valid flag (end position of V-flag)
72	0×48	AVIEWSYS	A-VIEW setup	1word	Num of bank at AUTOVIEW mode
73	0×49	AUTOVIEWON	A-VIEW start	-	Strat AUTOVIEWing
74	0×4a	AUTOVIEWOFF	A-VIEW stop	-	Stop AUTOVIEWing
75	0×4b	AVWFBHSTART_0	A-VIEW setup	1word	Start position of bank#0 (H)
76	0×4c	AVWFBVSTART_0	A-VIEW setup	1word	Start position of bank#0 (V)
77	0×4d	AVWFBHSTART_1	A-VIEW setup	1word	Start position of bank#1 (H)
78	0×4e	AVWFBVSTART_1	A-VIEW setup	1word	Start position of bank#1 (V)
79	0×4f	AVWFBHSTART_2	A-VIEW setup	1word	Start position of bank#2 (H)
80	0×50	AVWFBVSTART_2	A-VIEW setup	1word	Start position of bank#2 (V)
81	0×51	CGMSA_CODE	CGMSA setup	1word	CGMSA code setting
82	0×52	CGMSA_TRM	CGMSA setup	1word	CGMSA position setting
83	0×53	WSS_CODE	WSS setup	1word	WSS code setting
84	0×54	WSS_TRM	WSS setup	1word	WSS position setting
85	0×55				reserved
|	|				|
112	0×70				reserved

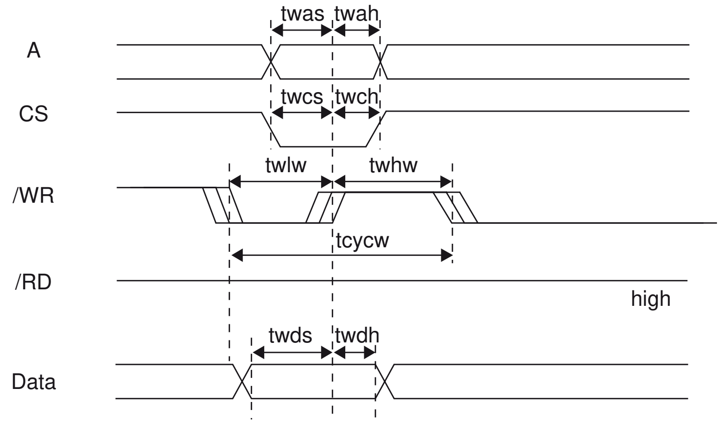
for I^2C

113	0×7E	0×FC (I^2C) : no use 0×FD (I^2C) : IMGPORT	Image port	
114	0×7F	0×FE (I^2C) : status (upper) 0×FF (I^2C) : status (lower)	Status	

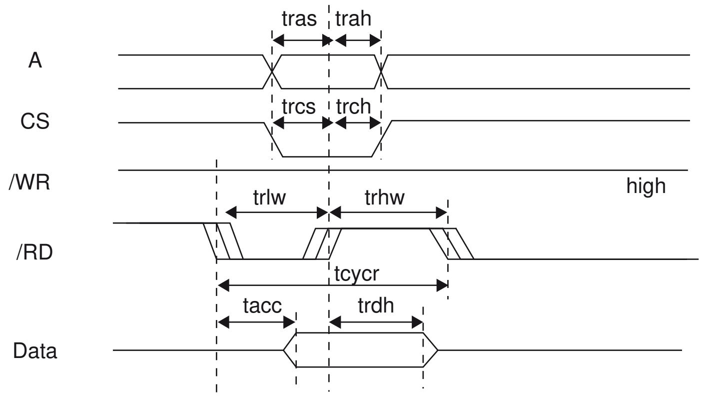
AC characteristics (CPU bus timing)

Parallel I/F (I80 like)

CPU WRITE



CPU READ



Item	Symbol	Condition	min	typ	max	unit
System cycle time (write) [×1 transfer]	tcycw	write	3T*			cyc
System cycle time (read) [×1 transfer]	tcycr	read	3T*			cyc
System cycle time (write) [×2, ×3 transfer]	tcycw	write	2T*			cyc
System cycle time (read) [×2, ×3 transfer]	tcycr	read	2T*			cyc
Address setup time (write)	twas	A	15			ns
Address hold time (write)	twah	A	5			ns
Address setup time (read)	tras	A	25			ns
Address hold time (read)	trah	A	5			ns
CS setup time (write)	twcs	/CS	15			ns
CS hold time (write)	twch	/CS	5			ns
CS setup time (read)	trcs	/CS	25			ns
CS hold time (read)	trch	/CS	5			ns
/WR low side pulse width	twlw	/WR	20			ns
/WR high side pulse width	twhw	/WR	15			ns
/RD low side pulse width	trlw	/RD	25			ns
/RD high side pulse width	trhw	/RD	15			ns
Data setup time	twds	Data [15:0]	15			ns
Data hold time	twdh	Data [15:0]	5			ns
Read access time	tacc*	Data [15:0]			20	ns
Data hold time	Trdh	Data [15:0]			10	ns

* T ⇒ MCLK (master clock) 1 cycle .ex. MCLK: 50MHz ⇒ 1T is 20ns.
*tacc ⇒ from (/RD) or (/CS)↓

I^2C transfer sequence and AC characteristics

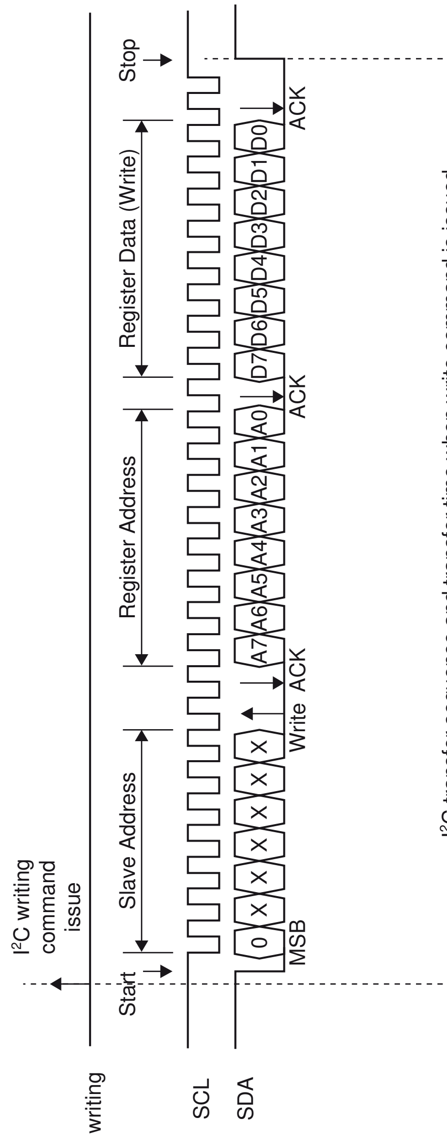
I^2C slave circuit is equipped to the LSI for the Video-I/F mode, which enables to read and to write command registers via SDA and SCL pins.

IDSEL pin sets one of two pre-defined device ID's,

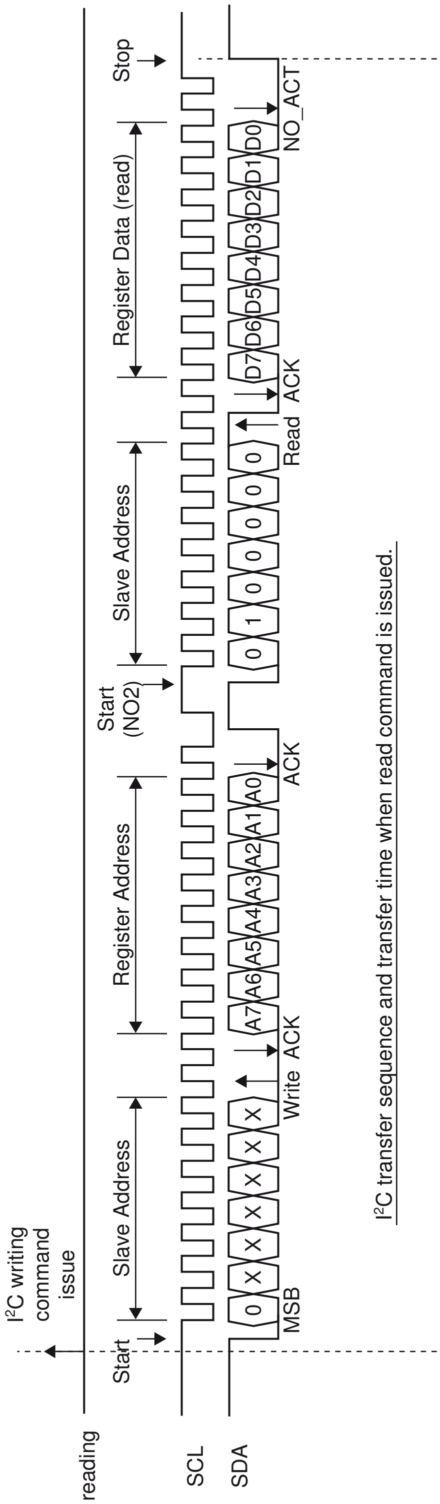
IDSEL: 0 then device ID=0×40 (0100_000_r)

IDSEL: 1 then device ID=0×42 (0100_001_r)

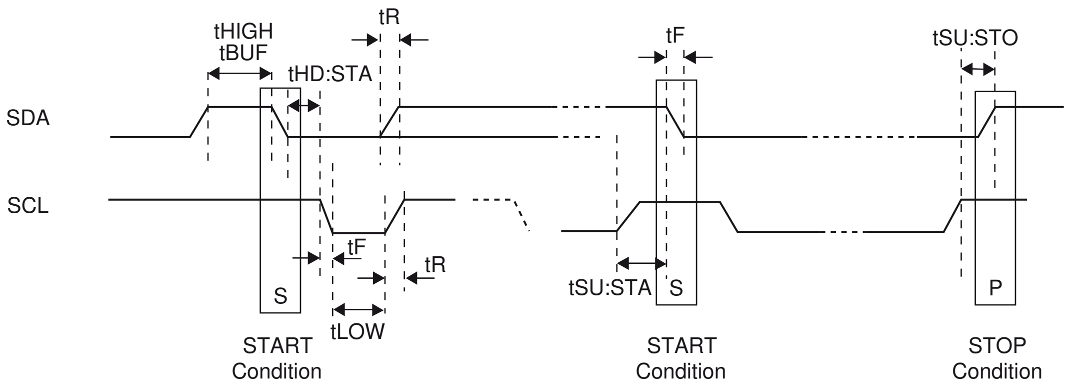
The transfer sequence of I^2C is explained below.



I^2C transfer sequence and transfer time when write command is issued.

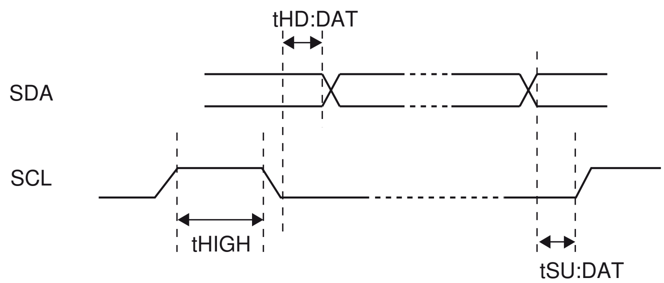


I^2C transfer sequence and transfer time when read command is issued.



I/O timing of I²C bus (at the time of SCL 400kHz cycle mode)

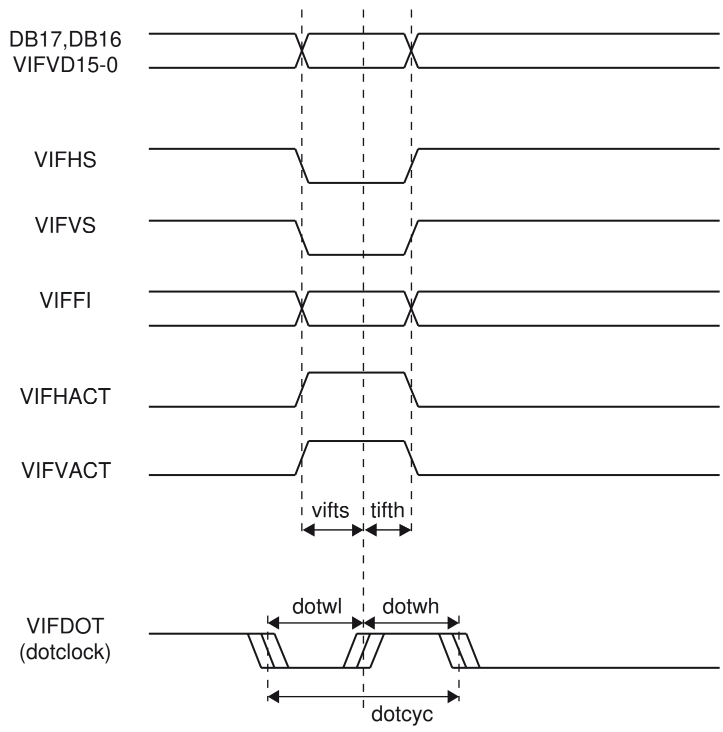
Symbol	Item	min	max	Unit
tBUF	Bus open period	1.3		µs
tHD: STA	Hold time (Start)	0.6		µs
tLOW	SCL_Lo period	1.3		µs
tHIGH	SCL_Hi period	1.3		µs
tR	Data rising		300	µs
tF	Data falling		300	µs
tSU: STA	Setup time (Start)	0.6		µs
tSU: STO	Setup time (Stop)	0.6		µs



I/O timing of I²C bus (at the time of high speed operation)

Symbol	Item	min	max	Unit
tSU: DAT	Setup time (Data)	100		ns
tHD: DAT	Hold time (Data)	0		ns
tHIGH	SCL_Hi period	150		ns

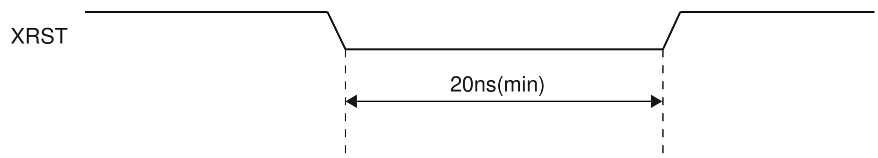
AC characteristics (VIDEO I/F timing)



SymbolItem	Symbol	Condition	min	typ	max	unit
Data/Flag Setup time	vifts	DB17/16 VIFVD, VIFHS, VIFVS, VIFFI VIFHACT VIFVACT	10			ns
Data/Flag Hold time	vifth	DB17/16 VIFVD, VIFHS, VIFVS, VIFFI VIFHACT VIFVACT	5			ns
Clock low side pulse width	dotwl	VIFDOT	15			ns
Clock high side pulse width	dotwh	VIFDOT	15			ns
Clock cycle time	dotcyc	VIFDOT	30			ns

AC characteristics (Reset condition)

Fixing XRST pin to Lo level initializes the internal FF. The filter circuit that used delay device is embedded inside so that an error operation won't be performed even if a noise is on XRST pin. The condition of Lo period is as follows.

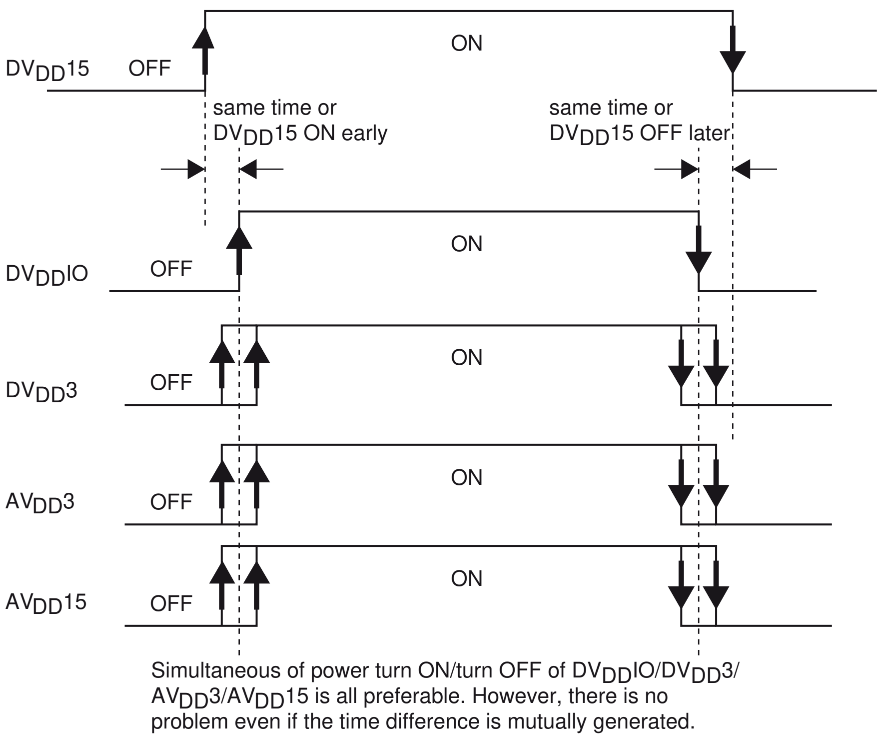


Lo period restricyion of XRST pin

Power turn-ON/turn OFF-conditions

This LSI needs digital power ($DV_{DD}15$ [core], $DV_{DD}3$ [DRAM], $DV_{DD}IO$), analog power for DAC ($AV_{DD}3$) and analog power for PLL ($AV_{DD}15$). Power turn ON/turn OFF conditions is shown in the following sequence diagram.

It is desirable for $DV_{DD}15$ and $DV_{DD}IO/DV_{DD}3$ to maintain
$DV_{DD}15 >= DV_{DD}IO/DV_{DD}3/AV_{DD}3/AV_{DD}15$ relation as below or at the same time.
However, the condition is acceptable when the period, which is the reversed relation, is within 1ms.
Simultaneous of power turn ON / turn OFF of $DV_{DD}IO/DV_{DD}3/AV_{DD}3/AV_{DD}15$ is all preferable. However, there is no problem even if the time difference is mutually generated.
However, please avoid keeping only a certain power supply in the state of power turn OFF.



Power turn-ON/turn-OFF sequence