19-2884; Rev 0; 7/03

EVALUATION KIT AVAILABLE

2.4GHz 802.11b Zero-IF Transceiver with Integrated PA and Tx/Rx Switch

MAX2822

General Description

The MAX2822 single-chip transceiver is designed for 802.11b (11Mbps) applications operating in the 2.4GHz to 2.5GHz ISM band. The transceiver includes all the circuitry required to implement an 802.11b RF-to-baseband transceiver solution, including the power amplifier, transmit/receive switch, and 50Ω matching. The fully integrated receive path, transmit path, VCO, frequency synthesis, and baseband/control interface provide all the required active RF circuitry. Only a small number of passive components are needed to form the complete radio front-end solution.

The IC eliminates the need for external IF SAW and RF image-reject filters by utilizing a direct-conversion radio architecture and monolithic baseband filters for both receiver and transmitter. It is specifically optimized for 802.11b (11Mbps CCK) and 22Mbps PBCC™ applications. The baseband filtering and Rx and Tx signal paths support the CCK modulation scheme for BER = 10^{-5} at the required sensitivity levels.

The transceiver is suitable for the full range of 802.11b data rates (1Mbps, 2Mbps, 5.5Mbps, and 11Mbps) as well as the higher-rate 22Mbps PBCC standard. The MAX2822 is available in the very small 7mm x 7mm 48-lead QFN or thin QFN packages. The small solution size makes it ideal for small form-factor 802.11b applications such as PDAs, SmartPhones, and embedded modules.

Features

- **2.4GHz to 2.5GHz ISM Band Operation**
- **802.11b (11Mbps CCK and 22Mbps PBCC) PHY Compatible**
- **Integrated +17dBm PA**
- **Integrated PA Power Detector**
- **Integrated Transmit/Receive Switch**
- **Complete RF-to-Baseband Transceiver**
  - **Direct Up/Down Conversion**
  - **Monolithic Low-Phase-Noise VCO**
  - **Integrated Baseband Lowpass Filters**
  - **Integrated PLL with 3-Wire Serial Interface**
  - **Digital Bias Control for PA**
  - **Transmit Power Control**
  - **Receive Baseband AGC**
  - **Complete Baseband Interface**
  - **Digital Tx/Rx Mode Control**
- **-95dBm Rx Sensitivity at 1Mbps**
- **-85dBm Rx Sensitivity at 11Mbps**
- **Single +2.7V to +3.0V Supply**
- **2µA Shutdown Mode**
- **Very Small 48-Pin QFN Package**

Applications

802.11b PDAs and SmartPhones

802.11b Embedded Modules

802.11b PC Cards, Mini-PCI Cards

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2822EGM	-40°C to +85°C	48 QFN
MAX2822ETM	-40°C to +85°C	48 Thin QFN

Pin Configuration/Functional Diagram appears at end of data sheet.

PBCC is a trademark of Texas Instruments, Inc.

ABSOLUTE MAXIMUM RATINGS

V_{CC} Pins to GND ....-0.3V to +3.6V
RF I/O: RFP, RFN (current into pin).....................................50mA
Baseband Inputs: TX_BBIP, TX_BBIN, TX_BBQP,
TX_BBQN to GND ....-0.3V to (V_{CC} + 0.3V)
Baseband Outputs: RX_BBIP, RX_BBIN, RX_BBQP,
RX_BBQN to GND.................................-0.3V to (V_{CC} + 0.3V)
Analog Inputs: RX_AGC, TX_GC, TUNE, ROSCN,
ROSCP to GND ....-0.3V to (V_{CC} + 0.3V)
Analog Outputs: PWR_DET, CP_OUT
to GND...-0.3V to (V_{CC} + 0.3V)
Digital Inputs: RX_ON, TX_ON, SHDNB, CSB, SCLK,
DIN, RF_GAIN, RX_1K to GND..............-0.3V to (V_{CC} + 0.3V)
Bias Voltages: RBIAS, BYP ....+0.9V to +1.5V
Short-Circuit Duration Digital Output: DOUT..........................10s
RF Input Power ....+10dBm
Continuous Power Dissipation (T_A = +70°C)
48-Lead QFN (derate 27.0mW/°C above +70°C) 2162mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX2822 EV kit: V_{CC} = +2.7V to +3.0V, RF_GAIN = V_{IH}, 0V ≤ V_{TX_GC} ≤ +2.0V, 0V ≤ V_{RX_AGC} ≤ +2.0V, R_{BIAS} = 12kΩ, no input signals at RF and baseband inputs, RF I/O terminated into 50Ω though a 2:1 balun, receiver baseband outputs are open, transmitter baseband inputs biased at +1.2V, registers set to default power-up settings, T_A = -40°C to +85°C, unless otherwise noted. Typical values are for V_{CC} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.7		3.0	V
Shutdown Current	SHDNB = V_{IL}, RX_ON = V_{IL}, TX_ON = V_{IL}		2	50	µA
Standby-Mode Supply Current	SHDNB = V_{IH}, RX_ON = V_{IL}, TX_ON = V_{IL}; T_A = +25°C		25	35	mA
	SHDNB = V_{IH}, RX_ON = V_{IL}, TX_ON = V_{IL}; T_A = -40°C to +85°C			40	
Receive-Mode Supply Current	SHDNB = V_{IH}, RX_ON = V_{IH}, TX_ON = V_{IL}; T_A = +25°C		80	100	mA
	SHDNB = V_{IH}, RX_ON = V_{IH}, TX_ON = V_{IL}; T_A = -40°C to +85°C			110	
Transmit-Mode Supply Current	SHDNB = V_{IH}, RX_ON = V_{IL}, TX_ON = V_{IH}, bias registers set as in Table 9; P_{OUT} = +3dBm		98		mA
	P_{OUT} = +12dBm; T_A = +25°C		157	175	
	P_{OUT} = +12dBm; T_A = -40°C to +85°C			185	
	P_{OUT} = +17dBm		220		
LOGIC INPUTS: SHDNB, RX_ON, TX_ON, SCLK, DIN, CSB, RF_GAIN					
Digital Input Voltage High (V_{IH})		V_{CC} - 0.5			V
Digital Input Voltage Low (V_{IL})				0.5	V
Digital Input Current High (I_{IH})		-5		+5	µA
Digital Input Current Low (I_{IL})		-5		+5	µA
LOGIC OUTPUT: DOUT					
Digital Output Voltage High (V_{OH})	Sourcing 100µA	V_{CC} - 0.5			V
Digital Output Voltage Low (V_{OL})	Sinking 100µA			0.5	V
ANALOG OUTPUT: PWR_DET					
Power-Detector Output Impedance			400		Ω

DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2822 EV kit: V_{CC} = +2.7V to +3.0V, RF_GAIN = V_{IH}, 0V ≤ V_{TX_GC} ≤ +2.0V, 0V ≤ V_{RX_AGC} ≤ +2.0V, R_{BIAS} = 12kΩ, no input signals at RF and baseband inputs, RF I/O terminated into 50Ω though a 2:1 balun, receiver baseband outputs are open, transmitter baseband inputs biased at +1.2V, registers set to default power-up settings, T_A = -40°C to +85°C, unless otherwise noted. Typical values are for V_{CC} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
RX BASEBAND I/O					
RX_AGC Input Resistance	0V ≤ V_{RX_AGC} ≤ +2.0V		50		kΩ
Rx I/Q Common-Mode Voltage			1.25		V
Rx I/Q Output DC Offsets	3σ limit		±15		mV
TX BASEBAND I/O					
TX BB Input Common-Mode Range		1.0	1.2	1.4	V
TX BBI and BBQ Input Bias Current			-10		µA
TX BB Input Impedance	Differential resistance		100		kΩ
TX_GC Input Bias Current	0V ≤ V_{TX_GC} ≤ +2.0V		10		µA
TX_GC Input Impedance	Resistance		250		kΩ
REFERENCE OSCILLATOR INPUT					
Reference Oscillator Input Impedance			20		kΩ
VOLTAGE REFERENCE					
Reference Voltage	I_{LOAD} = ±2mA	1.10	1.20	1.30	V

AC ELECTRICAL CHARACTERISTICS—RECEIVE MODE

(MAX2822 EV kit: V_{CC} = +2.7V to +3.0V, f_{RF} and f_{LO} = 2400MHz to 2499MHz, f_{OSC} = 22MHz or 44MHz, receive baseband output levels = 500mV_{P-P}, V_{SHDNB} = V_{RX_ON} = V_{IH}, V_{TX_ON} = V_{IL}, V_{CSB} = V_{IH}, V_{SCLK} = V_{DIN} = V_{IL}, V_{RF_GAIN} = V_{IH}, 0V ≤ V_{RX_AGC} ≤ +2.0V, R_{BIAS} = 12kΩ, I_{CP} = +2mA, BW_{PLL} = 45kHz, registers set to default power-up settings, T_A = +25°C, unless otherwise noted. Typical values are for V_{CC} = +2.7V, f_{LO} = 2437MHz, f_{OSC} = 22MHz, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER CASCADED PERFORMANCE (RF INPUT TO BASEBAND OUTPUT)						
RF Frequency Range			2400		2499	MHz
LO Frequency Range			2400		2499	MHz
Voltage Gain (Note 3)	RF_GAIN = V_{IH}, V_{RX_AGC} = 0V	T_A = +25°C	97	105		dB
		T_A = -40°C to +85°C	95			
	RF_GAIN = V_{IH}, V_{RX_AGC} = +2.0V			35		
	RF_GAIN = V_{IL}, V_{RX_AGC} = 0V			75		
	RF_GAIN = V_{IL}, V_{RX_AGC} = +2.0V			3		
RF Gain Step	From RF_GAIN = V_{IH} to RF_GAIN = V_{IL}			32		dB

2.4GHz 802.11b Zero-IF Transceiver with Integrated PA and Tx/Rx Switch

AC ELECTRICAL CHARACTERISTICS—RECEIVE MODE (continued)

(MAX2822 EV kit: V_{CC} = +2.7V to +3.0V, f_{RF} and f_{LO} = 2400MHz to 2499MHz, f_{OSC} = 22MHz or 44MHz, receive baseband output levels = 500mV_{P-P}, V_{SHDNB} = V_{RX_ON} = V_{IH}, V_{TX_ON} = V_{IL}, V_{CSB} = V_{IH}, V_{SCLK} = V_{DIN} = V_{IL}, V_{RF_GAIN} = V_{IH}, 0V ≤ V_{RX_AGC} ≤ +2.0V, R_{BIAS} = 12kΩ, I_{CP} = +2mA, BW_{PLL} = 45kHz, registers set to default power-up settings, T_A = +25°C, unless otherwise noted. Typical values are for V_{CC} = +2.7V, f_{LO} = 2437MHz, f_{OSC} = 22MHz, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DSB Noise Figure (Note 4)	RF_GAIN = V_{IH}, RX gain ≥ 80dB		5.5	6.0	dB
	RF_GAIN = V_{IH}, RX gain = 50dB		8		
	RF_GAIN = V_{IL}, RX gain = 50dB		35		
Adjacent Channel Rejection	RX gain = 70dB (Note 5)		45		dB
Input Third-Order Intercept Point (Note 6)	RF_GAIN = V_{IH}, RX gain = 80dB		-13		dBm
	RF_GAIN = V_{IL}, RX gain = 50dB		+19		
Input Second-Order Intercept Point (Note 7)	RF_GAIN = V_{IH}, RX gain = 80dB		+23		dBm
	RF_GAIN = V_{IL}, RX gain = 50dB		+60		
LO Leakage	At balun input		-65		dBm
Input Return Loss			15		dB
RECEIVER BASEBAND					
BASEBAND FILTER RESPONSE					
-3dB Frequency	Default bandwidth setting BW(2:0) = (010)		7		MHz
Attenuation Relative to Passband	At 12.5MHz		40		dB
	At 16MHz		65		
	At 20MHz		70		
	At 25MHz		85		
BASEBAND OUTPUT CHARACTERISTICS					
Rx I/Q Gain Imbalance	3σ limit		±1		dB
Rx I/Q Phase Quadrature Imbalance	3σ limit		±5		Degrees
Rx I/Q Output 1dB Compression	Differential voltage into 5kΩ		1		V_{P-P}
Rx I/Q Output THD	V_{OUT} = 500mV_{P-P} at 5.5MHz, Z_L = 5kΩ‖5pF		-35		dBc
BASEBAND AGC AMPLIFIER					
AGC Range	V_{RX_AGC} = 0 to +2.0V		70		dB
AGC Slope	Peak gain slope		60		dB/V
AGC Response Time	20dB gain step (80dB to 60dB), settling to ±1dB		2		µs

AC ELECTRICAL CHARACTERISTICS—TRANSMIT MODE

(MAX2822 EV kit, characteristics relative to RFP/RFN: V_{CC} = +2.7V to +3.0V, f_{RF} and f_{LO} = 2400MHz to 2499MHz, f_{OSC} = 22MHz or 44MHz, transmit baseband input signal: 500mV_{P-P} at 5.5MHz, V_{SHDNB} = V_{RX_ON} = V_{IL}, V_{TX_ON} = V_{IH}, V_{CSB} = V_{IH}, V_{SCLK} = V_{DIN} = V_{IL}, V_{RF_GAIN} = V_{IH}, 0V ≤ V_{TX_AGC} ≤ +2.0V, R_{BIAS} = 12kΩ, I_{CP} = +2mA, BW_{PLL} = 45kHz, baseband inputs DC biased to +1.2V, registers set to default power-up settings, measurements taken within 1s of TXON rising edge, T_A = +25°C, unless otherwise noted. Typical values are for V_{CC} = +2.7V, f_{LO} = 2437MHz, f_{OSC} = 22MHz, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMIT SIGNAL PATH: BASEBAND INPUT TO RF OUTPUT						
RF Output Frequency Range			2400		2499	MHz
LO Output Frequency Range			2400		2499	MHz
Tx RF Output Power	11Mbps CCK signal, ACPR (adj) ≤ -30dBc, ACPR (alt) ≤ -50dBc (Note 4)	T_A = +25°C	+16.5	+17.5		dBm
		T_A = -40°C to +85°C	+15.5			
Tx RF ACPR (Note 8)	Adjacent (adj): -22MHz ≤ f_{OFFSET} ≤ -11MHz, 11MHz ≤ f_{OFFSET} ≤ 22MHz, P_{OUT} = +16.5dBm			-33		dBc
	Alternate (alt): -33MHz ≤ f_{OFFSET} < -22MHz, 22MHz < f_{OFFSET} ≤ 33MHz, P_{OUT} = +16.5dBm			-56		
In-Band Spurious Signals Relative to Carrier	f_{RF} = 2400MHz to 2483MHz (Note 9)	Unwanted sideband		-40		dBc
		LO signal		-30		
		Spurs > ±22MHz		-80		
Tx RF Harmonics	11Mbps CCK at +16.5dBm	2 × f_{RF}		-45		dBm
		3 × f_{RF}		-30		
Tx RF Spurious Signal Emissions (Outside 2400MHz to 2483.5MHz) Nonharmonic Signals	< 2400MHz			-50		dBm
	2500MHz to 3350MHz			-35		
	> 3350MHz			-40		
Tx RF Output Noise	f_{OFFSET} ≥ 22MHz, 0V ≤ V_{TX_GC} ≤ +2.0V			-125		dBm/Hz
Tx RF Output Return Loss	100Ω balanced output impedance, P_{OUT} = +17dBm			10		dB
Tx BASEBAND FILTER RESPONSE						
-3dB Frequency				10		MHz
Attenuation Relative to Passband	At 22MHz			25		dB
	At 44MHz			50		
Tx GAIN-CONTROL CHARACTERISTICS						
Gain-Control Range	0V ≤ V_{TX_GC} ≤ +2.0V			20		dB
Gain-Control Slope	Peak gain slope			30		dB/V
Gain-Control Response Time	V_{TX_GC} = +2.0V to 0V step, settled to within ±1dB			0.3		µs

AC ELECTRICAL CHARACTERISTICS—TRANSMIT MODE (continued)

(MAX2822 EV kit, characteristics relative to RFP/RFN: V_{CC} = +2.7V to +3.0V, f_{RF} and f_{LO} = 2400MHz to 2499MHz, f_{OSC} = 22MHz or 44MHz, transmit baseband input signal: 500mV_{P-P} at 5.5MHz, V_{SHDNB} = V_{RX_ON} = V_{IL}, V_{TX_ON} = V_{IH}, V_{CSB} = V_{IH}, V_{SCLK} = V_{DIN} = V_{IL}, V_{RF_GAIN} = V_{IH}, 0V ≤ V_{TX_AGC} ≤ +2.0V, R_{BIAS} = 12kΩ, I_{CP} = +2mA, BW_{PLL} = 45kHz, baseband inputs DC biased to +1.2V, registers set to default power-up settings, measurements taken within 1s of TXON rising edge, T_A = +25°C, unless otherwise noted. Typical values are for V_{CC} = +2.7V, f_{LO} = 2437MHz, f_{OSC} = 22MHz, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER DETECTOR						
Power-Detection Range	0.1V ≤ V_{PWR_DET} ≤ 1.5V			17		dB
Power-Detection Error (3σ Limit)	Fixed V_{PWR_DET}, T_A = +25°C	P_{OUT} = +3dBm		±0.7		dB
		P_{OUT} = +17dBm		±0.5		
Power-Detection Error Variation with Temperature	T_A = -40°C to +85°C, relative to T_A = +25°C			±0.3		dB

AC ELECTRICAL CHARACTERISTICS—SYNTHESIZER

(MAX2822 EV kit: V_{CC} = +2.7V to +3.0V, f_{RF} and f_{LO} = 2400MHz to 2499MHz, f_{OSC} = 22MHz or 44MHz, SHDNB = V_{IH}, CSB = V_{IH}, R_{BIAS} = 12kΩ, I_{CP} = +2mA, BW_{PLL} = 45kHz, registers set to default power-up settings, T_A = +25°C, unless otherwise noted. Typical values are for V_{CC} = +2.7V, f_{LO} = 2437MHz, f_{OSC} = 22MHz, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER					
LO Frequency Range		2400		2499	MHz
Reference Frequency	SYNTH:R(0) = 0		22		MHz
	SYNTH:R(0) = 1		44		
Minimum Channel Spacing			1		MHz
Charge-Pump Output Current			±2		mA
Charge-Pump Compliance Range		0.4		V_{CC} - 0.4	V
Reference Spur Level (Note 10)	-11MHz ≤ f_{OFFSET} ≤ 11MHz		-41		dBc
	-22MHz ≤ f_{OFFSET} < -11MHz, 11MHz < f_{OFFSET} ≤ 22MHz		-75		
	f_{OFFSET} < -22MHz, f_{OFFSET} > 22MHz		-90		
Closed-Loop Phase Noise	f_{OFFSET} = 10kHz		-80		dBc/Hz
	f_{OFFSET} = 100kHz		-87		
Closed-Loop Integrated Phase Noise	Noise integrated from 100Hz to 10MHz, measured at the TX_RF output		2.5		$°_{RMS}$
Reference Oscillator Input Level	AC-coupled sine wave input	200	300	500	mV_{P-P}
VOLTAGE-CONTROLLED OSCILLATOR					
VCO Tuning Voltage Range	f_{LO} = 2400MHz	0.4			V
	f_{LO} = 2499MHz			2.3	
VCO Tuning Gain	f_{LO} = 2400MHz		170		MHz/V
	f_{LO} = 2499MHz		130		

AC ELECTRICAL CHARACTERISTICS—SYSTEM TIMING

(MAX2822 EV kit: V_{CC} = +2.7V to +3.0V, f_{RF} and f_{LO} = 2400MHz to 2499MHz, f_{OSC} = 22MHz or 44MHz, SHDNB = V_{IH}, CSB = V_{IH}, R_{BIAS} = 12kΩ, I_{CP} = +2mA, BW_{PLL} = 45kHz, registers set to default power-up settings, T_A = +25°C, unless otherwise noted. Typical values are for V_{CC} = +2.7V, f_{LO} = 2437MHz, f_{OSC} = 22MHz, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Channel-Switching Time	f_{LO} = 2400MHz ↔ 2499MHz, f_{LO} settles to ±10kHz (Note 11)		150	200	µs
Rx/Tx Turnaround Time	Rx to Tx, f_{LO} settles to within ±30kHz, relative to the rising edge of TX_ON			5	µs
	Tx to Rx, f_{LO} settles to within ±30kHz, relative to the rising edge of RX_ON			10	
Standby-to-Receive Mode	Standby to Rx, f_{LO} settles to within ±30kHz, relative to the rising edge of RX_ON			10	µs
Standby-to-Transmit Mode	Standby to Tx, f_{LO} settles to within ±30kHz, relative to the rising edge of TX_ON			5	µs

AC ELECTRICAL CHARACTERISTICS—SERIAL INTERFACE TIMING

(MAX2822 EV kit: V_{CC} = +2.7V to +3.0V, registers set to default power-up settings, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE TIMING (SEE FIGURE 1)					
t_{CSO}	SCLK rising edge to CSB falling edge wait time	5			ns
t_{CSS}	Falling edge of CSB to rising edge of first SCLK time	5			ns
t_{DS}	Data-to-serial clock setup time	5			ns
t_{DH}	Data-to-clock hold time	10			ns
t_{CH}	Serial clock pulse-width high	10			ns
t_{CL}	Clock pulse-width low	10			ns
t_{CSH}	Last SCLK rising edge to rising edge of CSB	5			ns
t_{CSW}	CSB high pulse width	10			ns
t_{CS1}	Time between the rising edge of CSB and the next rising edge of SCLK	5			ns
f_{CLK}	Clock frequency			50	MHz

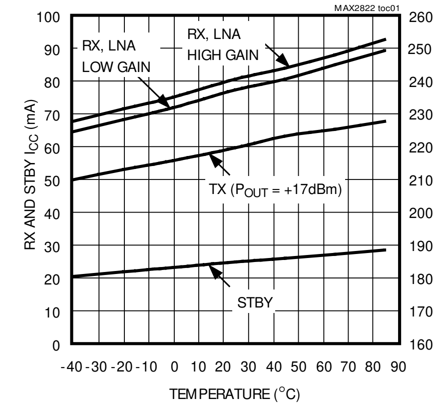
Note 1: Parameters are production tested at +25°C only. Min/max limits over temperature are guaranteed by design and characterization.
Note 2: Guaranteed by design and characterization.
Note 3: Defined as the baseband differential RMS output voltage divided by the RMS input voltage (at the RF balun input).
Note 4: Specification excludes the loss of the external balun. The external balun loss is typically ~0.5dB.
Note 5: CCK interferer at 25MHz offset. Desired signal equals -73dBm. Interferer amplitude increases until baseband output from interferer is 10dB below desired signal. Adjacent channel rejection = $P_{INTERFERER}$ - $P_{DESIRED}$.
Note 6: Measured at balun input. Two CW tones at -43dBm with 15MHz and 25MHz offset from the MAX2822 channel frequency. IP3 is computed from 5MHz IMD3 product measured at the Rx I/Q output.
Note 7: Two CW interferers at -38dBm with 24.5MHz and 25.5MHz offset from the MAX2822 channel frequency. IP2 is computed from the 1MHz IMD2 product measured at the RX I/Q output.
Note 8: V_{TXGC} adjusted for +16.5dBm output power; adjacent and alternate channel power relative to the desired signal. Power measured with 100kHz video BW and 100kHz resolution BW.
Note 9: CW tone at 2.25MHz offset from carrier with V_{TXGC} set for maximum modulated P_{OUT} at -30dBc/-50dBc (ADJ/ALT) ACPR limits. Unwanted sideband refers to suppressed image resulting from I/Q baseband input tones.
Note 10: Relative amplitude of reference spurious products appearing in the Tx RF output spectrum relative to a CW tone at 2.25MHz offset from the LO.
Note 11: Time required to reprogram the PLL, change the operating channel, and wait for the operating channel center frequency to settle within ±10kHz of the nominal (final) channel frequency.

2.4GHz 802.11b Zero-IF Transceiver with Integrated PA and Tx/Rx Switch

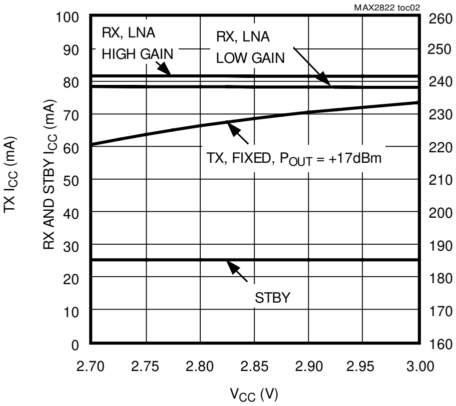
Typical Operating Characteristics

(MAX2822 EV kit, V_{CC} = +2.7V, f_{BB} = 1MHz, f_{LO} = 2437MHz, receive baseband outputs = 500mV$_{P-P}$, transmit baseband inputs = 400mV$_{P-P}$, ICP = +2mA, BWPLL = 45kHz, differential RF input/output matched to 50Ω through a balun, baseband input biased at +1.2V, registers set to default power-up settings, T_A = +25°C, unless otherwise noted.)

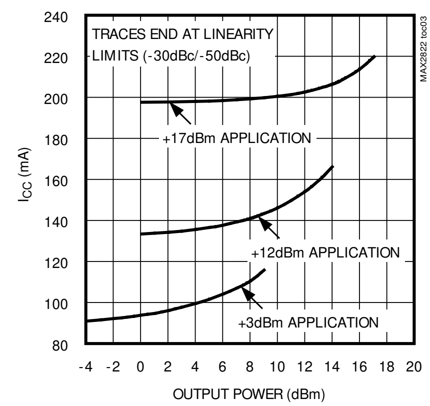
SUPPLY CURRENT vs. TEMPERATURE



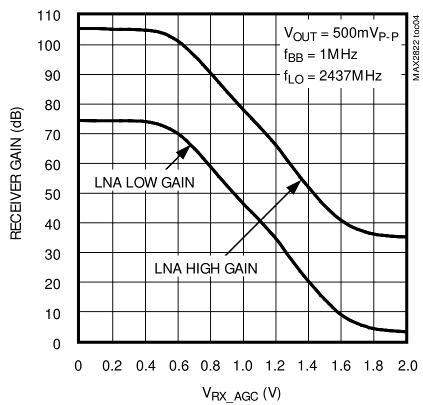
SUPPLY CURRENT vs. SUPPLY VOLTAGE



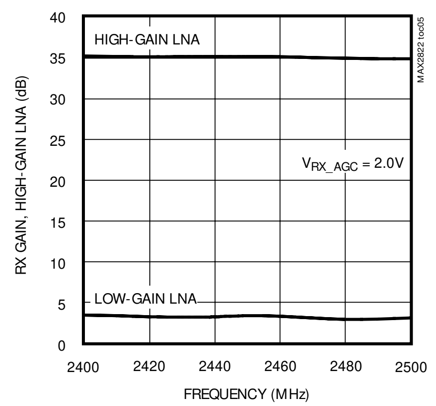
SUPPLY CURRENT vs. TX OUTPUT POWER



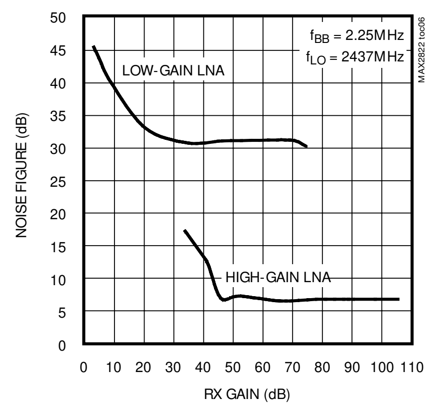
RECEIVER GAIN vs. GAIN-CONTROL VOLTAGE



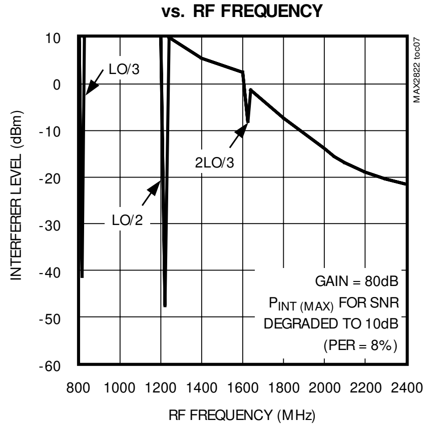
RECEIVER VOLTAGE GAIN vs. FREQUENCY



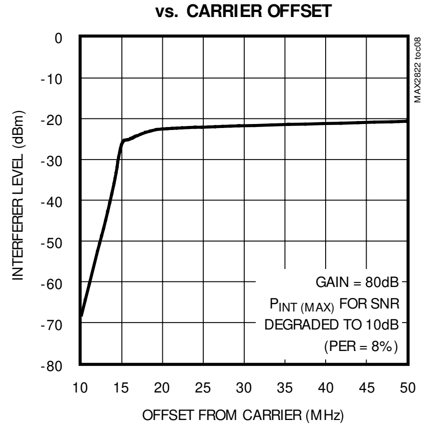
RECEIVER NOISE FIGURE vs. GAIN



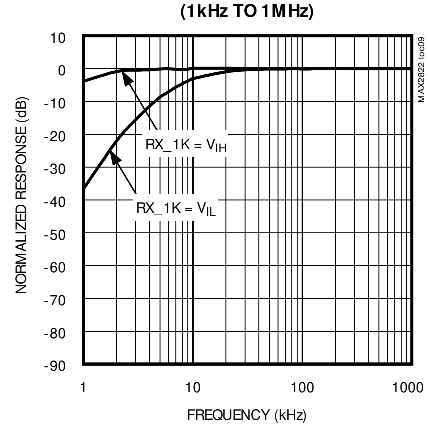
RECEIVER BLOCKER REJECTION vs. RF FREQUENCY



RECEIVER BLOCKER REJECTION vs. CARRIER OFFSET



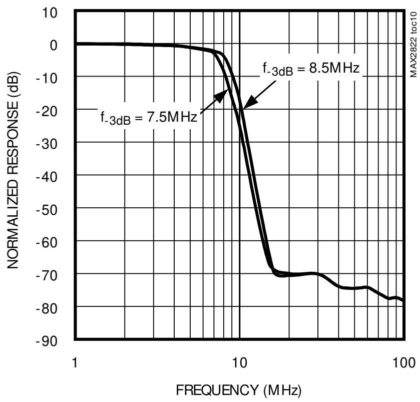
RECEIVER FILTER RESPONSE (1kHz TO 1MHz)



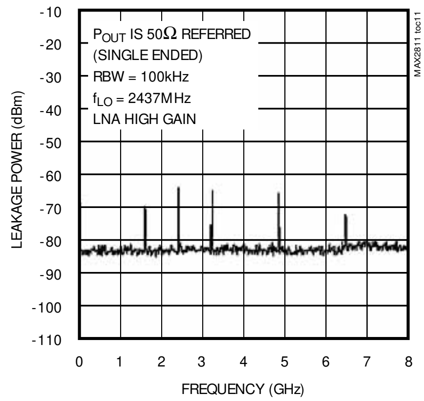
Typical Operating Characteristics (continued)

(MAX2822 EV kit, V_{CC} = +2.7V, f_{BB} = 1MHz, f_{LO} = 2437MHz, receive baseband outputs = 500mV_{P-P}, transmit baseband inputs = 400mV_{P-P}, ICP = +2mA, BWPLL = 45kHz, differential RF input/output matched to 50Ω through a balun, baseband input biased at +1.2V, registers set to default power-up settings, T_A = +25°C, unless otherwise noted.)

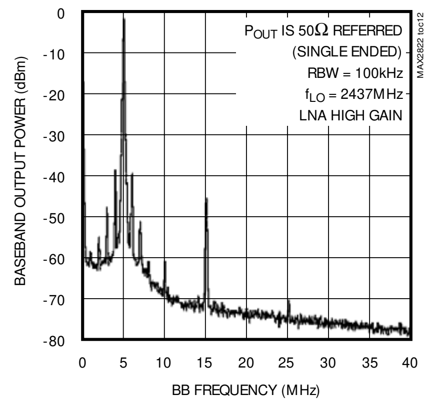
RECEIVER FILTER RESPONSE (1MHz TO 100MHz)



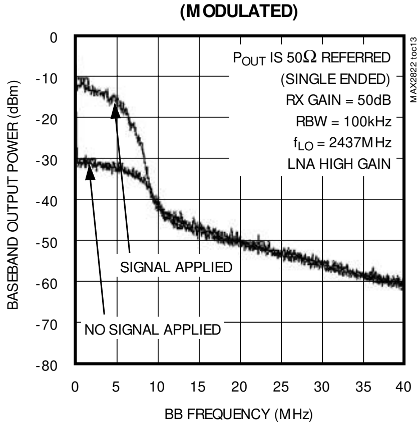
RECEIVER LEAKAGE SPECTRUM



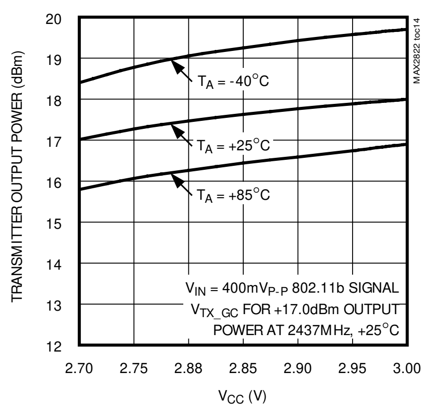
RECEIVER BASEBAND OUTPUT SPECTRUM (SINGLE TONE)



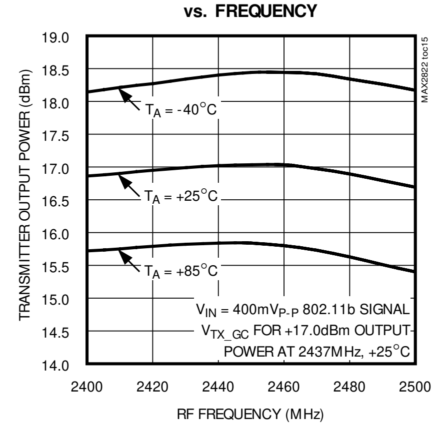
RECEIVER BASEBAND OUTPUT SPECTRUM (MODULATED)



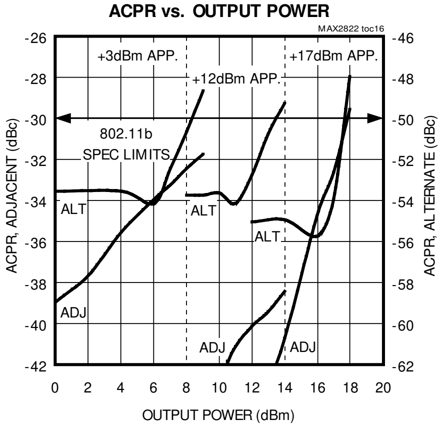
TRANSMITTER OUTPUT POWER vs. SUPPLY VOLTAGE



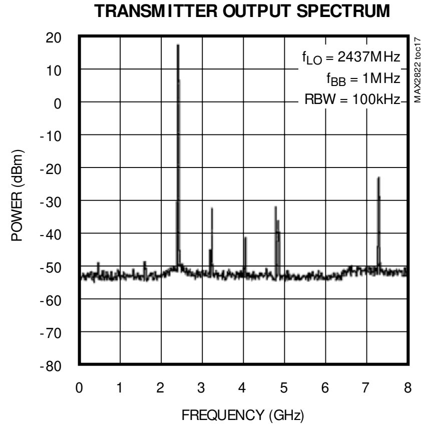
TRANSMITTER OUTPUT POWER vs. FREQUENCY



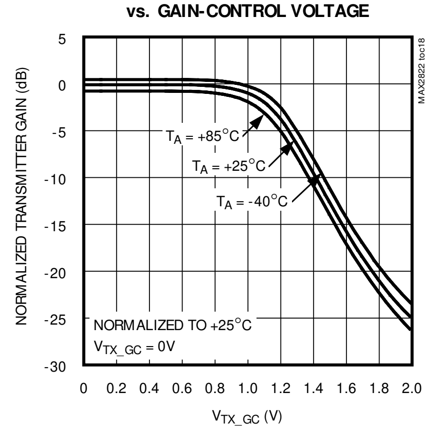
ACPR vs. OUTPUT POWER



TRANSMITTER OUTPUT SPECTRUM



TRANSMITTER GAIN vs. GAIN-CONTROL VOLTAGE

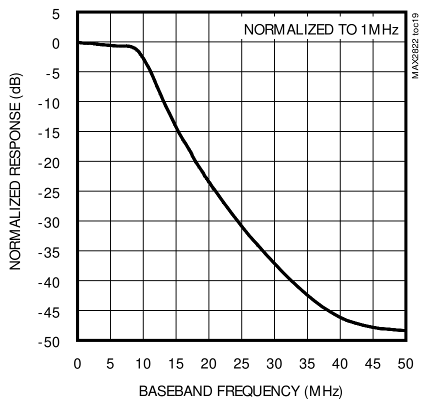


2.4GHz 802.11b Zero-IF Transceiver with Integrated PA and Tx/Rx Switch

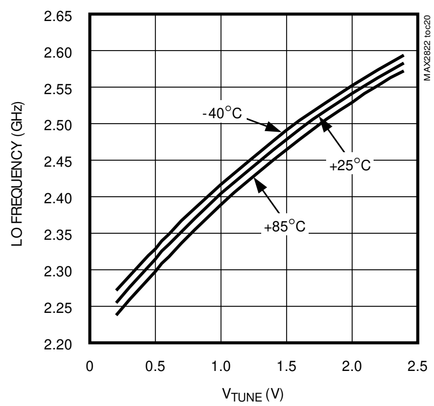
Typical Operating Characteristics (continued)

(MAX2822 EV kit, V_{CC} = +2.7V, f_{BB} = 1MHz, f_{LO} = 2437MHz, receive baseband outputs = 500mV_{P-P}, transmit baseband inputs = 400mV_{P-P}, ICP = +2mA, BWPLL = 45kHz, differential RF input/output matched to 50Ω through a balun, baseband input biased at +1.2V, registers set to default power-up settings, T_A = +25°C, unless otherwise noted.)

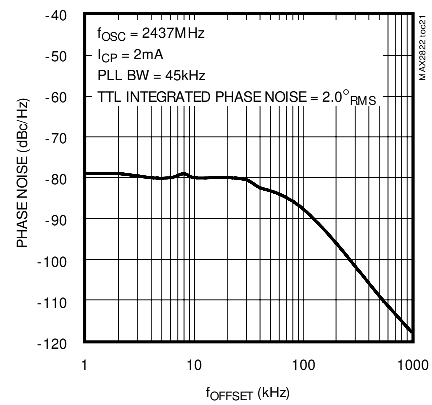
TRANSMITTER BASEBAND FILTER RESPONSE



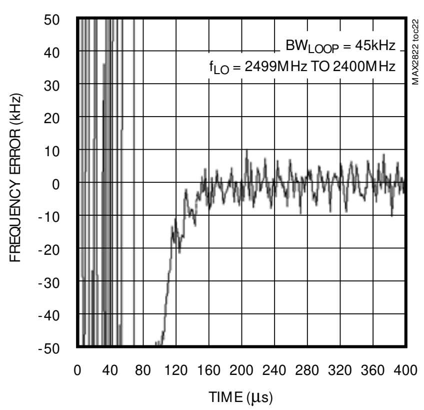
LO FREQUENCY vs. TUNING VOLTAGE



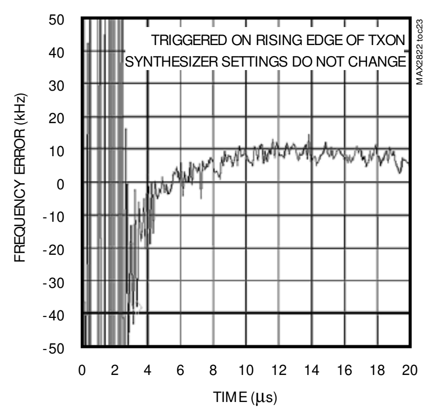
SYNTHESIZER CLOSED-LOOP PHASE NOISE



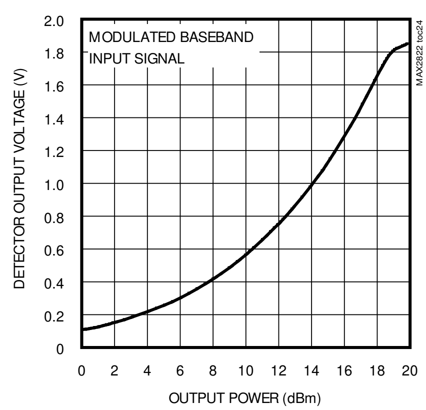
VCO/PLL SETTING TIME



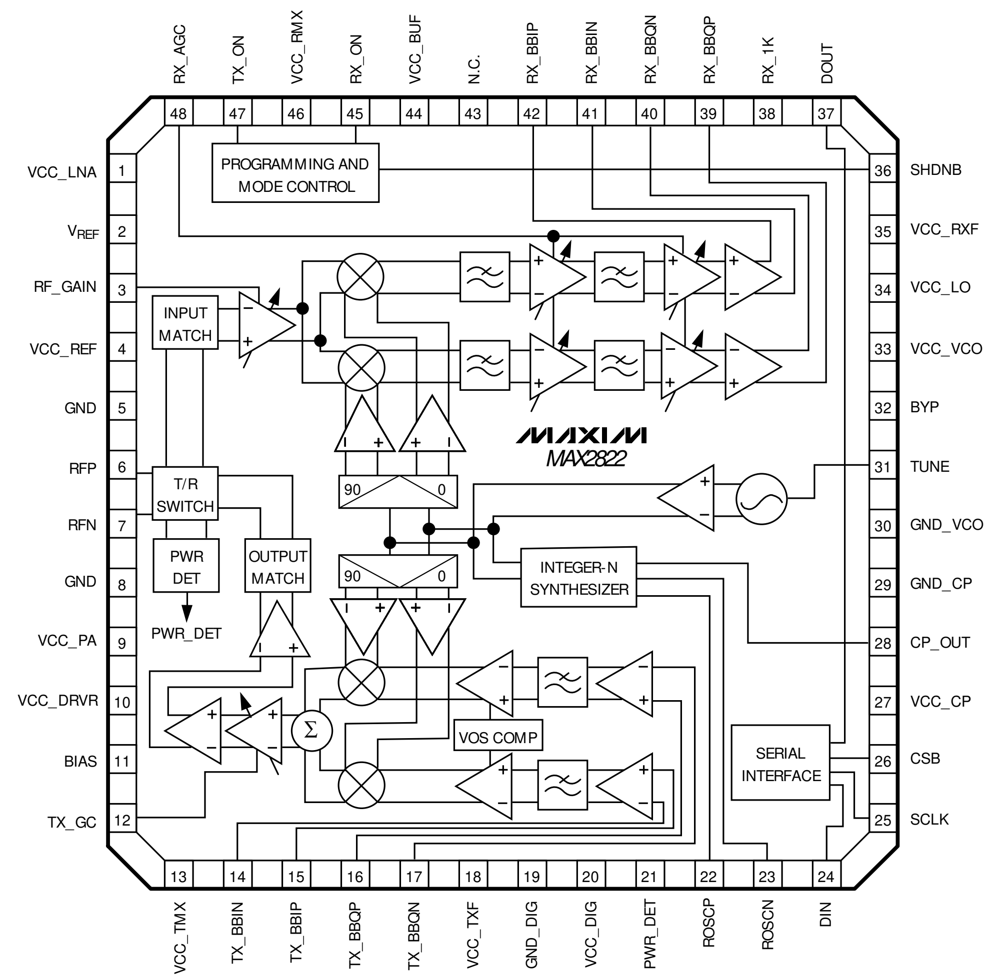
RX/TX TURNAROUND TIME



PA POWER-DETECTOR OUTPUT VOLTAGE vs. OUTPUT POWER



Pin Configuration/Functional Diagram



2.4GHz 802.11b Zero-IF Transceiver with Integrated PA and Tx/Rx Switch

Pin Description

PIN	NAME	FUNCTION
1	VCC_LNA	Supply Voltage Connection for LNA. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.
2	V_{REF}	Voltage Reference Output for Baseband IC. Requires external RF bypass to GND.
3	RF_GAIN	LNA Gain-Select Logic Input. Logic high for LNA high-gain mode, logic low for LNA low-gain mode.
4	VCC_REF	Supply Voltage for Bias Circuitry and Autotuner. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.
5, 8	GND	Ground
6	RFP	RF Balanced I/O Port (Positive). On-chip matched for 100Ω balanced.
7	RFN	RF Balanced I/O Port (Negative). On-chip matched for 100Ω balanced.
9	VCC_PA	Supply Voltage Connection for Power Amplifier. Requires external RF bypass to GND.
10	VCC_DRVR	Supply Voltage Connection for PA Driver. Requires external RF bypass to GND.
11	BIAS	Precision Bias Resistor Pin. Connect a 12kΩ precision resistor (≤ 2%) to GND.
12	TX_GC	Transmit Gain-Control Input. Analog high-impedance input. Connect directly to baseband IC DAC output. See Figure 3 for transmitter gain vs. gain-control voltage.
13	VCC_TMX	Supply Voltage for Transmit Mixer and VGA. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.
14	TX_BBIN	Transmit Negative In-Phase Baseband Input. Analog high-impedance differential input. Connect directly to baseband IC DAC voltage output. Requires a 1.2V common-mode voltage.
15	TX_BBIP	Transmit Positive In-Phase Baseband Input. Analog high-impedance differential input. Connect directly to baseband IC DAC voltage output. Requires a 1.2V common-mode voltage.
16	TX_BBQP	Transmit Positive Quadrature Baseband Input. Analog high-impedance differential input. Connect directly to baseband IC DAC voltage output. Requires a 1.2V common-mode voltage.
17	TX_BBQN	Transmit Negative Quadrature Baseband Input. Analog high-impedance differential input. Connect directly to baseband IC DAC voltage output. Requires a 1.2V common-mode voltage.
18	VCC_TXF	Supply Voltage for Transmit Baseband Filter. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.
19	GND_DIG	Digital Ground
20	VCC_DIG	Supply Voltage for Digital Circuitry. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.
21	PWR_DET	Transmitter Power-Detector Output
22	ROSCP	Reference Oscillator Positive Input. Analog high-impedance differential input. DC-coupled. Requires external AC-coupling. Connect an external reference oscillator to this analog input.
23	ROSCN	Reference Oscillator Negative Input. Analog high-impedance differential input. DC-coupled. Requires external AC-coupling. Bypass this analog input to ground with capacitor for single-ended operation.
24	DIN	3-Wire Serial Interface Data Input. Digital high-impedance input. Connect directly to baseband IC serial interface CMOS output (SPI™/QSPI™/MICROWIRE™ compatible).
25	SCLK	3-Wire Serial Interface Clock Input. Digital high-impedance input. Connect this digital input directly to baseband IC serial interface CMOS output (SPI/QSPI/MICROWIRE compatible).

Pin Description (continued)

PIN	NAME	FUNCTION
26	CSB	3-Wire Serial Interface Enable Input. Digital high-impedance input. Connect directly to baseband IC serial interface CMOS output (SPI/QSPI/MICROWIRE compatible).
27	VCC_CP	Supply Voltage for PLL Charge Pump. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.
28	CP_OUT	PLL Charge-Pump Output. Analog high-impedance output. Current source. Connect directly to the PLL loop filter input.
29	GND_CP	PLL Charge-Pump Ground. Connect to PC board ground plane.
30	GND_VCO	VCO Ground. Connect to PC board ground plane.
31	TUNE	VCO Frequency Tuning Input. Analog high-impedance voltage input. Connect directly to the PLL loop filter output.
32	BYP	VCO Bias Bypass. Bypass with a 2000pF capacitor to ground.
33	VCC_VCO	Supply Voltage for VCO. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. **Important note:** Operate from separate regulated supply voltage.
34	VCC_LO	Supply Voltage for VCO, LO Buffers, and LO Quadrature Circuitry. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.
35	VCC_RXF	Supply Voltage for Receiver Baseband Filter. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.
36	SHDNB	Active-Low Shutdown Input. Digital high-impedance CMOS input. Connect directly to baseband IC mode-control CMOS output. Logic low to disable all device functions. Logic high to enable normal chip operation.
37	DOUT	Serial Interface Data Output. Digital CMOS output. Optional connection.
38	RX_1K	Receiver 1kHz Highpass Bandwidth Control. Digital CMOS input. Connect directly to baseband IC CMOS output. Controls receiver baseband highpass -3dB corner frequency; logic low for 10kHz, logic high for 1kHz. See the *Applications Information* section for proper use of this function.
39	RX_BBQP	Receive Positive Quadrature Baseband Output. Analog low-impedance differential buffer output. Connect output directly to baseband ADC input. Internally biased to 1.2V common-mode voltage and can drive loads up to 5kΩ || 5pF.
40	RX_BBQN	Receive Negative Quadrature Baseband Output. Analog low-impedance differential buffer output. Connect output directly to baseband ADC input. Internally biased to 1.2V common-mode voltage and can drive loads up to 5kΩ || 5pF.
41	RX_BBIN	Receive Negative In-Phase Baseband Output. Analog low-impedance differential buffer output. Connect output directly to baseband ADC input. Internally biased to 1.2V common-mode voltage and can drive loads up to 5kΩ || 5pF.
42	RX_BBIP	Receive Positive In-Phase Baseband Output. Analog low-impedance differential buffer output. Connect output directly to baseband ADC input. Internally biased to 1.2V and can drive loads up to 5kΩ || 5pF.
43	N.C.	No Connection. Make no connections to this pin.
44	VCC_BUF	Supply Voltage for Receiver Baseband Buffer. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.

2.4GHz 802.11b Zero-IF Transceiver with Integrated PA and Tx/Rx Switch

Pin Description (continued)

PIN	NAME	FUNCTION
45	RX_ON	Receiver-On Control Input. Digital CMOS input. Connect to baseband IC mode-control CMOS output.
46	VCC_RMX	Supply Voltage for Receiver Downconverter. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches.
47	TX_ON	Transmitter-On Control Input. Digital CMOS input. Connect directly to baseband IC mode-control CMOS output.
48	RX_AGC	Receive AGC Control. Analog high-impedance input. Connect directly to baseband IC DAC voltage output. See Figure 2 for gain vs. V_{RX_AGC}.
Exposed Paddle	GND	DC and AC Ground Return for IC. Connect to PC board ground plane using multiple vias.

Table 1. Operating Mode Truth Table

OPERATING MODE	MODE-CONTROL INPUTS			CIRCUIT BLOCK STATES		
	SHDNB	TX_ON	RX_ON	RX_PATH	TX_PATH	PLL/VCO/LO GEN
Shutdown	0	X	X	OFF	OFF	OFF
Standby	1	0	0	OFF	OFF	ON
Receive	1	0	1	ON	OFF	ON
Transmit	1	1	0	OFF	ON	ON
Not Allowed	1	1	1	—	—	—

Detailed Description

Operating Modes

The MAX2822 has four primary modes of operation: shutdown, standby, receive active, and transmit active. The modes are controlled by the digital inputs SHDNB, TX_ON, and RX_ON. Table 1 shows the operating mode vs. the digital mode-control inputs.

Shutdown Mode

Shutdown mode is enabled by driving SHDNB low. In shutdown mode, all circuit blocks are powered down, except for the serial interface circuitry. While the device is in shutdown, the serial interface registers can still be loaded by applying V_{CC} to the digital supply voltage (VCC_DIG). All previously programmed register values are preserved during the shutdown mode, as long as VCC_DIG is applied.

Standby Mode

Standby mode is achieved by driving SHDNB high, and RX_ON and TX_ON low. In standby mode, the PLL, VCO, LO generation circuitry, and filter autotuner are powered on by default. The standby mode is intended to provide time for the slower-settling circuitry (PLL and autotuner) to turn on and settle to the correct frequency before making Rx or Tx active. The 3-wire serial interface is active and can load register values at any time. Refer to the serial interface specifications for details.

Receive Mode

Receive mode is enabled by driving SHDNB high, RX_ON high, and TX_ON low. In receive mode, all receive circuit blocks are powered on and all VCO, PLL, and autotuner circuits are powered on. None of the transmit path blocks are active in this mode. Although the receiver blocks turn on quickly, the DC offset nulling requires ~10µs to settle. The receiver signal path is ready ~10µs after a low-to-high transition on RX_ON.

Transmit Mode

Transmit mode is enabled by driving the digital inputs SHDNB high, RX_ON low, and TX_ON high. In transmit mode, all transmit circuit blocks are powered on and all VCO, PLL, and autotuner circuits are powered on. None of the receive path blocks are active in this mode. Although the transmitter blocks turn on quickly, the baseband DC offset calibration requires ~2.2µs to complete. In addition, the Tx driver amplifier is ramped from the low-gain state (minimum RF output) to high-gain state (peak RF output) over the next 1µs to 2µs. Also, the LO takes a few microseconds after TX_ON rises to resettle. The transmit signal path is ready ~5µs after a low-to-high transition on TX_ON.

Programmable Registers

The MAX2822 contains programmable registers to control various modes of operation for the major circuit blocks. The registers can be programmed through the 3-wire SPI/QSPI/MICROWIRE-compatible serial port. The MAX2822 includes five programmable registers:

1) Block-enable register
2) Synthesizer register
3) Channel frequency register
4) Receiver settings register
5) Transmitter settings register

Each register consists of 16 bits. The four most significant bits (MSBs) are the register's address. The twelve least significant bits (LSBs) are used for register data. Table 2 summarizes the register configuration. A detailed description of each register is provided in Tables 4–8.

Data bits are shifted in the MSB first. The data sent to the MAX2822, in 16-bit words, is framed by CSB. When CSB is low, the clock is active and data is shifted with the rising edge of the clock. When CSB transitions to high, the shift register is latched into the register selected by the contents of the address bits. Only the last 16 bits shifted into the MAX2822 are retained in the shift register. No check is made on the number of clock pulses. Figure 1 documents the serial interface timing for the MAX2822.

Power-Up Default States

The MAX2822 provides power-up loading of default states for each of the registers. The states are loaded on a VCC_DIG supply voltage transition from 0V to V_{CC}. The default values are retained until reprogrammed through the serial interface or the power-supply voltage is taken to 0V. The default state of each register is described in Table 3. **Note:** Putting the IC in shutdown mode does not change the contents of the programming registers.

Block-Enable Register

The block-enable register permits individual control of the enable state for each major circuit block in the MAX2822. The actual enable condition of the circuit block is a logical function of the block-enable bit setting and other control input states. Table 4 documents the logical definition of state for each major circuit block.

Synthesizer Register

The synthesizer register (SYNTH) controls the reference frequency divider and charge-pump current of the PLL. See Table 5 for a description of the bit settings.

Channel Frequency Register

The channel frequency register (CHANNEL) sets the RF carrier frequency for the MAX2822. The channel is programmed as a number from 0 to 99. The actual frequency is 2400 + channel in MHz. The default setting is 37 for 2437MHz. See Table 6 for a description of the bit settings.

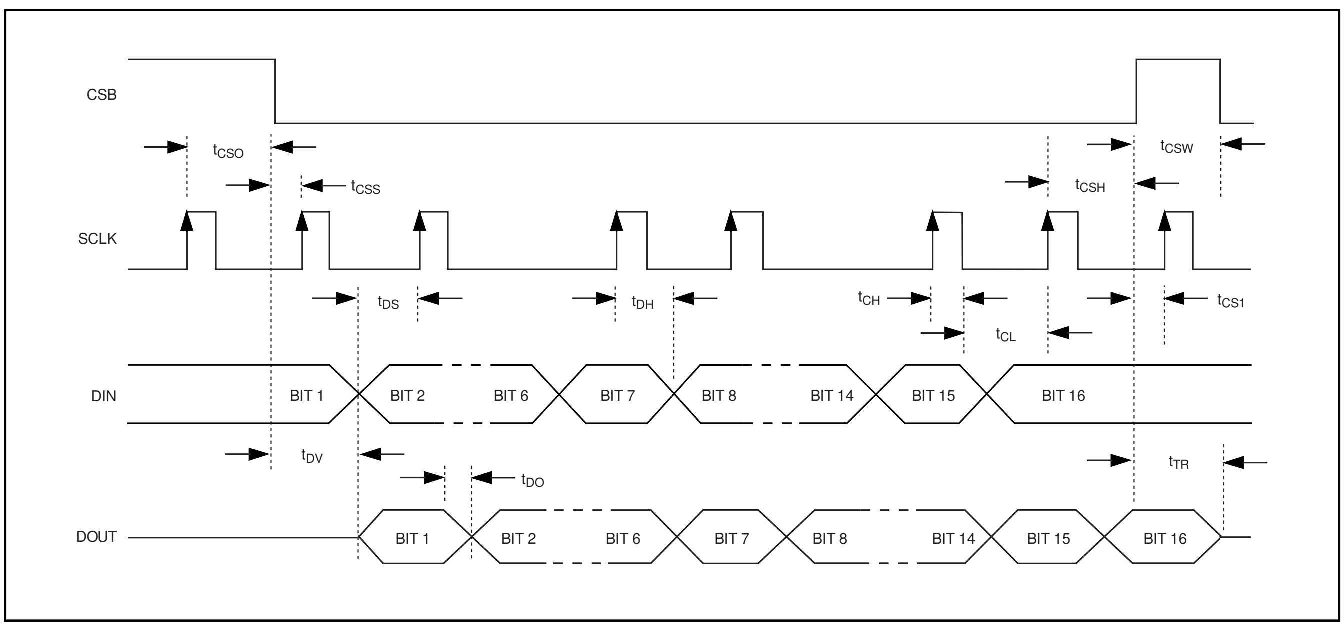


Figure 1. MAX2822 Serial Interface Timing Diagram

Receiver Settings Register

The receiver settings register (RECEIVE) controls the receive filter -3dB corner frequency and VGA DC offset nulling parameters. The defaults are intended to provide proper operation. However, the filter frequency and detector can be modified if desired. Do not reprogram VGA DC offset nulling parameters. These settings were optimized during development. See Table 7 for a description of the bit settings.

Transmitter Settings Register

The transmitter settings register (TRANSMIT) provides a 6-bit digital control of the PA bias and 1-bit enable for the transmit power detector. Bits D0:D3 control the PA output stage bias current (0000 lowest, 1111 highest) and PA driver stage bias current (00 lowest, 11 highest). The appropriate values vs. target output power are given in Table 9. The detector enable bit allows independent turn-on of the detector for testing purposes.

Table 2. Programming Register Definition Summary

REGISTER NAME	4 ADDRESS BITS				12 DATA BITS											
	A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	LSB
ENABLE	0	0	0	1	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
SYNTH	0	0	1	0	X	X	X	X	0	1	0	0	0	0	0	R0
CHANNEL	0	0	1	1	X	X	X	X	X	CF6	CF5	CF4	CF3	CF2	CF1	CF0
RECEIVE	0	1	0	0	2C2	2C1	2C0	1C2	1C1	1C0	DL1	DL0	SF	BW2	BW1	BW0
TRANSMIT	0	1	0	1	X	X	X	X	X	DE	DR1	DR0	PA3	PA2	PA1	PA0

X = Don't care.

Table 3. Register Power-Up Defaults States

REGISTER	ADDRESS	DEFAULT	FUNCTION
ENABLE	0001	0000 0001 1110	Block-Enable Control Settings (E)
SYNTH	0010	0000 0100 0000	Synthesizer Settings: • Reference frequency (R)
CHANNEL	0011	0000 0010 0101	Channel frequency settings (CF)
RECEIVE	0100	1111 1101 0010	Receiver Settings: • -3dB lowpass filter bandwidth (BW) • Detector midpoint level (DL)
TRANSMIT	0101	0000 0010 1101	Transmit Settings: • PA bias (PA) • PA driver bias (D) • PA driver enable (DE)

Table 4. Block-Enable Register (ENABLE)

ADDRESS	DATA BIT	CONTENT	DEFAULT	DESCRIPTION AND LOGICAL DEFINITION
0 0 0 1	D11	E(11)	0	Reserved
	D10	E(10)	0	PA Bias-Control Enable (PAB_EN) PAB_EN = SHDNB • (E(10) + TX_ON)
	D9	E(9)	0	Transmit Baseband Filters Enable (TXFLT_EN) TXFLT_EN = SHDNB • (E(9) + TX_ON)
	D8	E(8)	0	Tx Upconverter + VGA + Driver Amp Enable (TXUVD_EN) TXUVD_EN = SHDNB • (E(8) + TX_ON)
	D7	E(7)	0	Reserved
	D6	E(6)	0	Rx Downconverter + Filters + AGC Amps Enable (RXDFA_EN) RXDFA_EN = SHDNB • (E(6) + RX_ON)
	D5	E(5)	0	Receive LNA Enable (RXLNA_EN) RXLNA_EN = SHDNB • (E(5) + RX_ON)
	D4	E(4)	1	Autotuner Enable (AT_EN) AT_EN = SHDNB • (E(4) + RX_ON + TX_ON)
	D3	E(3)	1	PLL Charge-Pump Enable (CP_EN) CP_EN = SHDNB • E(3)
	D2	E(2)	1	PLL Enable (PLL_EN) PLL_EN = SHDNB • E(2)
	D1	E(1)	1	VCO Enable (VCO_EN) VCO_EN = SHDNB • E(1)
	D0	E(0)	0	Reserved

Table 5. Synthesizer Settings Register (SYNTH)

ADDRESS	DATA BIT	CONTENT	DEFAULT	DESCRIPTION
0 0 1 0	D11:D8	X	0000	Reserved
	D7	—	0	Must be 0 for proper operation
	D6	—	1	Must be 1 for proper operation
	D5:D0	R(5:0)	000000	Reference Frequency Divider: • 000000 = 22MHz • 000001 = 44MHz

Table 6. Channel Frequency Register (CHANNEL)

ADDRESS	DATA BIT	CONTENT	DEFAULT	DESCRIPTION
0 0 1 1	D11:D7	X	00000	Reserved
	D6:D0	CF(6:0)	0100101	Channel Frequency Select: f_{LO} = (2400 + CF(6:0))MHz • 0000000 = 2400MHz • 0000001 = 2401MHz • ………… • 1100010 = 2498MHz • 1100011 = 2499MHz

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Table 7. Receiver Settings Register (RECEIVE)

ADDRESS	DATA BIT	CONTENT	DEFAULT	DESCRIPTION
0 1 0 0	D11:D4	—	11111111	Must be 11111111 for proper operation
	D3	—	0	Must be 0 for proper operation
	D2:D0	BW(2:0)	010	Receive Filter -3dB Frequency Select (frequencies are approximate): • 000 = 8.5MHz • 001 = 8.0MHz • 010 = 7.5MHz • 011 = 7.0MHz • 100 = 6.5MHz • 101 = 6.0MHz

Table 8. Transmit Settings Register (TRANSMIT)

ADDRESS	DATA BIT	CONTENT	DEFAULT	DESCRIPTION
0 1 0 1	D11:D7	X	X	Reserved
	D6	DE	0	Transmit Power-Detector Enable
	D5:D4	D(1:0)	10	PA Predriver Bias: • 11 = Highest predriver bias • ………… • 00 = Lowest predriver bias
	D3:D0	PA(3:0)	1101	PA Bias Select: • 1111 = Highest PA bias • ………… • 0000 = Lowest PA bias

Applications Information

RF I/O and Tx/Rx Switching

The MAX2822 completely integrates the power amplifier, low-noise amplifier, transmit/receive (Tx/Rx) switch, as well as all matching components, to allow direct connection to the antenna through a balun or combination balun/filter. This single RF interface (RFP and RFN) is internally matched to form a 100Ω balanced port—no additional components are required to impedance-match the I/O. Most applications employ a 100Ω balanced to 50Ω single-ended RF bandpass filter between the RF port and the antenna.

Receive Path

LNA

Given the LNA input is internally matched to 100Ω differential, it is important that the differential pair from RFP/RFN to the RF BPF be an identical pair of transmission lines to present a 100Ω differential impedance to the balun. Identical line layout on the differential input traces is important in maintaining good IP2 performance and RF common-mode noise rejection.

The MAX2822 has two LNA gain modes that are digitally controlled by the logic signal applied to RF_GAIN. RF_GAIN high enables the high-gain mode, and RF_GAIN low enables the low-gain mode. The LNA gain step is nominally 32dB. In most applications, RF_GAIN is connected directly to a CMOS output of the baseband IC, and the baseband IC controls the state of the LNA gain based on the detected signal amplitude.

Receiver Baseband Lowpass Filtering

The MAX2822 on-chip receive lowpass filters provide the steep filtering necessary to attenuate the out-of-band (> 11MHz) interfering signals to sufficiently low levels to preserve receiver sensitivity. The filter frequency response is precisely controlled on-chip and does not require user adjustment. However, a provision is made to permit the -3dB corner frequency and entire response to be slightly shifted up or down in frequency. This is intended to offer some flexibility in trading off adjacent channel rejection vs. passband distortion. The filter -3dB frequency is programmed through the serial interface. The specific bit setting vs. -3dB frequency is shown in Table 7. The typical receive baseband filter gain vs. frequency profile is shown in the *Typical Operating Characteristics*. Default filter settings are optimal (-3dB corner at 7.5MHz)—this provides the best trade-off between noise filtering and baseband distortion to obtain best receive sensitivity. No user adjustment is required.

Receive Gain Control

The MAX2822 receive path gain is varied through an external voltage applied to the pin RX_AGC. Maximum gain is at V_{RX_AGC} = 0V and minimum gain is at V_{RX_AGC} = 2V. The RX_AGC input is a high-impedance analog input designed for direct connection to the RX_AGC DAC output of the baseband IC. The gain-control range, which is continuously variable, is typically 70dB. The gain-control characteristic is shown in the *Typical Operating Characteristics* Receiver Voltage Gain vs. Gain-Control Voltage graph and again as a full-page plot in Figure 2.

Some local noise filtering through a simple RC network at the input is permissible. However, the time constant of this network should be kept sufficiently low to not limit the desired response time of the Rx gain-control function.

Receiver Baseband Amplifier Outputs

The MAX2822 receiver baseband outputs (RX_BBIP, RX_BBIN, RX_BBQP, and RX_BBQN) are differential low-impedance buffer outputs. The outputs are designed to be directly connected (DC-coupled) to the in-phase (I) and quadrature-phase (Q) ADC inputs of the baseband IC. The Rx I/Q outputs are internally biased to +1.2V common-mode voltage. The outputs are capable of driving loads up to 5kΩ || 5pF with the full bandwidth baseband signals at a differential amplitude of $500mV_{P-P}$.

Proper board layout is essential to maintain good balance between I/Q traces. This provides good quadrature phase accuracy.

Transmit Path

Transmitter Baseband Inputs

The MAX2822 transmitter baseband inputs (TX_BBIP, TX_BBIN, TX_BBQP, and TX_BBQN) are high-impedance differential analog inputs. The inputs are designed to be directly connected (DC-coupled) to the in-phase (I) and quadrature-phase (Q) DAC outputs of the baseband IC. The inputs must be externally biased to +1.2V common-mode voltage. Typically, the DAC outputs are current outputs with external resistor loads to ground. I and Q are driven by a $400mV_{P-P}$ (nominal) differential baseband signal.

Proper board layout is essential to maintain good balance between I/Q traces. This provides good quadrature phase accuracy by maintaining equal parasitic capacitance on the lines. In addition, it is important not to expose the Tx I/Q circuit board traces going from the digital baseband IC to the MAX2822. The lines should be shielded on an inner layer to prevent coupling of RF to these Tx I/Q inputs and possible envelope demodulation of the RF signal.

Transmit Path Baseband Lowpass Filtering

The MAX2822 on-chip transmit lowpass filters provide the filtering necessary to attenuate the unwanted higher-frequency spurious signal content that arises from the DAC clock feedthrough and sampling images. In addition, the filter provides additional attenuation of the second sidelobe of signal spectrum. The filter frequency response is set on-chip. No user adjustment or programming is required. The Typical Gain vs. Frequency profile is shown in the *Typical Operating Characteristics*.

Transmitter DC Offset Calibration

In a zero-IF system, the DC offset of the Tx baseband signal path must be reduced to as near zero as possible to minimize LO leakage at the RF output. Given that the amplifier stages, baseband filters, and Tx DAC possess some finite DC offset that is too large for the required LO leakage specification, it is necessary to null the DC offset. The MAX2822 accomplishes this through an on-chip calibration sequence. During this sequence, the net Tx baseband signal path offsets are sampled and cancelled in the baseband amplifiers. This calibration occurs in the first ~2.2µs after TX_ON is taken high. The calibration corrects for any DC offset from the DAC, but this DC offset must not change after this cal sequence. Be sure the DAC outputs are set to zero state before taking TX_ON high.

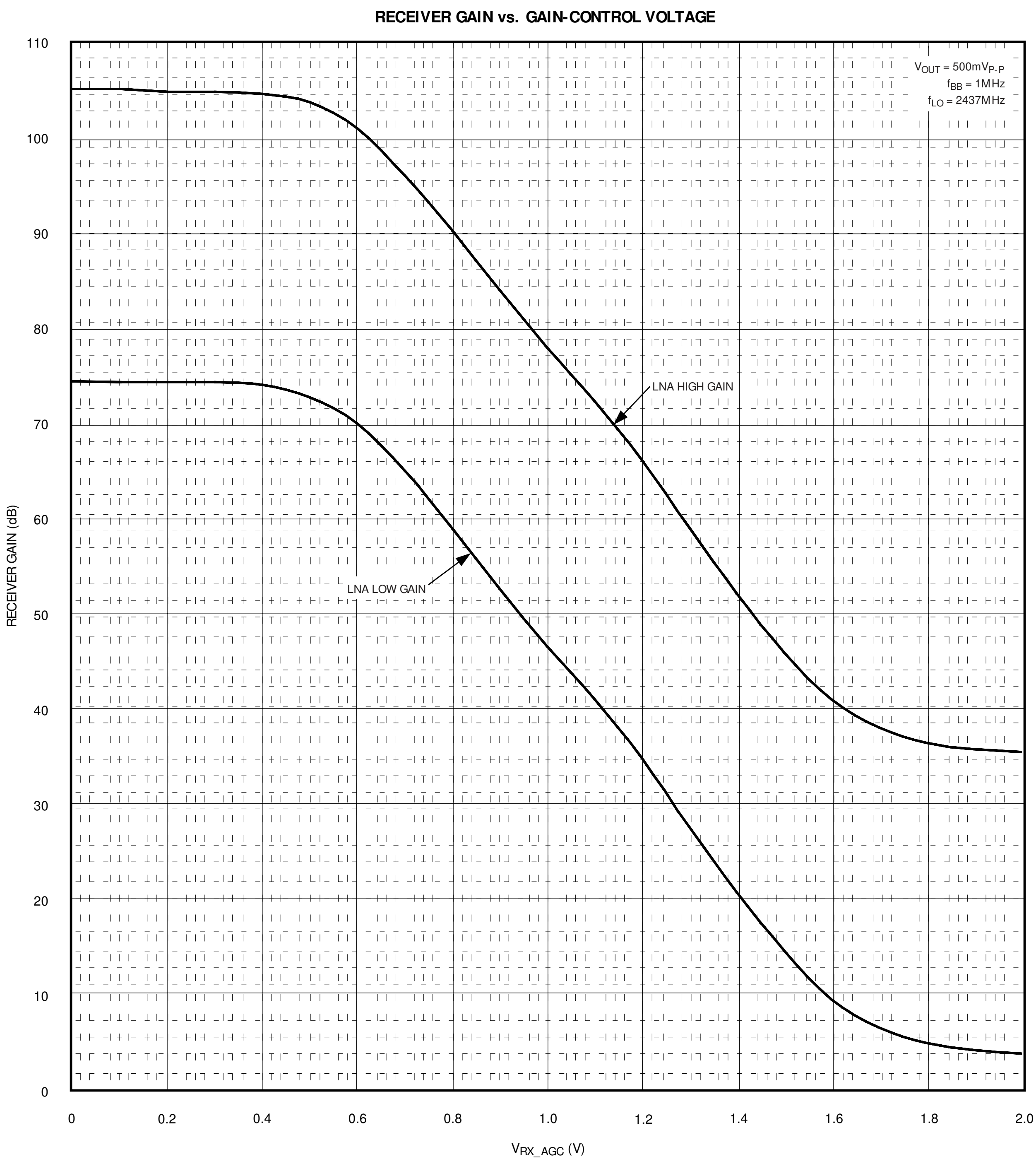


Figure 2. Receiver Gain vs. V_{RX_AGC}

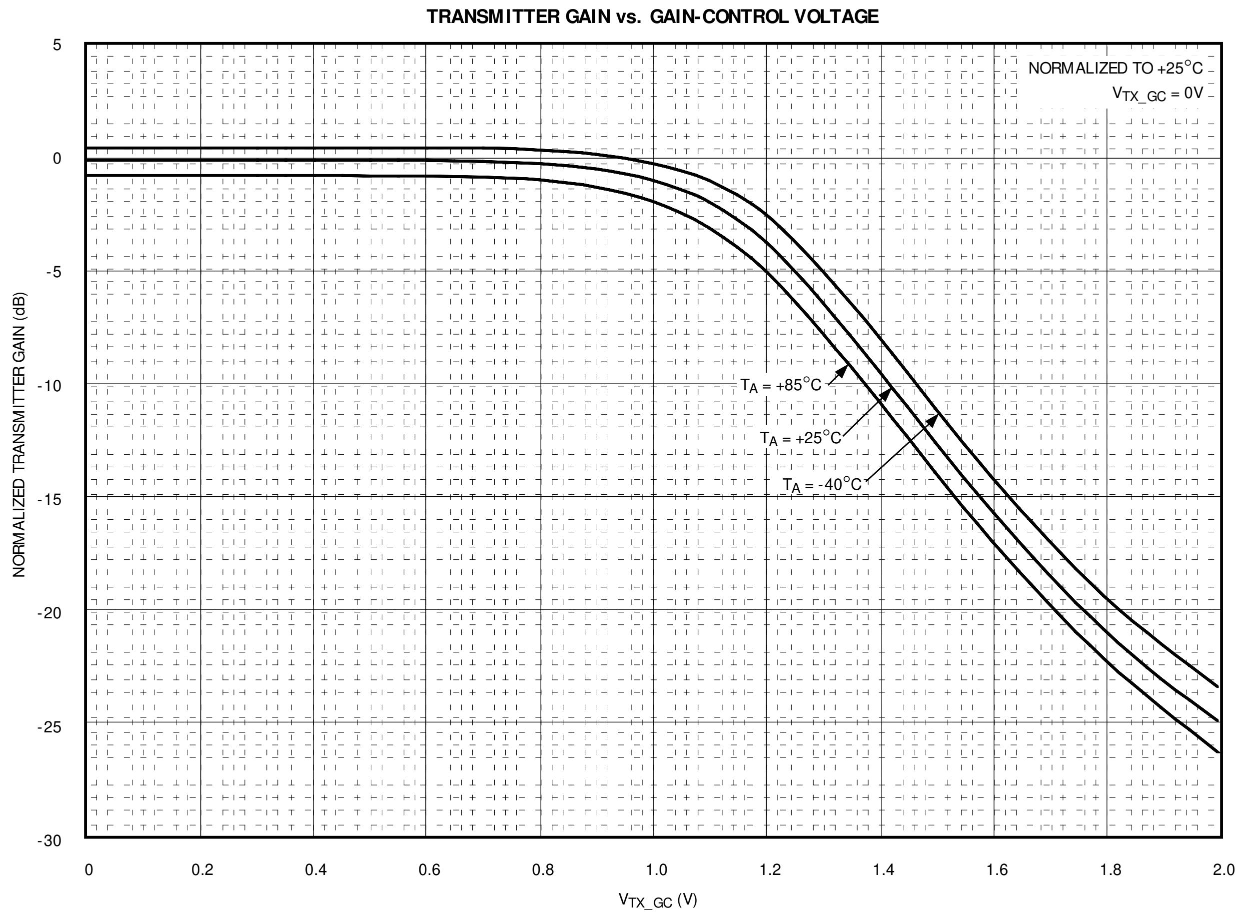


Figure 3. Transmitter Gain vs. V_{TX_GC}

The DC offset circuitry uses a sample-and-hold technique to accomplish this DC offset nulling. Over time (many seconds), the sample-and-hold storage cap slowly discharges, causing the DC value at the Tx BB to slowly increase, and the LO level in the RF output to slowly increase. This can be seen on the bench during evaluation, when the transceiver is left in Tx mode for more than 30 to 60 seconds. Even under worst-case conditions, however, the DC null value changes very little during the longest 802.11b Tx burst of 20ms—LO suppression in 802.11b applications always remains around the -30dBc typical level specified in the *Electrical Characteristics* table.

Transmit Gain Control

The transmit gain-control input provides a direct analog control over the transmit path gain. The transmit gain of the MAX2822 is controlled by an external voltage at pin TX_GC. The typical gain-control characteristic is provided in the *Typical Operating Characteristics* Transmitter Gain Control vs. Gain-Control Voltage graph and again as a full-page plot in Figure 3. The input is a high-impedance analog input designed to directly connect to the DAC output of the baseband IC. Some local noise filtering through a simple RC network at the input is permissible. However, the time constant of this network should be kept sufficiently low so the desired response time of the Tx gain-control function is not limited.

During the Tx turn-on sequence, internally the gain is set at the minimum while the Tx baseband offset calibration is taking place. The RF output is effectively blanked for the first 2.2µs after TX_ON is taken high. After 2.2µs, the blanking is released, and the gain-control amplifier ramps to the gain set by the external voltage applied to the TX_GC input.

Power Amplifier

The MAX2822 provides two programmable analog current sources for internally biasing the on-chip RF power amplifier and the PA predriver. The PA predriver current is controlled by two bits in the TRANSMIT control register (TRANSMIT:D5, D4). The value of the PA bias current is determined by four bits (TRANSMIT:D3–D0). This programmability permits optimizing of the power amplifier idle current based on the output power level of the PA. See Table 8 for a description of the TRANSMIT control bits, and the corresponding PA predriver and PA bias currents. These two bias current settings significantly affect both efficiency and linearity. They should be chosen based on the target output power for the application. Table 9 shows the recommended register settings for three target output powers.

Synthesizer

Channel Frequency and Reference Frequency

The synthesizer/PLL channel frequency and reference settings establish the divider/counter settings in the integer-N synthesizer of the MAX2822. Both the channel frequency and reference divider are programmable through the serial interface. The channel frequency is programmed as a channel number 0 to 99 to set the carrier frequency to 2400MHz to 2499MHz (LO frequency = channel + 2400). The reference divider is programmable to allow for 22MHz or 44MHz reference oscillators. These settings are intended to cover only the required 802.11b channel spacing and the two typical crystal oscillator options used in the radios.

Reference Oscillator Input

The reference oscillator inputs ROSCP and ROSCN are high-impedance analog inputs. They are designed to be connected to the reference oscillator output through a coupling capacitor. The input amplitude can range from 200mV$_{P-P}$ to 500mV$_{P-P}$; therefore, in the case of a reference oscillator with a CMOS output, the signal must be attenuated before being applied to the ROSC inputs. The signal can be attenuated with a resistor- or capacitor-divider network.

Loop Filter

The PLL uses a classical charge pump into an external loop filter (C-RC) in which the filter output connects to the voltage tuning input of the VCO. This simple third-order lowpass loop filter closes the loop around the synthesizer. The *Typical Application Circuit* shows the loop filter elements around the MAX2822. The capacitor and resistor values are set to provide the loop bandwidth required to achieve the desired lock time while also maintaining loop stability. Refer to the MAX2822

Table 9. Suggested PA and PA Driver Bias Current Settings

TARGET OUTPUT POWER (dBm)	PA DRIVER BIAS SETTING (TRANSMIT: D5, D4)	PA BIAS SETTING (TRANSMIT: D3–D0)
+3	00	0011
+12	01	0111
+17	10	1101

EV kit schematic for component values. A 45kHz loop bandwidth is recommended to ensure the loop settles quickly enough to achieve 5µs Tx turnaround time and 10µs Rx turnaround time. This is the loop filter on the EV kit. Narrowing the loop bandwidth increases the settling time and results in unacceptable Tx/Rx turnaround time performance.

PC Board Layout

Careful PC board layout is mandatory for any radio to meet its specifications. General rules for RF layout apply: keep differential pairs close together, keep all RF traces as short as possible, keep RF bypassing as close to the IC as possible, provide a separate filtered supply line from a large central filter capacitor for each V_{CC} pin (star supply bypassing topology), and have each ground pin use its own via to the ground plane—do not connect ground pins directly to the ground slug on the IC. In addition, below is a list of more specific layout issues to keep in mind for the MAX2822:

- RF I/O: Keep RF differential pair from the IC to the balun/filter electrically and environmentally symmetrical. That is, shape the top layer ground equally on either side of the traces, and place the RF decoupling caps for the nearby RF supplies in a symmetrical fashion. This minimizes second-order distortion of the signal on the differential pair.
- RBIAS: This external resistor sets the bias for the RF section of the transceiver, and this pin is connected *directly* to the bias section. The network connected to this port must look high impedance to RF, so do not place any RF filtering here—use only a 1% or 2% 12kΩ resistor, as specified in the *Typical Application Circuit*. Place this resistor as close to the IC as possible on the top layer of the PC board.
- GND_DIG: Use a via to connect this digital ground to the main PC board ground plane. The small inductance of the trace and the via helps to filter out the noise from the digital interface, and helps keep the main system ground clean. It is very important not to connect this directly to the IC ground slug, or directly to any other ground pins, which allows noise from the digital section to couple into sensitive sections of the radio.
- PLL section (CP_OUT, GND_CP, GND_VCO, TUNE): The capacitors directly at the output of the PLL's charge pump need to have their ground return connected as close to the charge pump's ground as possible, and as isolated from the VCO's ground as possible. Create separate vias to the ground plane for each of the two grounds (GND_CP and GND_VCO). Referring to the *Typical Application Circuit*, connect the ground side of C30 and C52 to the ground path for GND_CP, and connect the ground side of C31 to the ground path for GND_VCO. Keeping the charge-pump return currents from bouncing the VCO's ground minimizes the LO comparison frequency spurs.
- BYP: This bypass capacitor is directly connected to the VCO bias circuitry—it is used to filter out noise within the loop bandwidth of the PLL (about 50kHz). The value for this capacitor is critical—be sure to use the 2000pF capacitor specified in the *Typical Application Circuit*. Keep this cap as close to the IC as possible, since noise pickup on this trace couples directly into the VCO bias and degrade phase noise.

Supply and Regulation

The typical application circuit for the MAX2822 employs two low-dropout linear regulators (LDOs)—one supplies the internal VCO, and the other supplies everything else (see the *Pin Description* table for details on supply pin names, numbers, and functions). Supplying the VCO from a dedicated LDO minimizes noise pickup by the VCO that can degrade phase noise and produce spurs. The VCO only draws 10mA, so power dissipation is not an issue. Choose a small, low-noise, high-PSRR LDO like the MAX8510. This LDO comes in a tiny 5-pin SC70 package and is available in many preset output voltages in the 2.7V to 3.0V range.

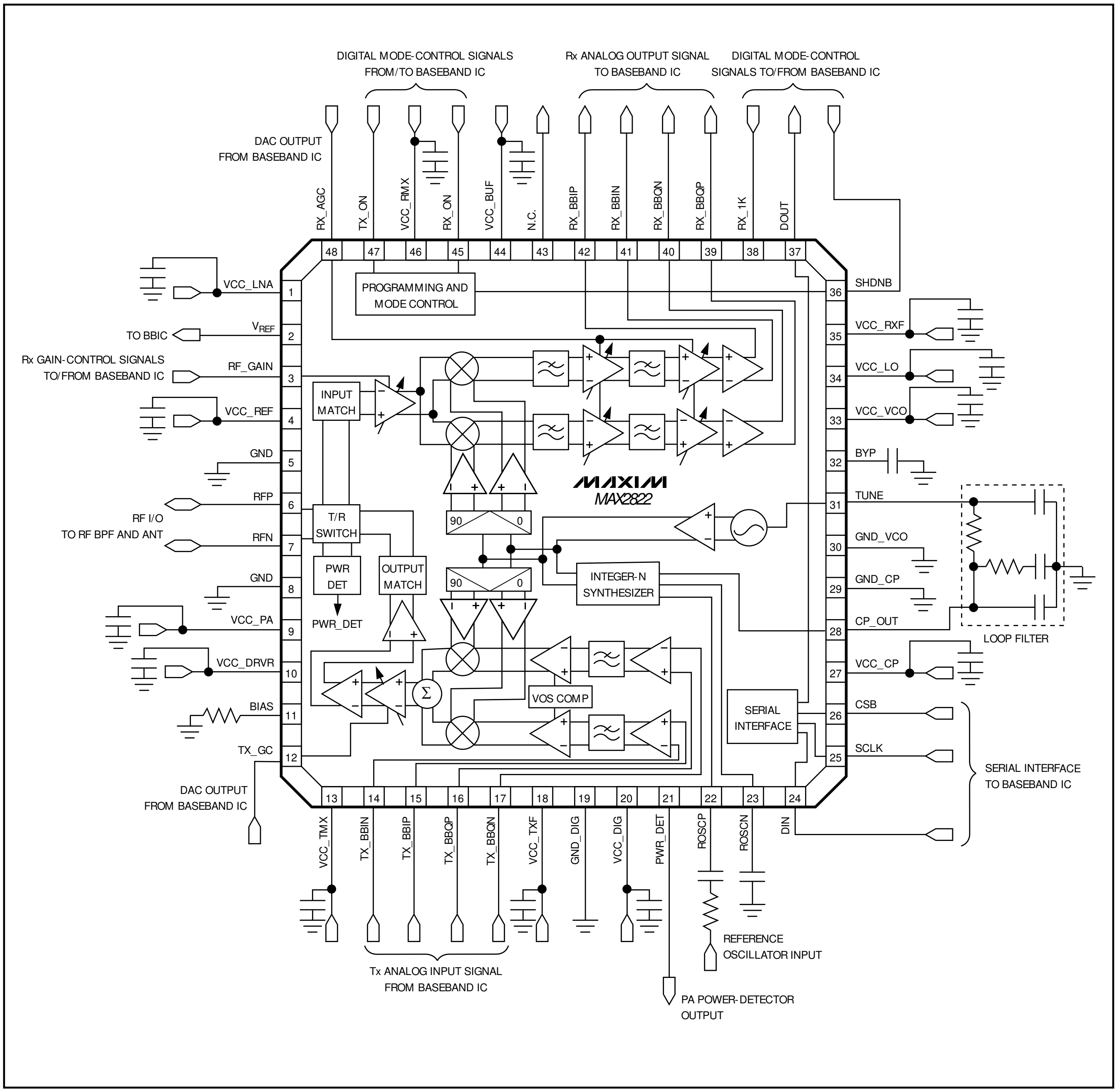
Having the VCO and the rest of the IC supplied from different voltages is acceptable. Therefore, if the MAX2822 main supply is 2.7V, but the application already has a low-noise, 3.0V supply available, simply run the VCO from this 3.0V supply—there is no need for another dedicated 2.7V supply for the VCO.

Switching power supplies should not be used to directly power any RF transceiver; the spurious content of their outputs often falls in the middle of the system's baseband spectrum (50kHz to 11MHz). This can couple into the Tx path and degrade the output spectrum, and can couple into the Rx path and degrade sensitivity and BER.

When laying out the supply lines for the IC, always use a star bypassing topology. Have a large (10µF) low-ESR capacitor at the main supply connection point, and run dedicated traces to each of the supply pins (there are about ten in total). Each supply pin should have a pair of smaller decoupling caps (10nF and 100pF work well). It is especially important to isolate the supplies for the LNA bias (VCC_LNA) and the Rx baseband filter bias (VCC_BUF).

Also be sure to use local RF decoupling on the logic lines. Proper decoupling minimizes noise pickup and coupling.

Typical Application Circuit

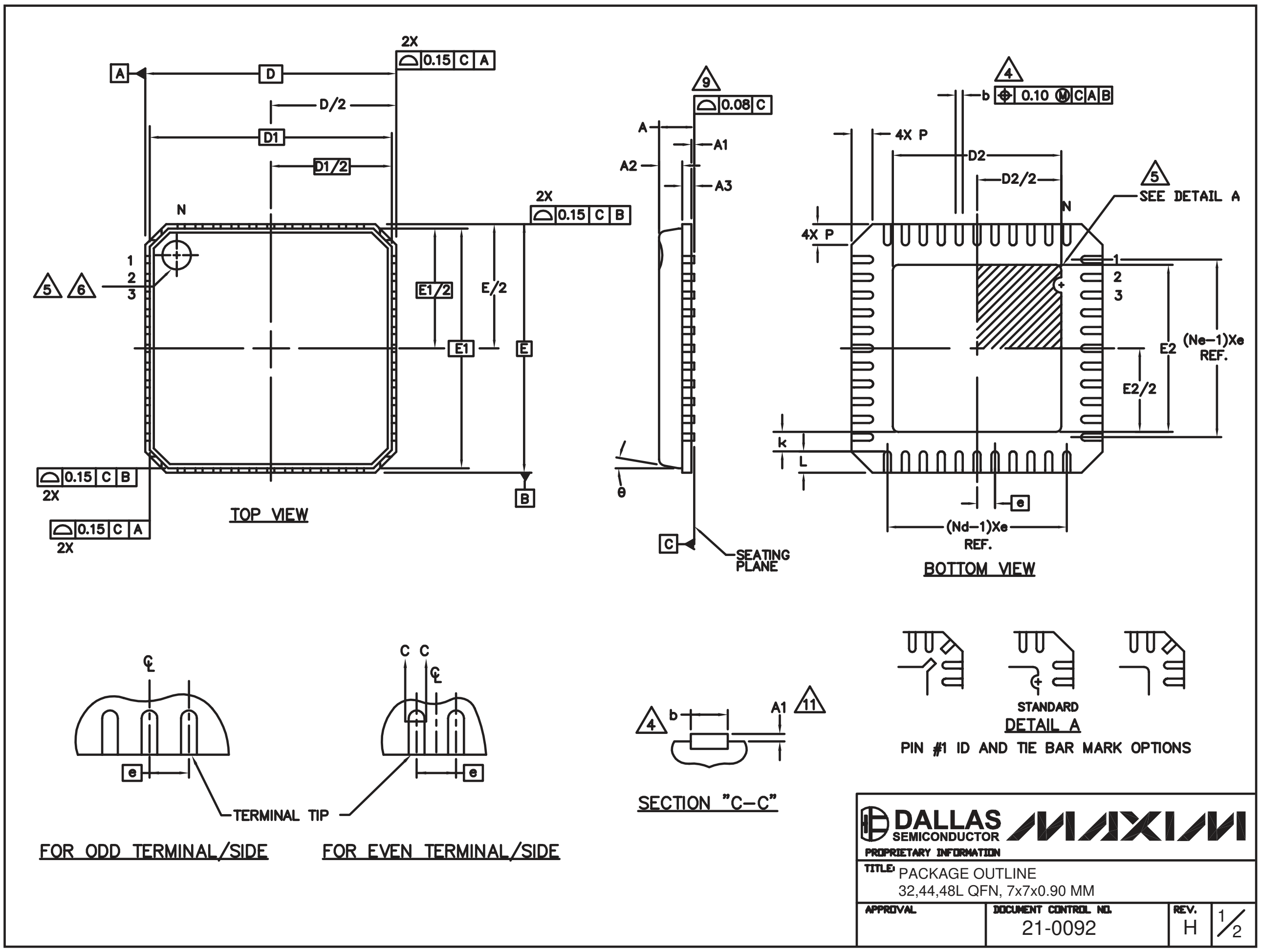


Chip Information

TRANSISTOR COUNT: 16,097

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



2.4GHz 802.11b Zero-IF Transceiver with Integrated PA and Tx/Rx Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG	32L 7x7			44L 7x7			48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF		
b	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
D1	6.75 BSC			6.75 BSC			6.75 BSC		
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E1	6.75 BSC			6.75 BSC			6.75 BSC		
e	0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	-	-	0.25	-	-	0.25	-	-
L	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	32			44			48		
Nd	8			11			12		
Ne	8			11			12		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
U	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G3277-2	4.55	4.70	4.85	4.55	4.70	4.85
G4477-1	3.65	3.80	3.95	3.65	3.80	3.95
G4477-2	4.55	4.70	4.85	4.55	4.70	4.85
G4477-3	3.15	3.30	3.45	3.15	3.30	3.45
G4877-1	4.95	5.10	5.25	4.95	5.10	5.25
G4877-2	5.45	5.60	5.75	5.45	5.60	5.75

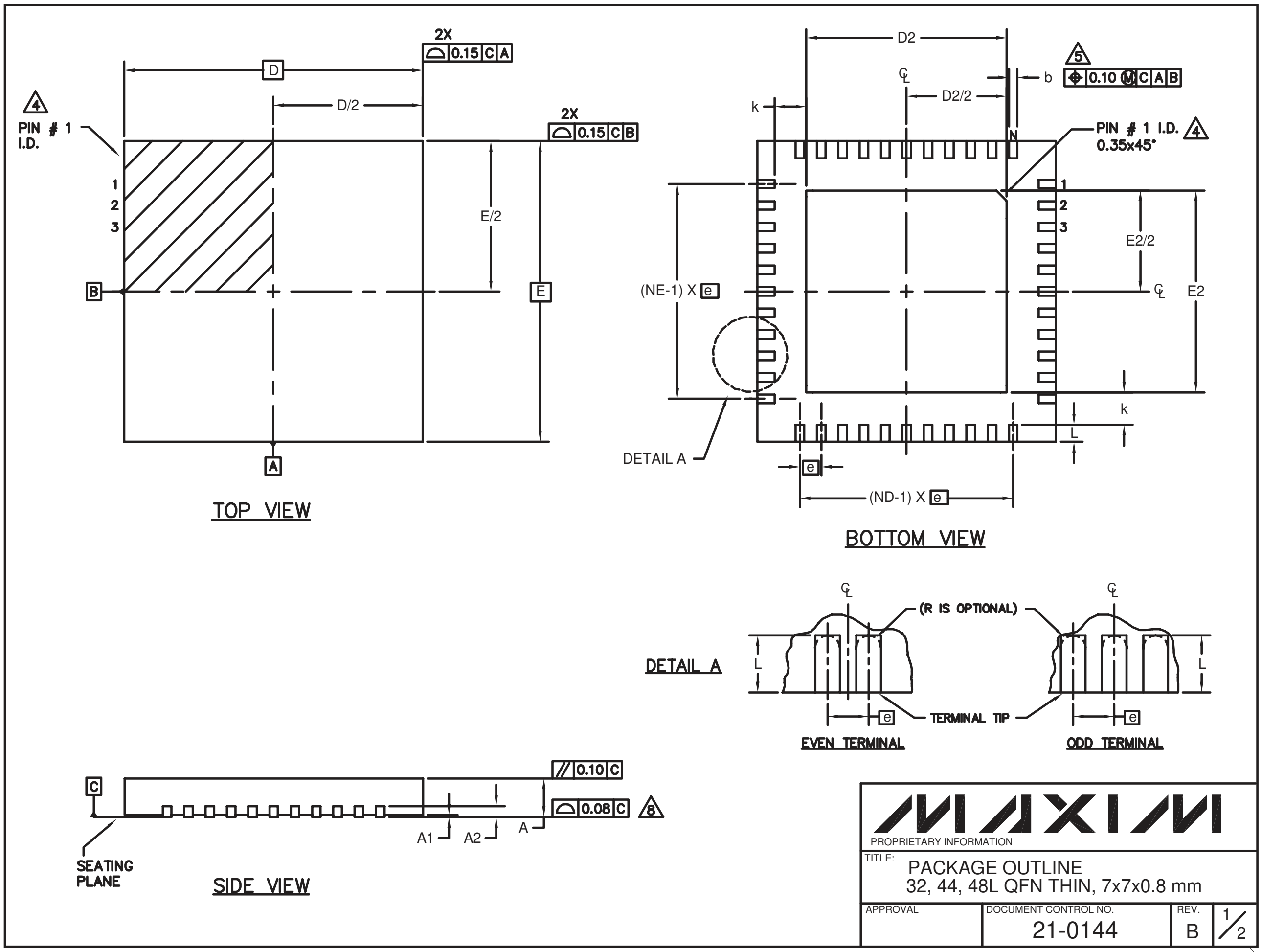
NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.08mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220 EXCEPT DIMENSION "b" MINIMUM.
11. APPLY ONLY FOR TERMINAL.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION(STEPPED SIDES).

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 32,44,48L QFN, 7x7x0.90 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0092 | REV. H | 2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65
N	32			44			48			44		
ND	8			11			12			10		
NE	8			11			12			12		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-1	-	4.55	4.70	4.85	4.55	4.70	4.85	-
T4477-1	-	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13, 24, 37, 48	4.20	4.30	4.40	4.20	4.30	4.40	-
T4877-2	-	5.45	5.60	5.63	5.45	5.60	5.63	WKKD-2

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M−1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95−1 SPP−012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
32, 44, 48L QFN THIN, 7x7x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	B	2/2