



Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

MAX4484/MAX4486/MAX4487

General Description

The MAX4484/MAX4486/MAX4487 single/dual/quad low-cost general-purpose op amps operate from a single +2.7V to +5.5V supply. The op amps are unity-gain stable with a 7MHz gain-bandwidth product, capable of driving an external 2kΩ load with Rail-to-Rail® output swing. The amplifiers are stable with capacitive loads of up to 100pF. The MAX4484/MAX4486/MAX4487 are specified from -40°C to +125°C, making them suitable for a variety of harsh environments, such as automotive.

The single MAX4484 is available in the ultra-small 5-pin SC70, while the dual MAX4486 is packaged in the space-saving 8-pin SOT23 and μMAX packages. The quad MAX4487 is available in the 14-pin SO and TSSOP packages.

Applications

- Single-Supply Zero-Crossing Detector
- Instruments and Terminals
- Portable Communicators
- Electronic Ignition Modules
- Infrared Receivers for Remote Controls
- Sensor Signal Detection

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

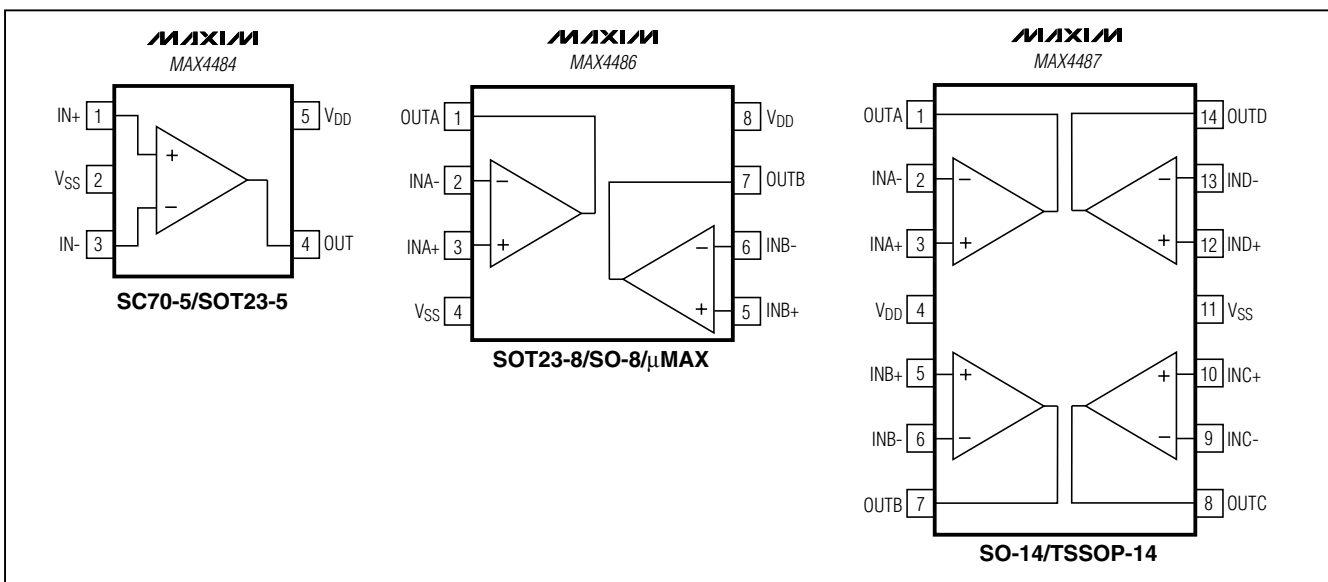
Features

- ◆ 7MHz Unity-Gain Stable Bandwidth
- ◆ Stable for Capacitive Loads up to 100pF
- ◆ +2.7V to +5.5V Single-Supply Voltage Range
- ◆ Ground-Sensing Inputs
- ◆ Outputs Swing Rail-to-Rail
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ 85dB AVOL with 2kΩ Load
- ◆ 0.01% THD with 2kΩ Load
- ◆ Available in Space-Saving Packages
 - 5-Pin SC70 (MAX4484)
 - 8-Pin SOT23 (MAX4486)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX4484AXK-T	-40°C to +125°C	5 SC70-5	ABQ
MAX4484AUK-T	-40°C to +125°C	5 SOT23-5	ADPE
MAX4486AKA-T	-40°C to +125°C	8 SOT23-8	AAEP
MAX4486ASA	-40°C to +125°C	8 SO	—
MAX4486AUA	-40°C to +125°C	8 μMAX	—
MAX4487AUD	-40°C to +125°C	14 TSSOP	—
MAX4487ASD	-40°C to +125°C	14 SO	—

Pin Configurations/Functional Diagrams



Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V _{DD} to V _{SS})-0.3V to +6V	8-Pin μ MAX (derate 4.5mW/°C above +70°C)362mW
All Other Pins(V _{SS} - 0.3V) to (V _{DD} + 0.3V)	14-Pin TSSOP (derate 9.1mW/°C above +70°C)727mW
Output Short-Circuit Duration (OUT shorted to V _{DD} or V _{SS})Continuous	14-Pin SO (derate 8.33mW/°C above +70°C)667mW
Continuous Power Dissipation (T _A = +70°C)		Operating Temperature Range-55°C to +125°C
5-Pin SC70 (derate 3.1mW/°C above +70°C)247mW	Junction Temperature+150°C
5-Pin SOT23 (derate 7.1mW/°C above +70°C)571mW	Storage Temperature Range-65°C to +150°C
8-Pin SOT23 (derate 9.1mW/°C above +70°C)727mW	Lead Temperature (soldering, 10s)+300°C
8-Pin SO (derate 5.88mW/°C above +70°C)471mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—T_A = +25°C

(V_{DD} = +5.0V, V_{SS} = 0, V_{CM} = 0, V_{OUT} = V_{DD}/2, R_L = ∞ to V_{DD}/2, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V _{DD}	Inferred from PSRR test	2.7		5.5	V
Supply Current per Amplifier	I _{DD}	V _{DD} = +2.7V		1.9		mA
		V _{DD} = +5.0V		2.2	3.5	
Input Offset Voltage	V _{OS}	MAX4484		±0.3	±5.0	mV
		MAX4486		±0.3	±7.0	
		MAX4487		±0.3	±9.0	
Input Bias Current	I _B	(Note 1)		±0.1	100	pA
Input Offset Current	I _{OS}	(Note 1)		±0.1	100	pA
Input Resistance	R _{IN}	Differential or common mode		1000		G Ω
Input Common-Mode Voltage Range	V _{CM}	Inferred from CMRR test	V _{SS}		V _{DD} - 1.3	V
Common-Mode Rejection Ratio	CMRR	V _{SS} ≤ V _{CM} ≤ V _{DD} - 1.3V	67	83		dB
Power-Supply Rejection Ratio	PSRR	+2.7V ≤ V _{DD} ≤ +5.5V	70	85		dB
Large-Signal Voltage Gain	A _{VOL}	V _{SS} + 0.3V ≤ V _{OUT} ≤ V _{DD} - 0.3V	R _L = 100k Ω	98		dB
			R _L = 2k Ω	76	85	
Output Voltage High	V _{OH}	Specified as V _{DD} - V _{OH}	R _L = 100k Ω	3		mV
			R _L = 2k Ω	15	50	
Output Voltage Low	V _{OL}	Specified as V _{OL} - V _{SS}	R _L = 100k Ω	1		mV
			R _L = 2k Ω	20	50	
Output Short-Circuit Current	I _{SC}	Sourcing		27		mA
		Sinking		33		
Gain-Bandwidth Product	GBW			7		MHz
Phase Margin	ϕ_m			55		degrees
Gain Margin	G _m			12		dB
Slew Rate	SR			20		V/ μ s
Input Voltage Noise Density	e _n	f = 10kHz		29		nV/ \sqrt Hz
Input Current Noise Density	i _n	f = 10kHz		1		fA/ \sqrt Hz

Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

MAX4484/MAX4486/MAX4487

ELECTRICAL CHARACTERISTICS— $T_A = +25^\circ\text{C}$ (continued)

($V_{DD} = +5.0\text{V}$, $V_{SS} = 0$, $V_{CM} = 0$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$ to $V_{DD}/2$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitive-Load Stability	C_{LOAD}	$A_V = +1V/V$ (Note 1)	100			pF
Power-On Time	t_{ON}			1		μs
Input Capacitance	C_{IN}			2		pF
Total Harmonic Distortion	THD	$f = 10\text{kHz}$, $V_{OUT} = 2V_{p-p}$, $A_V = +1V/V$	$R_L = 100\text{k}\Omega$	0.006		%
			$R_L = 2\text{k}\Omega$	0.01		
Settling Time to 0.01%	t_S	$V_{OUT} = 4V$ step, $A_V = +1V/V$		450		ns

ELECTRICAL CHARACTERISTICS— $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$

($V_{DD} = +5.0\text{V}$, $V_{SS} = 0$, $V_{CM} = 0$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$ to $V_{DD}/2$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Inferred from PSRR test	2.7		5.5	V
Supply Current per Amplifier	I_{DD}				4.0	mA
Input Offset Voltage	V_{OS}	MAX4484			± 8.5	mV
		MAX4486			± 10.0	
		MAX4487			± 11.0	
Input Offset Voltage Drift	TC_{VOS}			± 6		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	(Note 1)			± 100	pA
Input Offset Current	I_{OS}	(Note 1)			± 100	pA
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test	V_{SS}		$V_{DD} - 1.4$	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \leq V_{CM} \leq V_{DD} - 1.4\text{V}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	65		dB
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	62		
Power-Supply Rejection Ratio	PSRR	$+2.7\text{V} \leq V_{DD} \leq +5.5\text{V}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	67		dB
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	64		
Large-Signal Voltage Gain	A_{VOL}	$V_{SS} + 0.3\text{V} \leq V_{OUT} \leq V_{DD} - 0.3\text{V}$, $R_L = 2\text{k}\Omega$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	66		dB
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	62		
Output Voltage High	V_{OH}	$ V_{DD} - V_{OUT} $, $R_L = 2\text{k}\Omega$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	100		mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	100		
Output Voltage Low	V_{OL}	$ V_{OUT} - V_{SS} $, $R_L = 2\text{k}\Omega$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	100		mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	250		

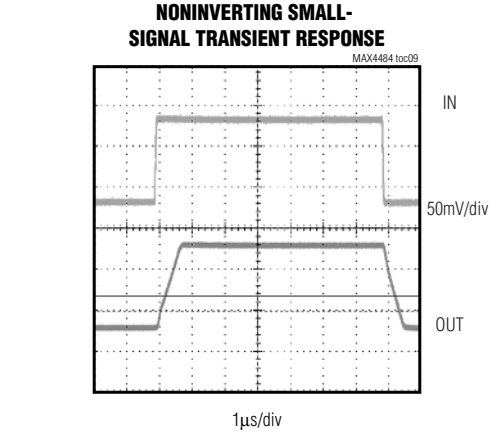
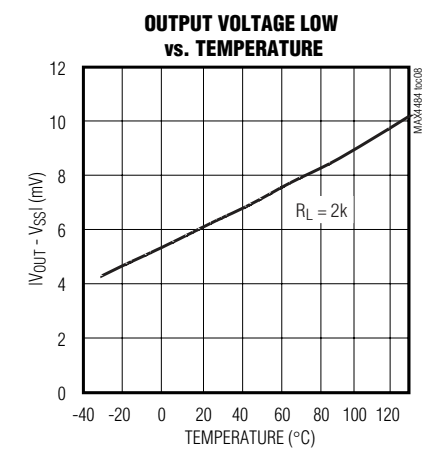
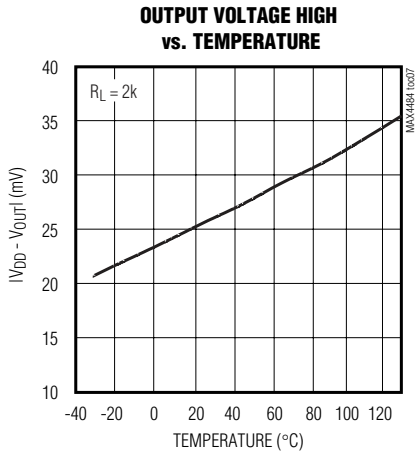
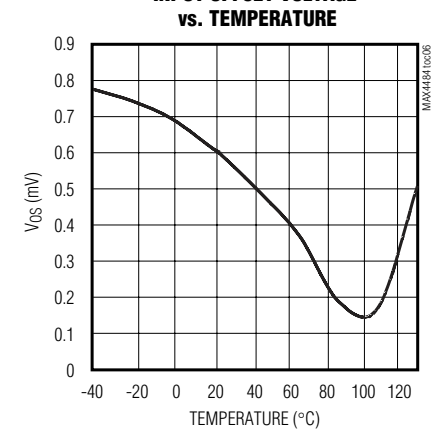
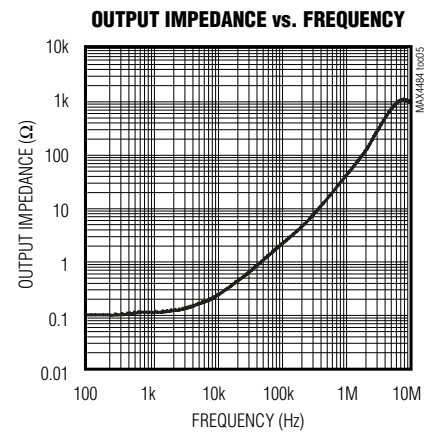
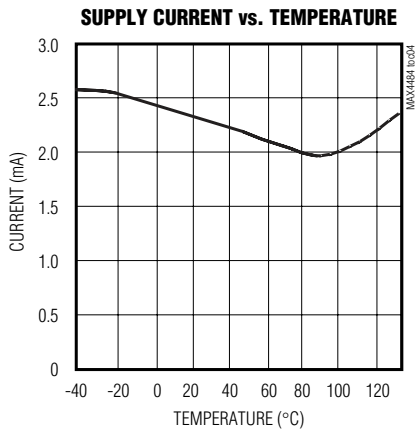
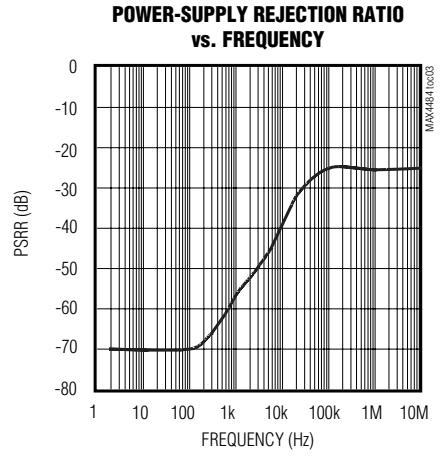
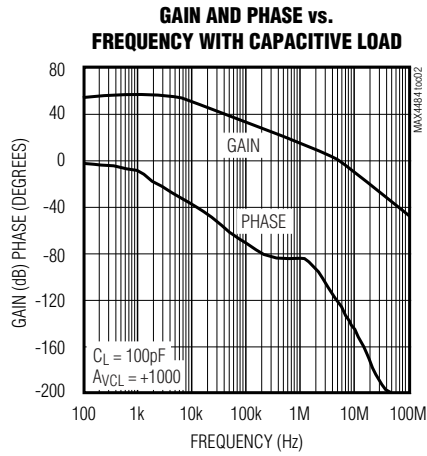
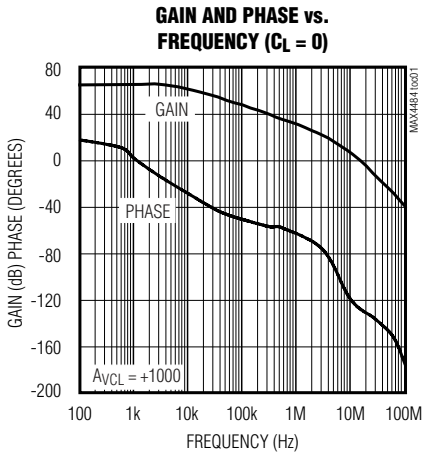
Note 1: Guaranteed by design.

Note 2: Specifications are 100% tested at $T_A = +25^\circ\text{C}$ (exceptions marked). All temperature limits are guaranteed by design.

Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

Typical Operating Characteristics

($V_{DD} = +5V$, $V_{SS} = 0$, $V_{CM} = V_{DD}/2$, $R_L = \infty$ to $V_{DD}/2$, unless otherwise noted.)



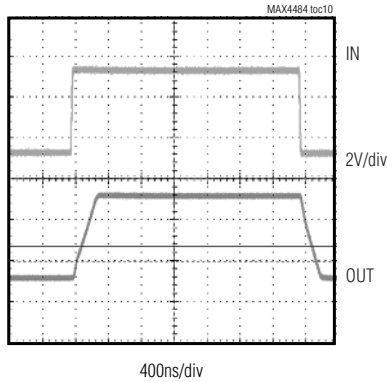
Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

Typical Operating Characteristics (continued)

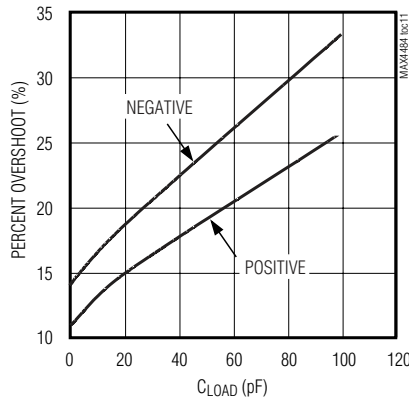
($V_{DD} = +5V$, $V_{SS} = 0$, $V_{CM} = V_{DD}/2$, $R_L = \infty$ to $V_{DD}/2$, unless otherwise noted.)

MAX4484/MAX4486/MAX4487

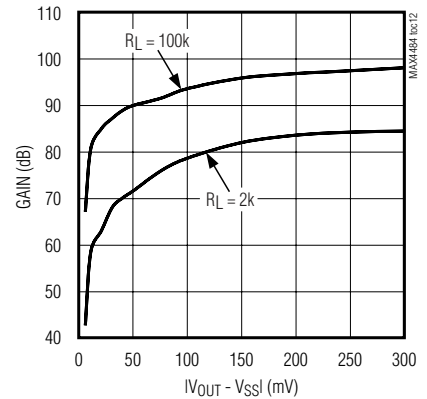
**NONINVERTING LARGE-SIGNAL
TRANSIENT RESPONSE**



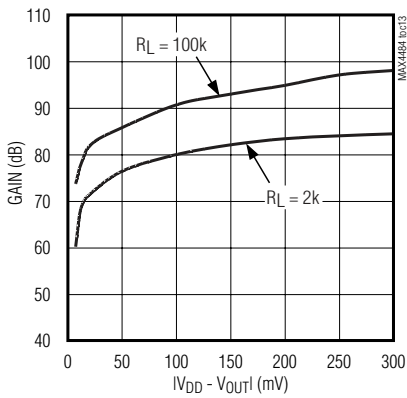
**PERCENT OVERSHOOT
vs. CAPACITIVE LOAD**



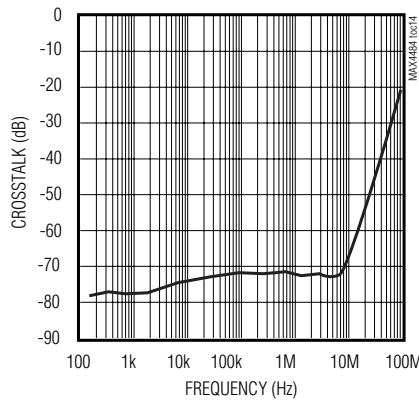
**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE LOW**



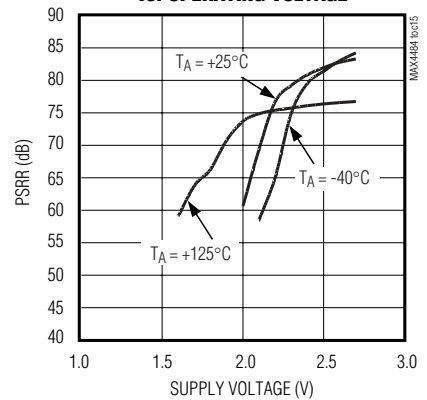
**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE HIGH**



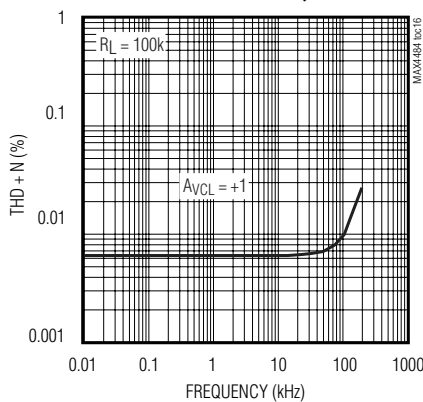
CROSSTALK vs. FREQUENCY



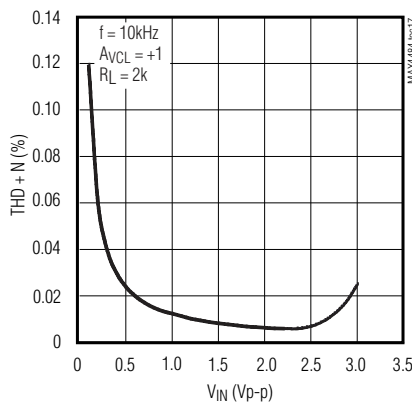
**POWER-SUPPLY REJECTION RATIO
vs. OPERATING VOLTAGE**



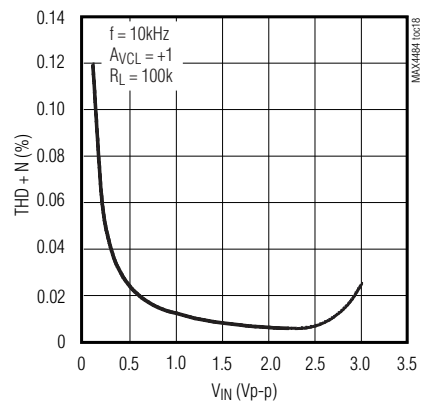
**TOTAL HARMONIC DISTORTION
PLUS NOISE vs. FREQUENCY**



**TOTAL HARMONIC DISTORTION
PLUS NOISE vs. AMPLITUDE**



**TOTAL HARMONIC DISTORTION
PLUS NOISE vs. AMPLITUDE**



Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

Pin Description

PIN			NAME	FUNCTION
MAX4484	MAX4486	MAX4487		
3	—	—	IN-	Inverting Amplifier Input
1	—	—	IN+	Noninverting Amplifier Input
4	—	—	OUT	Amplifier Output
—	2	2	INA-	Inverting Amplifier Input (Channel A)
—	3	3	INA+	Noninverting Amplifier Input (Channel A)
—	1	1	OUTA	Amplifier Output (Channel A)
—	6	6	INB-	Inverting Amplifier Input (Channel B)
—	5	5	INB+	Noninverting Amplifier Input (Channel B)
—	7	7	OUTB	Amplifier Output (Channel B)
—	—	9	INC-	Inverting Amplifier Input (Channel C)
—	—	10	INC+	Noninverting Amplifier Input (Channel C)
—	—	8	OUTC	Amplifier Output (Channel C)
—	—	13	IND-	Inverting Amplifier Input (Channel D)
—	—	12	IND+	Noninverting Amplifier Input (Channel D)
—	—	14	OUTD	Amplifier Output (Channel D)
2	4	11	V _{SS}	Negative Power-Supply Voltage
5	8	4	V _{DD}	Positive Power-Supply Voltage

Detailed Description

Rail-to-Rail Output Stage

The MAX4484/MAX4486/MAX4487 can drive a 2k Ω load and still swing within 50mV of the supply rails. Figure 1 shows the output swing of the MAX4484 configured with $A_V = +1V/V$.

Driving Capacitive Loads

Driving a capacitive load can cause instability in many op amps, especially those with low quiescent current. The MAX4484/MAX4486/MAX4487 are unity-gain stable for a range of capacitive loads up to 100pF. Figure 2 shows the response of the MAX4484 with an excessive capacitive load. Adding a series resistor between the output and the load capacitor (Figure 3) improves the circuit's response by isolating the load capacitance from the op amp's output.

Applications Information

Power Supplies and Layout

The MAX4484/MAX4486/MAX4487 operates from a single +2.7V to +5.5V power supply. Bypass the power supply with 0.1 μ F capacitor to ground.

Good layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins. Use surface-mount components for best results.

Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

MAX4484/MAX4486/MAX4487

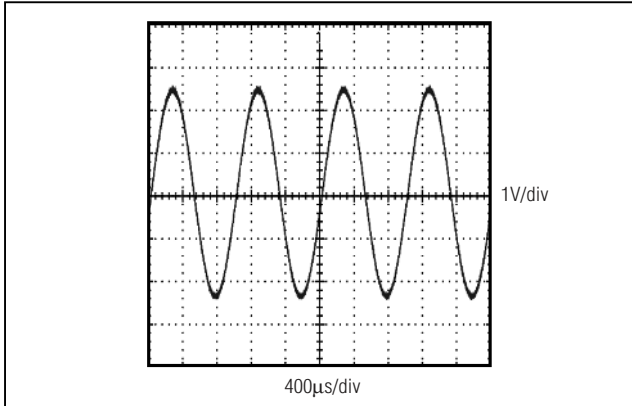


Figure 1. Rail-to-Rail Output Operation

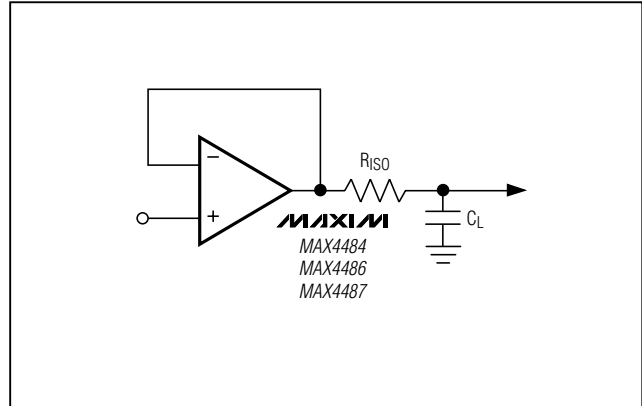


Figure 3. Capacitive-Load-Driving Circuit

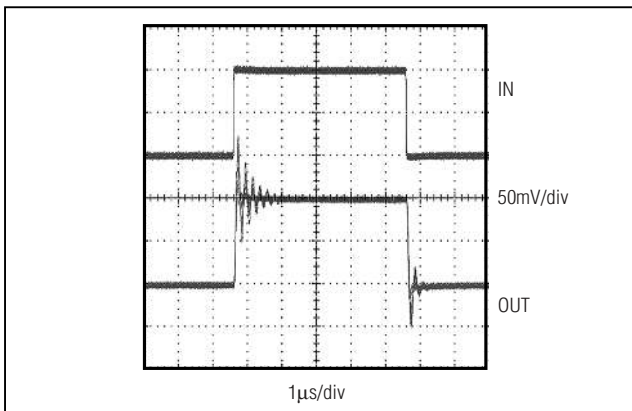


Figure 2. Small-Signal Transient Response with Excessive Capacitive Load ($C_L = 270\text{pF}$)

Chip Information

TRANSISTOR COUNT: MAX4484: 101
 MAX4486: 202
 MAX4487: 404

Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

Package Information

SYMBOL	MIN	MAX
e	0.65	BSC
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
L1	0.425	TYP.

NOTE:
 1. ALL DIMENSIONS ARE IN MILLIMETERS
 2. DIMENSIONS ARE INCLUSIVE OF PLATING
 3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
 4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70
 5. COPLANARITY 4 MILS. MAX.

MAXIM		
<small>PROPRIETARY INFORMATION</small>		
<small>TITLE:</small>		
PACKAGE OUTLINE, SC70, 5L		
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small>	<small>REV</small>
	21-0076	B 1/1

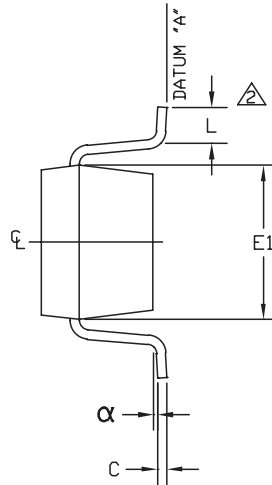
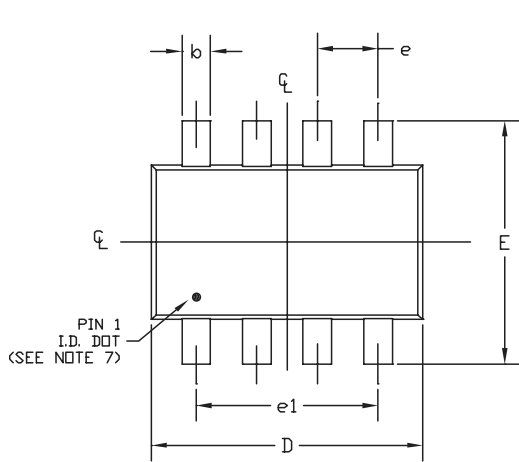
SC70-5LEPS

Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

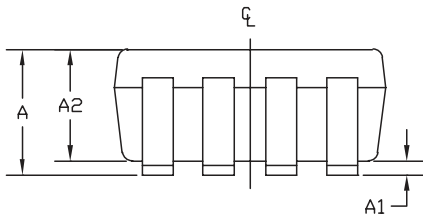
Package Information (continued)

MAX4484/MAX4486/MAX4487

SOT23, 8LEPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



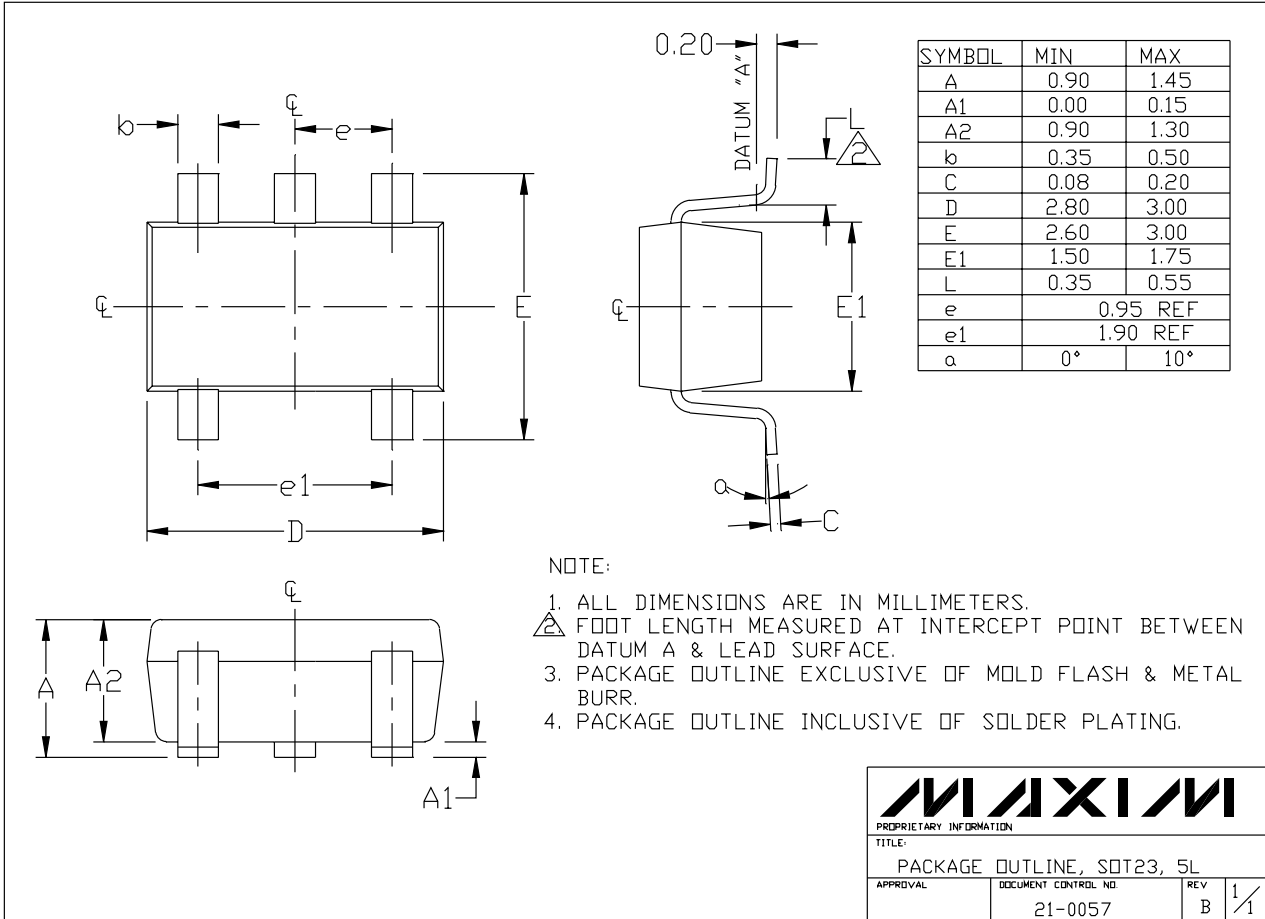
NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. \triangle FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ϕ MIN. LOCATED ABOVE PIN 1.

MAXIM		
PROPRIETARY INFORMATION		
TITLE: PACKAGE OUTLINE, SOT 23, 8L		
APPROVAL	DOCUMENT CONTROL NO. 21-0078	REV B 1/1

Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

Package Information (continued)



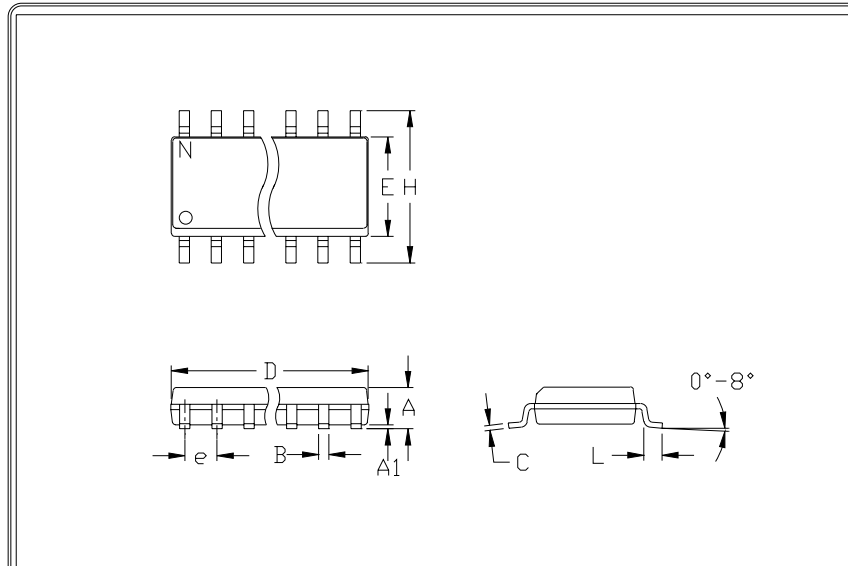
SOT23-5L

MAXIM
PROPRIETARY INFORMATION
 TITLE:
 PACKAGE OUTLINE, SOT23, 5L
 APPROVAL: _____ DOCUMENT CONTROL NO: 21-0057 REV: B 1/1

Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

Package Information (continued)

MAX4484/MAX4486/MAX4487



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS



PACKAGE FAMILY OUTLINE: SOIC .150" TITLE

1/1

21-0041 A DOCUMENT CONTROL NUMBER REV

Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

Package Information (continued)

COMMON DIMENSIONS

	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.05	1.10	.002	.043
A ₁	0.85	0.95	.033	.037
A ₂	0.19	0.30	.007	.012
b	0.19	0.25	.007	.010
b ₁	0.090	0.20	.0035	.008
c	0.090	0.135	.0035	.0053
D	SEE VARIATIONS SEE VARIATIONS			
E	4.30	4.50	.169	.177
e	0.65 BSC .026 BSC			
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS SEE VARIATIONS			
α	0°	8°	0°	8°

JEDEC	MD-153	N	VARIATIONS			
			MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AD	20	D	6.40	6.60	.252	.260
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386

NOTES:

- DIMENSIONS D AND E DO NOT INCLUDE FLASH
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
- CONTROLLING DIMENSION: MILLIMETER
- MEETS JEDEC OUTLINE MD-153 VARIATIONS- AB, AC, AD, AE, AF
- *N* REFERS TO NUMBER OF LEADS

△ THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL: _____ DOCUMENT CONTROL NO: 21-0066 REV: D 1/1

TSSOP, NO PADS, EPS

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