

## 64-Channel Serial-to-Parallel Converter with P-Channel Open Drain Controllable Output Current

### Features

- 5V CMOS Logic
- Up to -85V Output Voltage
- Output Current Source Control
- 16 MHz Equivalent Data Rate
- Latched Data Outputs
- Forward and Reverse Shifting Options (DIR pin)
- Diode to  $V_{DD}$  allows Efficient Power Recovery

### Applications

- Plasma Panel Driver
- Display Driver
- Print Head Driver
- Relay Driver
- Microelectromechanical Systems Applications

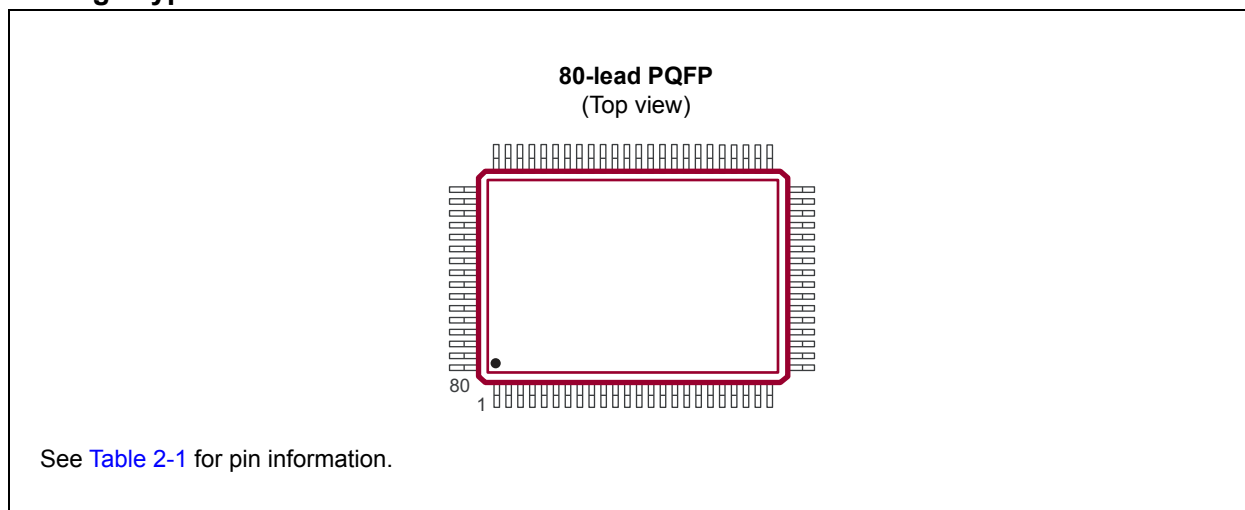
### General Description

The HV57009 is a low-voltage to high-voltage serial-to-parallel converter with P-channel open drain outputs. This device has been designed as a driver for plasma panels.

The device has two parallel 32-bit Shift registers, permitting data rates twice the speed of one in a single clock cycle. There are also 64 latches and control logic to perform the blanking of the outputs.  $HV_{OUT1}$  is connected to the first stage of the first Shift register through the blanking logic. Data is shifted through the Shift registers on the logic low-to-high transition of the clock. The DIR pin causes counter-clockwise shifting when connected to  $V_{SS}$  and clockwise shifting when connected to  $V_{DD}$ . A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register,  $HV_{OUT64}$ . The operation of the Shift register is not affected by the latch enable ( $\overline{LE}$ ) and the blanking ( $\overline{BL}$ ) inputs. Data transfer from the Shift registers to the latches occurs when the  $\overline{LE}$  input is high. The data in the latches is stored when  $\overline{LE}$  is low.

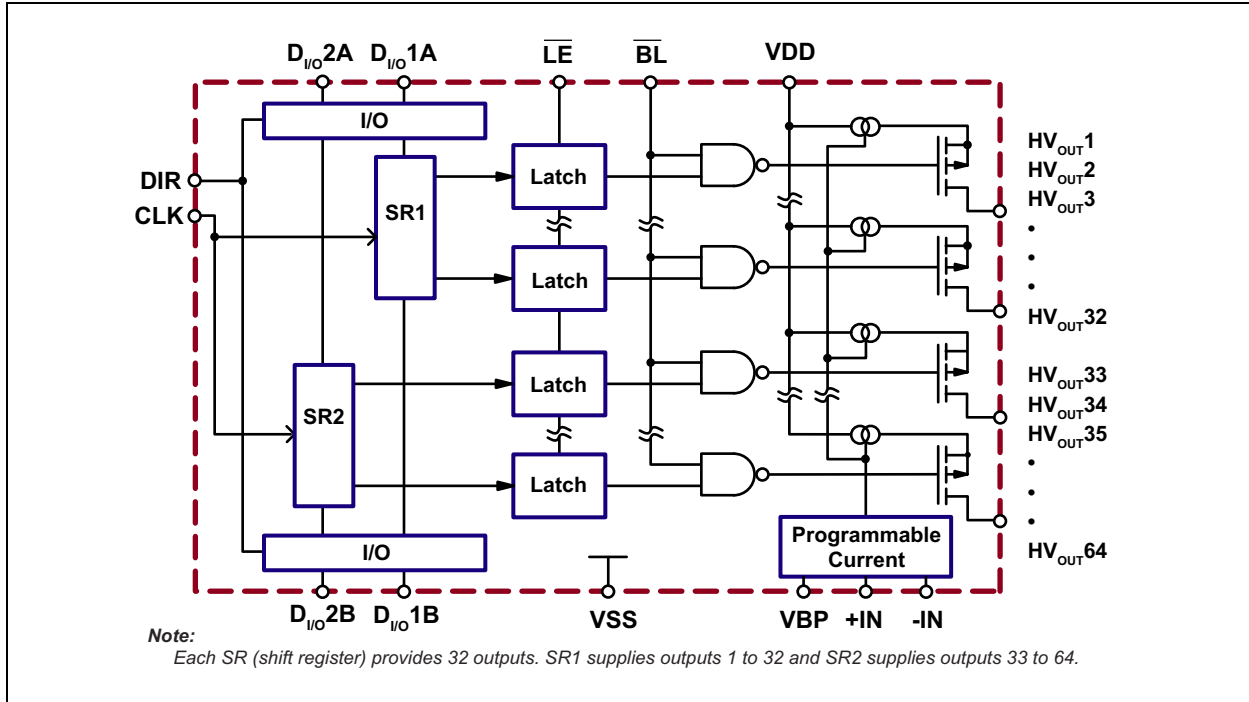
The HV57009 has 64 channels of output constant-current sourcing capability. They are adjustable from 0.1 mA to 2 mA through one external resistor or a current source.

### Package Type

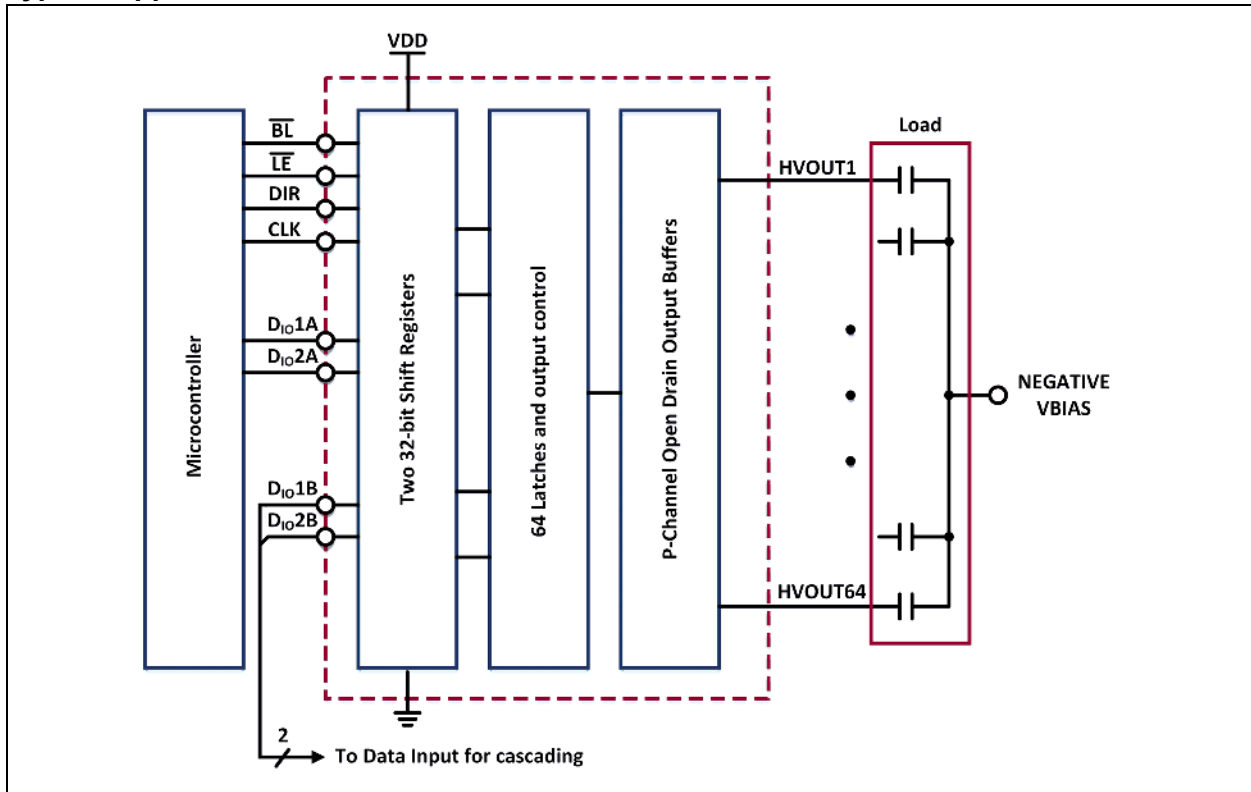


# HV57009

## Functional Block Diagram



## Typical Application Circuit



# HV57009

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Supply Voltage, $V_{DD}$ (Note 1)	–0.5V to +7.5V
Output Voltage, $V_{NN}$ (Note 1)	$V_{DD} + 0.5V$ to $-95V$
Logic Input Levels (Note 1)	$-0.3V$ to $V_{DD} + 0.3V$
Ground Current (Note 2)	1.5A
Operating Ambient Temperature, $T_A$	$-40^{\circ}C$ to $+85^{\circ}C$
Storage Temperature, $T_S$	$-65^{\circ}C$ to $+150^{\circ}C$
Continuous Total Power Dissipation:	
80-lead PQFP (Note 3)	1200 mW

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** All voltages are referenced to  $V_{SS}$ .

**Note 2:** Duty cycle is limited by the total power dissipated in the package.

**Note 3:** For operations above  $25^{\circ}C$  ambient, derate linearly to the maximum operating temperature at  $20\text{ mW}/^{\circ}C$ .

### RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	$V_{DD}$	4.5	—	5.5	V	
High-Voltage Output Voltage	$HV_{OUT}$	–85	—	$V_{DD}$	V	
High-Level Input Voltage	$V_{IH}$	$V_{DD}-1.2V$	—	$V_{DD}$	V	
Low-Level Input Voltage	$V_{IL}$	0	—	1.2	V	
Clock Frequency per Register	$f_{CLK}$	DC	—	8	MHz	
			—	4.5	MHz	
Operating Ambient Temperature	$T_A$	–40	—	+85	$^{\circ}C$	

## DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** All voltages are referenced to  $V_{SS}$ ,  $V_{SS} = 0$ , and  $T_A = 25^\circ\text{C}$ . Current going out of the chip is considered negative.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions	
$V_{DD}$ Supply Current	$I_{DD}$	—	—	15	mA	$V_{DD} = V_{DD}$ maximum, $f_{CLK} = 8$ MHz	
High-Voltage Supply Current	$I_{NN}$	—	—	-10	$\mu\text{A}$	Outputs off, $HV_{OUT} = -85\text{V}$ (total of all outputs)	
Quiescent $V_{DD}$ Supply Current	$I_{DDQ}$	—	—	100	$\mu\text{A}$	All inputs = $V_{DD}$ , except $+IN = V_{SS} = \text{GND}$	
High-Level Output	Data Out	$V_{OH}$	$V_{DD}-0.5\text{V}$	—	—	V	$I_O = -100 \mu\text{A}$
	$HV_{OUT}$		+1	—	$V_{DD}$	V	$I_O = -2 \text{ mA}$
Low-Level Output	Data Out	$V_{OL}$	—	—	+0.5	V	$I_O = 100 \mu\text{A}$
High-Level Logic Input Current	$I_{IH}$	—	—	1	$\mu\text{A}$	$V_{IH} = V_{DD}$	
Low-Level Logic Input Current	$I_{IL}$	—	—	-1	$\mu\text{A}$	$V_{IL} = 0\text{V}$	
High-Output Source Current	$I_{CS}$	—	—	-2	mA	$V_{REF} = 2\text{V}$ , $R_{EXT} = 1 \text{ k}\Omega$ , See <a href="#">Figure 3-3</a> and <a href="#">Figure 3-4</a> .	
		-0.1	—	—	mA	$V_{REF} = 0.1\text{V}$ , $R_{EXT} = 1 \text{ k}\Omega$ , See <a href="#">Figure 3-3</a> and <a href="#">Figure 3-4</a> .	
High-Voltage Output Source Current for $I_{REF} = 2 \text{ mA}$	$\Delta I_{CS}$	—	—	10	%	$V_{REF} = 2\text{V}$ , $R_{EXT} = 1 \text{ k}\Omega$ ,	

## AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Logic signal inputs and data inputs have  $t_r$ ,  $t_f \leq 5 \text{ ns}$  (10% and 90% points) for measurements.

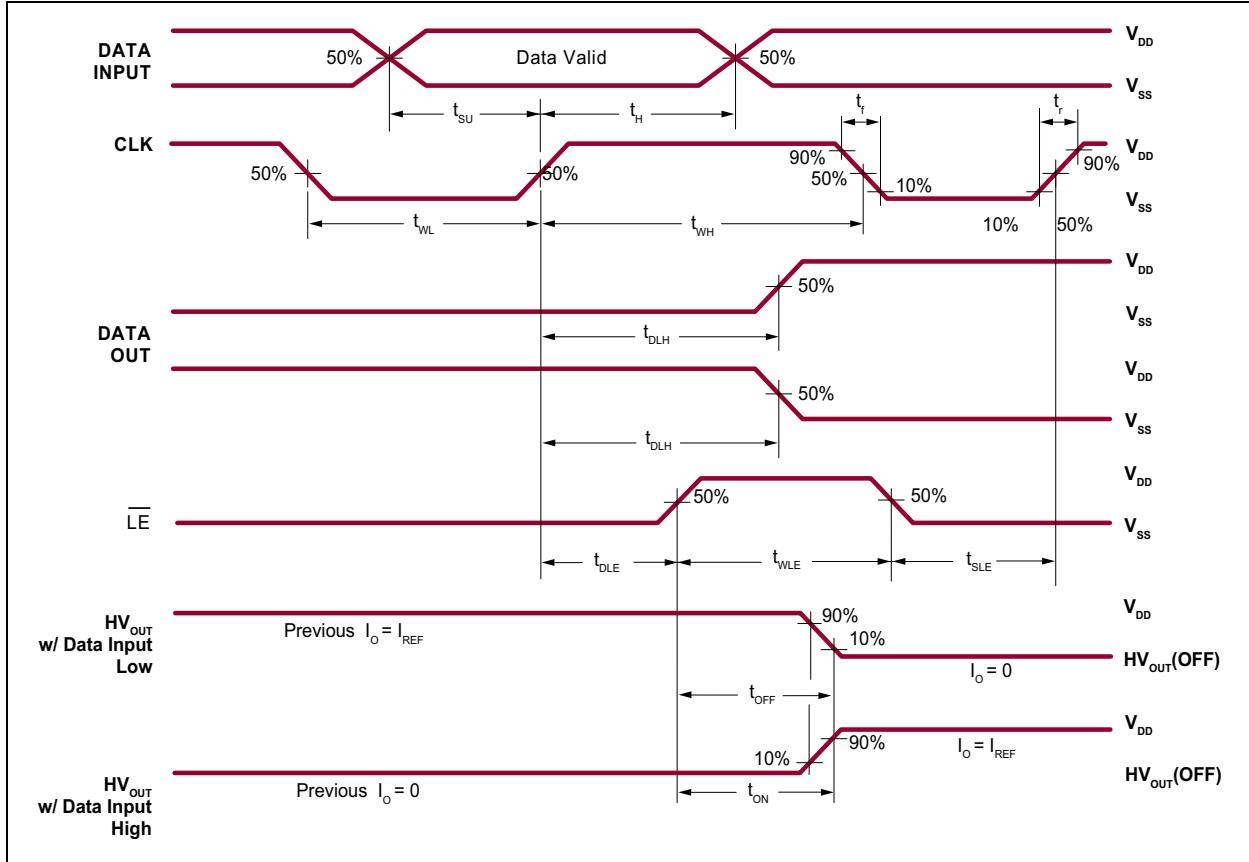
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	$f_{CLK}$	DC	—	8	MHz	Per register
			—	4.5	MHz	When cascading devices
Clock Width High or Low	$t_{WL}$ , $t_{WH}$	62	—	—	ns	
Data Set-Up Time before Clock Rises	$t_{SU}$	20	—	—	ns	
Data Hold Time after Clock Rises	$t_H$	15	—	—	ns	
Time from Latch Enable to $HV_{OUT}$	$t_{ON}$ , $t_{OFF}$	—	—	500	ns	$C_L = 15 \text{ pF}$
Latch Enable Pulse Width	$t_{WLE}$	25	—	—	ns	
Delay Time Clock to Latch Enable Low to High	$t_{DLE}$	45	—	—	ns	
Latch Enable Set-Up Time before Clock Rises	$t_{SLE}$	0	—	—	ns	
Delay Time Clock to Data Low to High	$t_{DLH}$	—	—	150	ns	$C_L = 15 \text{ pF}$
Delay Time Clock to Data High to Low	$t_{DHL}$	—	—	150	ns	$C_L = 15 \text{ pF}$
Maximum Allowable Clock Rise and Fall Time (10% and 90% Points)	$t_r$ , $t_f$	—	—	100	ns	

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## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Ambient Temperature	$T_A$	-40	—	+85	°C	
Storage Temperature	$T_S$	-65	—	+150	°C	
<b>PACKAGE THERMAL RESISTANCE</b>						
80-lead PQFP	$\theta_{JA}$	—	37	—	°C/W	

## Timing Waveforms



## 2.0 PIN DESCRIPTION

The details on the pins of HV57009 are listed on [Table 2-1](#). Refer to [Package Type](#) for the location of pins.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	HVOUT24	High-voltage output
2	HVOUT23	High-voltage output
3	HVOUT22	High-voltage output
4	HVOUT21	High-voltage output
5	HVOUT20	High-voltage output
6	HVOUT19	High-voltage output
7	HVOUT18	High-voltage output
8	HVOUT17	High-voltage output
9	HVOUT16	High-voltage output
10	HVOUT15	High-voltage output
11	HVOUT14	High-voltage output
12	HVOUT13	High-voltage output
13	HVOUT12	High-voltage output
14	HVOUT11	High-voltage output
15	HVOUT10	High-voltage output
16	HVOUT9	High-voltage output
17	HVOUT8	High-voltage output
18	HVOUT7	High-voltage output
19	HVOUT6	High-voltage output
20	HVOUT5	High-voltage output
21	HVOUT4	High-voltage output
22	HVOUT3	High-voltage output
23	HVOUT2	High-voltage output
24	HVOUT1	High-voltage output
25	DI/O1A	Data Input/Output 1A pin
26	DI/O2A	Data Input/Output 2A pin
27	NC	No connection
28	NC	No connection
29	$\overline{LE}$	Latch enable pin
30	CLK	Clock pin
31	$\overline{BL}$	Blanking pin
32	VSS	Reference voltage (usually ground)
33	DIR	Direction pin (See <a href="#">Note 1</a> .)
34	VDD	Logic supply voltage (See <a href="#">Note 2</a> .)

**Note 1:** Pin designation for DIR =  $V_{DD}$ .

**2:** 0.1  $\mu$ F capacitor is needed between VDD and VBP (pin 40) for better output current stability and to prevent transient cross-coupling between outputs. See [Figure 3-3](#) and [Figure 3-4](#).

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TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
35	-IN	-IN input pin
36	DI/O2B	Data Input/Output 2B pin
37	DI/O1B	Data Input/Output 1B pin
38	NC	No connection
39	+IN	+IN input pin
40	VBP	Bias control voltage (See <a href="#">Note 2</a> .)
41	HVOUT64	High-voltage output
42	HVOUT63	High-voltage output
43	HVOUT62	High-voltage output
44	HVOUT61	High-voltage output
45	HVOUT60	High-voltage output
46	HVOUT59	High-voltage output
47	HVOUT58	High-voltage output
48	HVOUT57	High-voltage output
49	HVOUT56	High-voltage output
50	HVOUT55	High-voltage output
51	HVOUT54	High-voltage output
52	HVOUT53	High-voltage output
53	HVOUT52	High-voltage output
54	HVOUT51	High-voltage output
55	HVOUT50	High-voltage output
56	HVOUT49	High-voltage output
57	HVOUT48	High-voltage output
58	HVOUT47	High-voltage output
59	HVOUT46	High-voltage output
60	HVOUT45	High-voltage output
61	HVOUT44	High-voltage output
62	HVOUT43	High-voltage output
63	HVOUT42	High-voltage output
64	HVOUT41	High-voltage output
65	HVOUT40	High-voltage output
66	HVOUT39	High-voltage output
67	HVOUT38	High-voltage output
68	HVOUT37	High-voltage output
69	HVOUT36	High-voltage output
70	HVOUT35	High-voltage output
71	HVOUT34	High-voltage output
72	HVOUT33	High-voltage output
73	HVOUT32	High-voltage output

**Note 1:** Pin designation for DIR =  $V_{DD}$ .

**2:** 0.1  $\mu$ F capacitor is needed between VDD and VBP (pin 40) for better output current stability and to prevent transient cross-coupling between outputs. See [Figure 3-3](#) and [Figure 3-4](#).



**TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)**

Pin Number	Pin Name	Description
74	HVOUT31	High-voltage output
75	HVOUT30	High-voltage output
76	HVOUT29	High-voltage output
77	HVOUT28	High-voltage output
78	HVOUT27	High-voltage output
79	HVOUT26	High-voltage output
80	HVOUT25	High-voltage output

**Note 1:** Pin designation for DIR =  $V_{DD}$ .

**2:** 0.1  $\mu$ F capacitor is needed between VDD and VBP (pin 40) for better output current stability and to prevent transient cross-coupling between outputs. See [Figure 3-3](#) and [Figure 3-4](#).

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## 3.0 FUNCTIONAL DESCRIPTION

Follow the steps in [Table 3-1](#) to power up and power down the HV57009.

**TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE**

Power-up		Power-down	
Step	Description	Step	Description
1	Connect ground.	1	Remove $V_{PP}$ .
2	Apply $V_{DD}$ .	2	Remove all inputs.
3	Set all inputs (Data, CLK, Enable, etc.) to a known state.	3	Remove $V_{DD}$ .
4	Apply $V_{PP}$ .	4	Disconnect ground.

**TABLE 3-2: TRUTH FUNCTION TABLE**

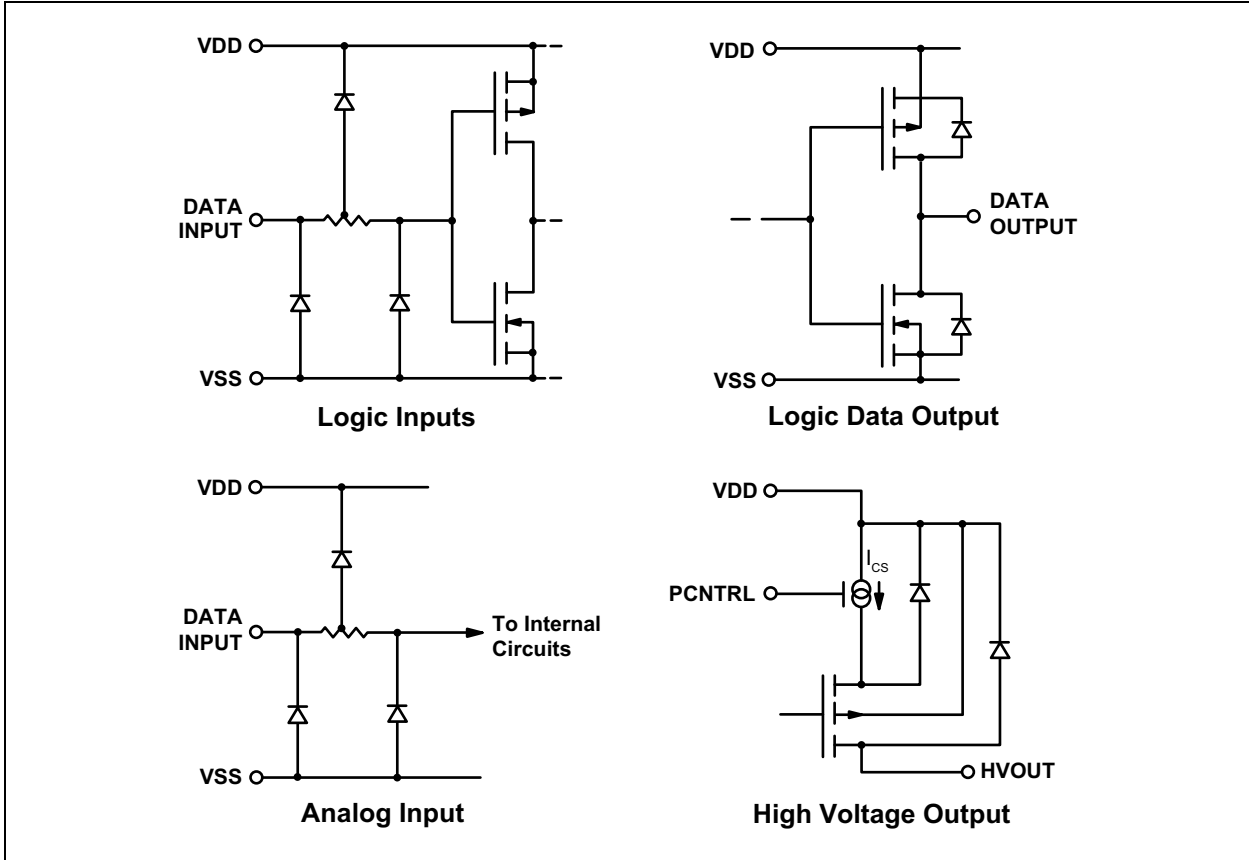
Function	Inputs						Outputs	
	Data	CLK	$\overline{LE}$	$\overline{BL}$	DIR	Shift Register	High-voltage Output	Data Out
All O/P High	X	X	X	L	X	*	ON	*
Data Falls Through (Latches Transparent)	L	↑	H	H	X	L...L	ON	L
	H	↑	H	H	X	H...H	OFF	H
Data Stored in Latches	X	X	L	H	X	*	Inversion of stored data	*
I/O Relation	$D_{I/O1-2A}$	↑	H	H	H	$Q_N \rightarrow Q_{N+1}$	New ON or OFF	$D_{I/O1-2B}$
	$D_{I/O1-2A}$	↑	L	H	H	$Q_N \rightarrow Q_{N+1}$	Previous ON or OFF	$D_{I/O1-2B}$
	$D_{I/O1-2B}$	↑	L	H	L	$Q_N \rightarrow Q_{N-1}$	Previous ON or OFF	$D_{I/O1-2A}$
	$D_{I/O1-2B}$	↑	H	H	L	$Q_N \rightarrow Q_{N-1}$	New ON or OFF	$D_{I/O1-2A}$

**Note:** H =  $V_{DD}$  (Logic)/ $V_{NN}$  (HV Outputs)

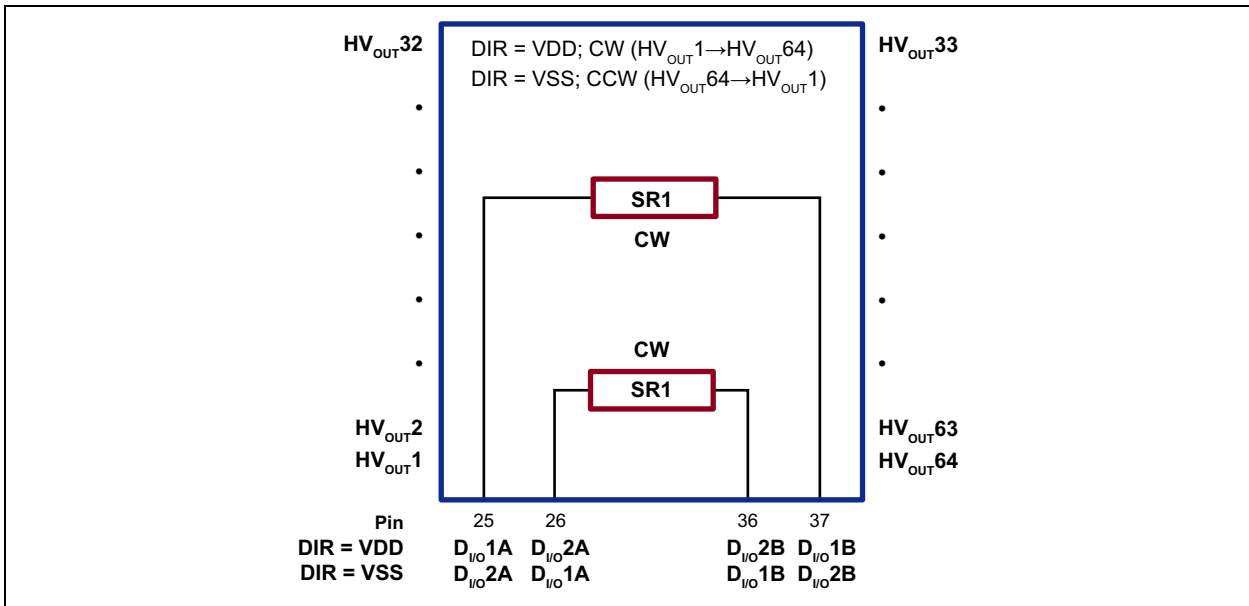
L =  $V_{SS}$

↑ = Low-to-high transition

\* = Dependent on the previous stage's state. See [Figure 3-2](#) for  $D_{IN}$  and  $D_{OUT}$  pin designation for clockwise and counter-clockwise shifts.



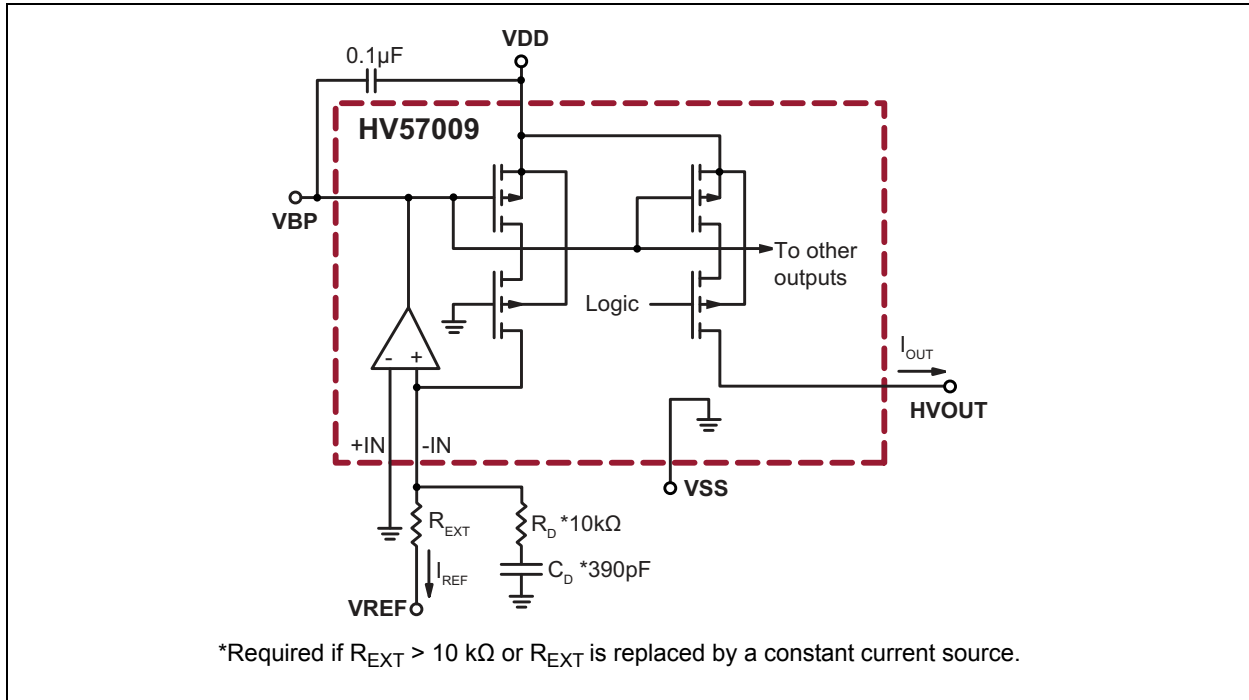
**FIGURE 3-1:** Input and Output Equivalent Circuits.



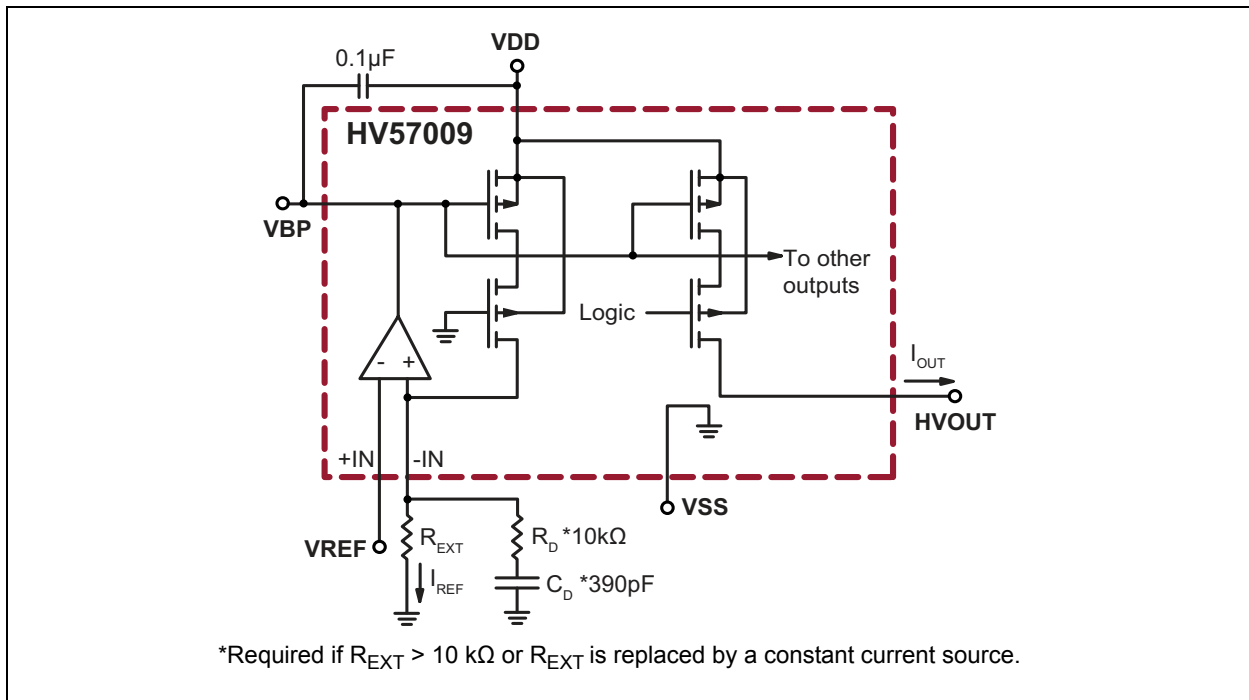
**FIGURE 3-2:** Shift Register Operation.

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## 3.1 Typical Current Programming Circuits



**FIGURE 3-3:** Negative Control Circuit.



**FIGURE 3-4:** Positive Control Circuit.

Figure 3-3 and Figure 3-4 show the programming circuits to control the high-voltage output current limit. A reference current  $I_{REF}$  is set by the external resistor  $R_{EXT}$  and reference voltage  $V_{REF}$ . The current mirror formed by the matching transistors uses the reference current to cap the maximum allowed current at the high-voltage output. The relationship between  $I_{OUT}$  and  $I_{REF}$  are shown in Equation 3-1 and Equation 3-2.

**EQUATION 3-1:**

$$I_{OUT} = I_{REF} = |V_{REF}| / R_{EXT}$$

**EQUATION 3-2:**

If  $I_{OUT} = 2 \text{ mA}$  and  $V_{REF} = -5V \rightarrow R_{EXT} = 2.5 \text{ k}\Omega$   
 If  $I_{OUT} = 1 \text{ mA}$  and  $R_{EXT} = 1 \text{ k}\Omega \rightarrow V_{REF} = -1V$

If  $R_{EXT} > 10 \text{ k}\Omega$ , add series network  $R_D$  and  $C_D$  to ground for stability as shown in Figure 3-3 and Figure 3-4.

This control method behaves linearly as long as the operational amplifier is not saturated. However, it requires a negative power source and needs to provide a current  $I_{REF} = I_{OUT}$  for each HV57009 chip being controlled.

If  $HV_{OUT} \geq +1V$ , the  $HV_{OUT}$  cascade may no longer operate as a perfect current source, and the output current will diminish. This effect depends on the magnitude of the output current.

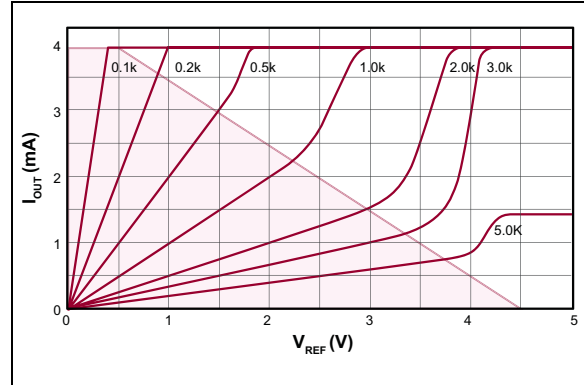
Given  $I_{OUT}$  and  $V_{REF}$ , the  $R_{EXT}$  can be calculated using Equation 3-3:

**EQUATION 3-3:**

$$R_{EXT} = V_{REF} / I_{REF} = V_{REF} / I_{OUT}$$

The intersection of a set of  $I_{OUT}$  and  $V_{REF}$  values can be located in Figure 3-5. The value picked for  $R_{EXT}$  must always be in the shaded area for linear operation. This control method has the advantage that  $V_{REF}$  is positive and draws leakage current only. If  $R_{EXT} > 10 \text{ k}\Omega$ , add series network  $R_D$  and  $C_D$  to ground for stability as shown in Figure 3-3 and Figure 3-4.

**Note:** Lower reference current,  $I_{REF}$ , results in higher distortion,  $\Delta I_{CS}$ , on the output.

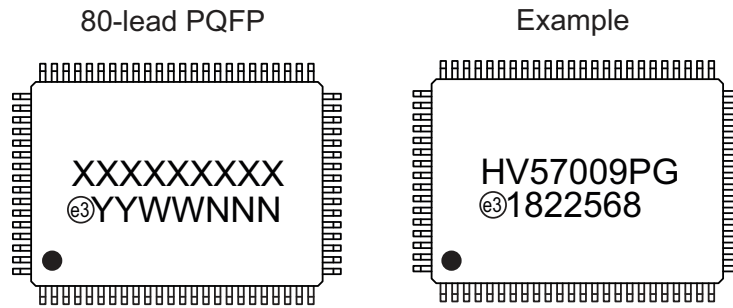


**FIGURE 3-5:**  $I_{OUT}$  vs.  $I_{REF}$

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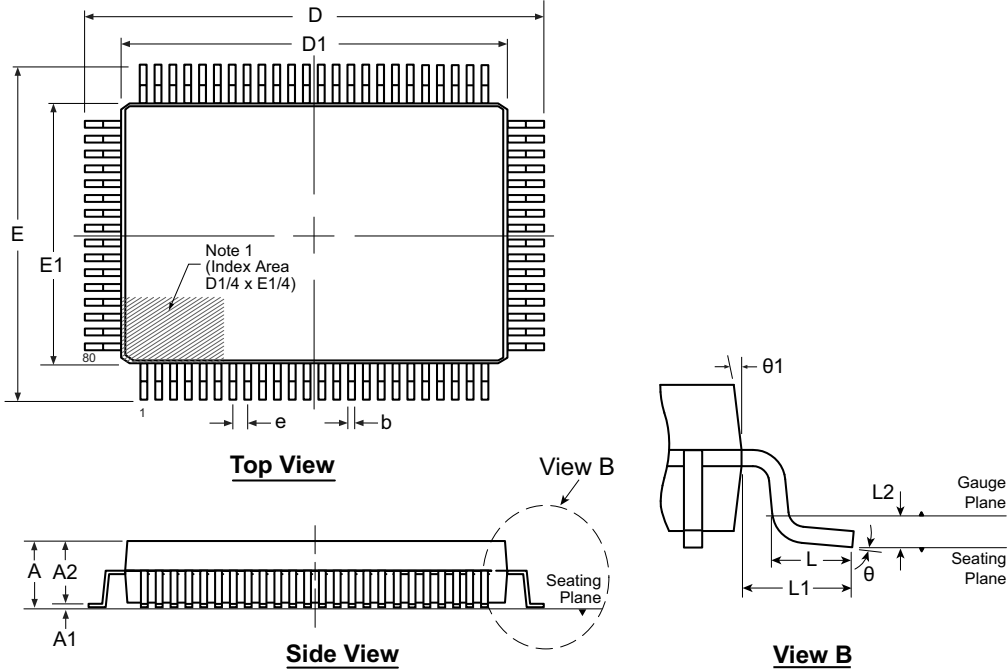
## 4.0 PACKAGE MARKING INFORMATION

### 4.1 Packaging Information



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

## 80-Lead PQFP Package Outline (PG) 20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

- Note:
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1	
Dimension (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88		3.5°	-	
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03		7°	16°	

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept. 1995.  
 \* This dimension is not specified in the JEDEC drawing.  
 Drawings not to scale.

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NOTES:



## APPENDIX A: REVISION HISTORY

### Revision A (April 2018)

- Converted Supertex Doc # DSFP-HV57009 to Microchip DS20005856A
- Removed “HVCMOS<sup>®</sup> Technology” in the Features section
- Changed the package marking format
- Made minor changes throughout the document

# HV57009

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	HV57009	=	64-Channel Serial-to-Parallel Converter with P-Channel Open Drain Controllable Output Current		
Package:	PG	=	80-lead PQFP		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	66/Tray for a PG Package		

**Example:**

a) HV57009PG-G: 64-Channel Serial-to-Parallel Converter with P-Channel Open Drain Controllable Output Current, 80-lead PQFP, 66/Tray

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