Dual Synchronous Step-Down Controller for Low-Voltage Power Rails in Embedded Computing Systems

FEATURES

- **High Efficiency, Low-Power Consumption, Shutdowns to <1 μA**
- **Fixed Frequency Emulated On-Time Control, Frequency Selectable From Three Options**
- **D-CAP™ Mode Enables Fast Transient Response**
- **Auto-Skip Mode**
- **Less Than 1% Initial Reference Accuracy**
- **Low Output Ripple**
- **Wide Input Voltage Range: 3 V to 28 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Low-Side $R_{DS(on)}$ Loss-less Current Sensing**
- **Adaptive Gate Drivers With Integrated Boost Diode**
- **Internal 1.2-ms Voltage-Servo Soft Start**
- **Power-Good Signals for Each Channel With Delay Timer**
- **Output Discharge During Disable, Fault**

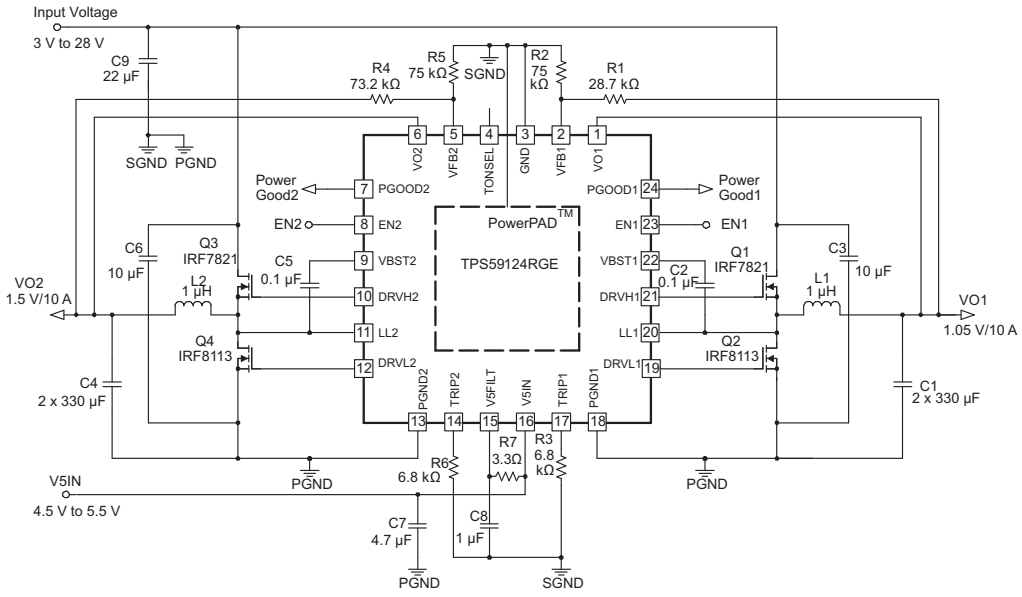
APPLICATIONS

- **I/O and Low Voltage System Bus in Embedded Computing Systems**

DESCRIPTION

The TPS59124 is a dual, adaptive on-time D-CAP™ mode synchronous buck controller. This device enables system designers to cost effectively complete the suite of embedded computer power bus regulators with the absolute lowest external component count and lowest standby consumption. The fixed-frequency emulated adaptive on-time control supports seamless operation between PWM mode at heavy load condition and reduced frequency operation at light load for high-efficiency down to milliampere range. The main control loop for the TPS59124 uses the D-CAP mode that optimized for low-ESR output capacitors such as POSCAP or SP-CAP promises fast transient response with no external compensation. Simple and separate power good signals for each channel allow flexibility of power sequencing. The device provides convenient and efficient operation with supply input voltages (V5IN, V5FILT) ranging from 4.5 V to 5.5 V, conversion voltages (drain voltage for the synchronous high-side MOSFET) from 3 V to 28 V and output voltages from 0.76 V to 5.5 V.

The TPS59124 is available in 24-pin QFN package specified from –40°C to 85°C ambient temperature range.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY	MINIMUM ORDER QUANTITY	ECO PLAN
–40°C to 85°C	Plastic Quad Flat Pack (QFN)	TPS59124RGET	24	Tape-and-Reel	250	Green (RoHS and no Sb/Br)
		TPS59124RGER			3000	

(1) All packaging options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input voltage range	VBST1, VBST2	–0.3 to 36	V
	VBST1, VBST2 (wrt LLx)	–0.3 to 6	
	V5IN, V5FILT, EN1, EN2, VFB1, VFB2, TRIP1, TRIP2, VO1, VO2, TONSEL	–0.3 to 6	
Output voltage range	DRVH1, DRVH2	–1 to 36	V
	DRVH1, DRVH2 (wrt LLx)	–0.3 to 6	
	LL1, LL2	–2 to 30	
	PGOOD1, PGOOD2, DRVL1, DRVL2	–0.3 to 6	
	PGND1, PGND2	–0.3 to 0.3	
T_A	Operating ambient temperature range	–40 to 85	°C
T_{stg}	Storage temperature range	–55 to 150	°C
T_J	Junction temperature range	–40 to 125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted

DISSIPATION RATINGS

PACKAGE	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
24-pin QFN(1)	2.33 W	23.3 mW/°C	0.93 W

(1) Enhanced thermal conductance by 2 × 2 thermal vias beneath thermal pad.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply input voltage range	V5IN, V5FILT	4.5	5.5	V
Input voltage range	VBST1, VBST2	–0.1	34	V
	VBST1, VBST2 (wrt LLx)	–0.1	5.5	
	EN1, EN2, VFB1, VFB2, TRIP1, TRIP2, VO1, VO2, TONSEL	–0.1	5.5	
Output voltage range	DRVH1, DRVH2	–0.8	34	V
	DRVH1, DRVH2 (wrt LLx)	–0.1	5.5	
	LL1, LL2	–1.8	28	
	PGOOD1, PGOOD2, DRVL1, DRVL2	–0.1	5.5	
	PGND1, PGND2	–0.1	0.1	
T_A Operating ambient temperature range		–40	85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{V5IN} = V_{V5FILT} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V5FILT}	V5FILT supply current	V5FILT current, no load, V_{EN1} = V_{EN2} = 5 V, V_{VFB1} = V_{VFB2} = 0.77 V, V_{LL1} = V_{LL2} = 0.5 V		350	700	µA
$I_{V5INSDN}$	V5IN shutdown current	V5IN current, no load, EN1 = EN2 = 0 V			1	µA
$I_{V5FILTSDN}$	V5FILT shutdown current	V5FILT current, no load, EN1 = EN2 = 0 V			1	µA
VFB VOLTAGE and DISCHARGE RESISTANCE						
V_{VFB}	VFB regulation voltage	Feedback voltage, skip mode (f_{PWM}/10)		764		mV
V_{VFB}	VFB regulation voltage tolerance	T_A = 25°C, bandgap initial accuracy	–0.9%		0.9%	
		T_A = 0°C to 85°C(1)	–1.3%		1.3%	
		T_A = –40°C to 85°C(1)	–1.6%		1.6%	
$V_{VFBSKIP}$	VFB regulation shift in continuous conduction	0.758-V target for resistor divider. See PWM Operation of Detailed Description(1)		758		mV
I_{VFB}	VFB input current	V_{VFBx} = 0.758 V, absolute value		0.02	0.1	µA
R_{Dischg}	VO discharge resistance	V_{ENx} = 0 V, V_{VOx} = = 0.5 V, T_A = 25°C		10	20	Ω
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
R_{DRVH}	DRVH resistance	Source, $V_{VBSTx–DRVHx}$ = 0.5 V		5	7	Ω
		Sink, $V_{DRVHx-LLx}$= 0.5 V		1.5	2.5	Ω
R_{DRVL}	DRVL resistance	Source, $V_{V5IN–DRVLx}$ = 0.5 V		4	6	Ω
		Sink, $V_{DRVLx–PGNDx}$ = 0.5 V		1	2.0	Ω
t_D	Dead time	DRVHx-low (DRVHx = 1 V) to DRVLx-on (DRVLx = 4 V), LL = –0.05 V,	10	20	50	ns
		DRVLx-low (DRVLx = 1 V) to DRVHx-on (DRVHx = 4 V), LL = –0.05 V,	30	40	60	ns
INTERNAL BST DIODE						
V_{FBST}	Forward voltage	$V_{V5IN–VBSTx}$, I_F = 10 mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakage current	V_{VBST} = 34 V, V_{LL} = 28 V, V_{VOx} = 5.5 V, T_A = 25°C		0.1	1	µA
ON-TIME TIMER CONTROL AND INTERNAL SOFT START,						
t_{ON11}	CH1, 240-kHz setting	V_{VO1} = 1.5 V,V_{TONSEL} = GND, V_{LL1} = 12 V	440	500	560	ns
t_{ON12}	CH1, 300-kHz setting	V_{VO1} = 1.5 V, V_{TONSEL} = FLOAT, V_{LL1} = 12 V	340	390	440	ns
t_{ON13}	CH1, 360-kHz setting	V_{VO1} = 1.5 V, V_{TONSEL} = V5FILT, V_{LL1} = 12 V	265	305	345	ns
t_{ON21}	CH2, 300-kHz setting	V_{VO2} = 1.05 V, V_{TONSEL} = GND, V_{LL2} = 12 V	235	270	305	ns
t_{ON22}	CH2, 360-kHz setting	V_{VO2} = 1.05 V, V_{TONSEL} = FLOAT, V_{LL2} = 12 V	180	210	240	ns
t_{ON23}	CH2, 420-kHz setting	V_{VO2} = 1.05 V, V_{TONSEL} = V5FILT, V_{LL2} = 12 V	120	150	180	ns
$t_{ON(min)}$	CH2 On time	V_{VO2} = 0.76 V, V_{TONSEL} = V5FILT, V_{LL2} = 28 V	80	110	140	ns
$t_{OFF(min)}$	CH1/CH2 Min. off time	V_{LLx} = –0.1 V, T_A= 25°C, VFB = 0.7 V		435		ns
t_{ss}	Internal SS time	Internal soft-start, time from V_{ENx} > 3 V to V_{VFBx} regulation value = 735 mV	0.85	1.2	1.40	ms

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (Continued)

over operating free-air temperature range, V5IN = V5FILT = 5 V (unless otherwise noted)

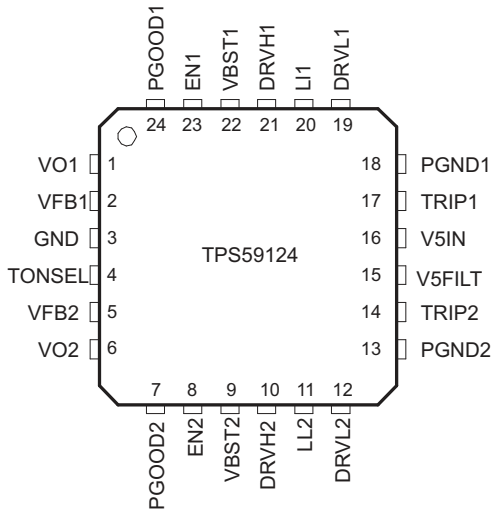
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO/LOGIC THRESHOLD						
$V_{UV5VFILT}$	V5FILT UVLO threshold	Wake up	3.7	4.0	4.3	V
		Hysteresis	0.2	0.3	0.4	V
V_{EN}	ENx threshold	Wake up	1.0	1.3	1.5	V
		Hysteresis		0.2		V
I_{EN}	ENx input current	Absolute value(1)		0.02	0.1	µA
V_{TONSEL}	TONSEL threshold	Fast(1)	V5FILT –0.3			V
		Medium(1)	2		V5FILT –1.0	V
		Slow(1)			0.5	V
I_{TONSEL}	TONSEL input current	V_{TONSEL}=0 V, current out of the pin(1)		1		µA
		V_{TONSEL}=5 V, current in to the pin(1)		1		µA
CURRENT SENSE						
I_{TRIP}	TRIP source current	V_{TRIPx} < 0.3 V, T_A = 25°C	9	10	11	µA
TC_{ITRIP}	I_{TRIP} temperature coeffficent	On the basis of 25°C(1)		4200		ppm/°C
V_{OCLoff}	OCP compensation offset	($V_{TRIPx-GND}$ – $V_{PGNDx-LLx}$) voltage, $V_{TRIPx-GND}$ = 60 mV	–10	0	10	mV
V_{ZC}	Zero cross detection comparator offset	VPGNDx-LLx voltage, PGOODx = Hi(1)		0.5		mV
V_{RTRIP}	Current limit threshold setting range	$V_{TRIPx-GND}$ voltage, all temperatures(1)	30		200	mV
POWER-GOOD COMPARATOR						
V_{THPG}	PG threshold	PG in from lower (PGOODx goes hi)	92.5%	95%	97.5%	
		PG low hysteresis (PGOODx goes low)		–5%		
		PG in from higher (PGOODx goes hi)	102.5%	105%	107.5%	
		PG high hysteresis (PGOODx goes low)		5%		
I_{PGMAX}	PG sink current	PGOODx = 0.5 V	2.5	5.0		mA
t_{PGDEL}	PG delay	Delay for PG in	400	510	620	µs
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	110%	115%	120%	
t_{OVPDEL}	Output OVP propagation delay time			1.5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis (recovery < 20 µs)		10%		
t_{UVPDEL}	Output UVP delay time		20	32	40	µs
t_{UVPEN}	Output UVP enable delay time	After 1.7 × Tss, UVP protection engaged	1.4	2	2.4	ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		160		°C
		Hysteresis(1)		10		

(1) Ensured by design. Not production tested.

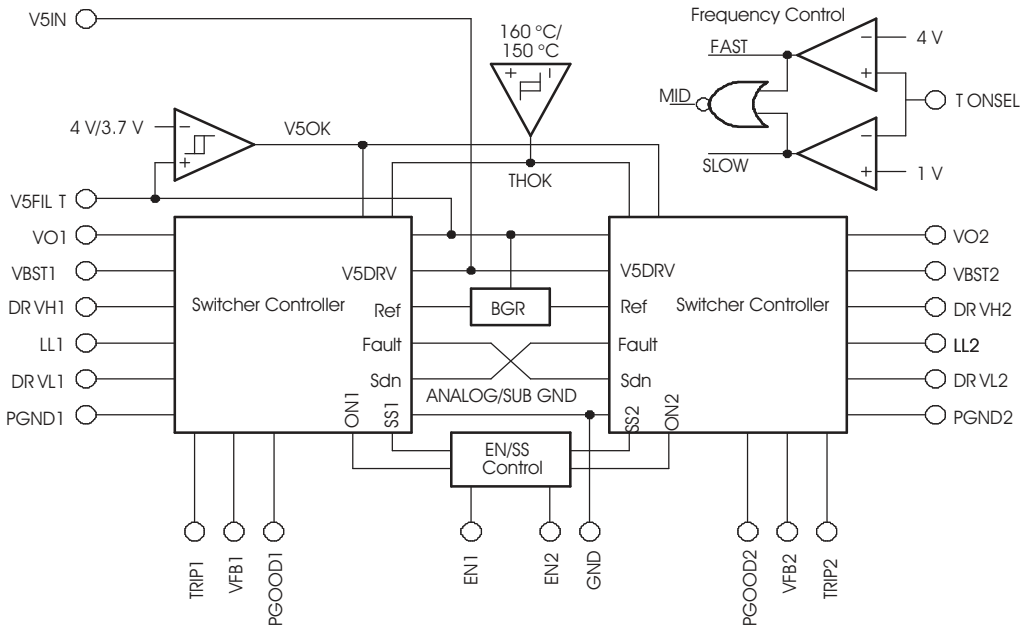
DEVICE INFORMATION

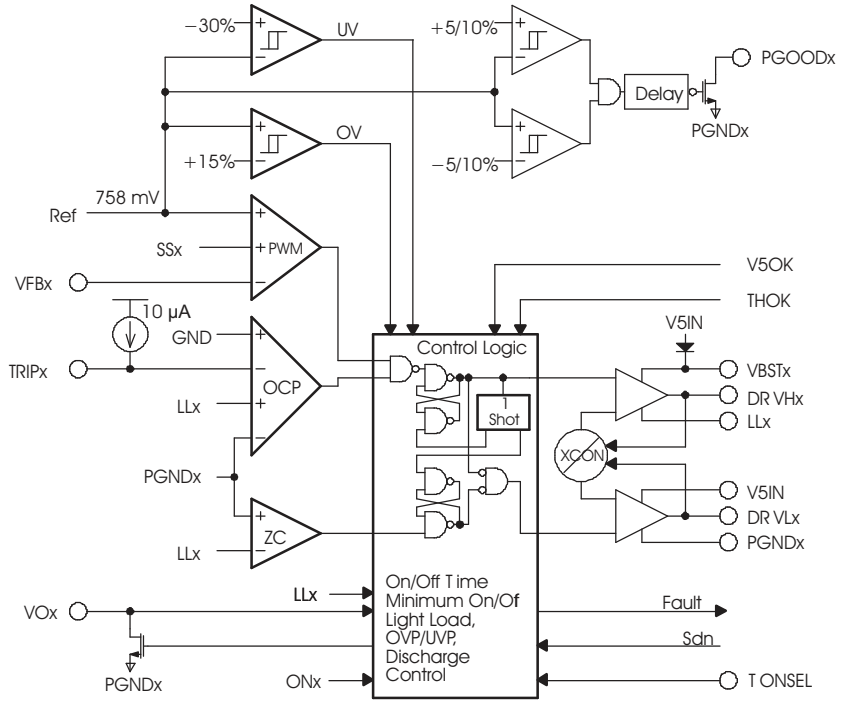
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DRVH1	21	O	Synchronous high-side MOSFET driver outputs. LL node referenced floating drivers. The gate drive voltage is defined by the voltage across VBST to LL node flying capacitor.
DRVH2	10		
DRVL1	19	O	Synchronous low-side MOSFET driver outputs. PGND referenced drivers. The gate drive voltage is defined by V5IN voltage.
DRVL2	12		
EN1	23	I	Channel 1 and channel 2 enable pins. Connect to 5 V or 3.3 V to turn on SMPS
EN2	8		
GND	3	I	Signal ground pin
LL1	20	I/O	Switch node connections for high-side drivers return. Also serve as input to current comparators and input voltage monitor for on-time control circuitry.
LL2	11		
PGND1	18	I/O	Ground returns for DRVL1 and DRVL2. Also serve as input of current comparators. Connect PGND1, PGND2, and GND strongly together near the IC. Output discharge current flows through this pin, also.
PGND2	13		
PGOOD1	24	O	Power Good window comparator open drain output for channel 1 and 2. Pull up with a resistor to 5 V, or appropriate signal voltage. Current capability is 5 mA. PGOOD goes high 0.5 ms after VFB comes within specified limits. Power bad, or the terminal goes low, is within 10 μs.
PGOOD2	7		
TONSEL	4	I	On-time selection pin. See Table 1.
TRIP1	17	I	Over-current trip point set input. Connect resistor from this pin to GND to set threshold for synchronous low-side $R_{DS(on)}$ sense. Voltage across this pin and GND is compared to voltage across PGND and LL at over-current comparator.
TRIP2	14		
VBST1	22	I	Supply input for synchronous high-side MOSFET driver (Boost Terminal). Connect capacitor from this pin to respective LL terminals. An internal PN diode is connected between V5IN to each of these pins. User can add external Schottky diode if forward drop is critical to drive the MOSFET.
VBST2	9		
VFB1	2	I	SMPS voltage feedback inputs. Connect with feedback resistor divider.
VFB2	5		
VO1	1	I	Output connections to SMPS. These terminals serve two functions: On-time adjustment and output discharge.
VO2	6		
V5FILT	15	I	5-V power supply input for the entire control circuit except the MOSFET drivers. Connect RC low-pass filter from V5IN to V5FILT.
V5IN	16	I	5-V power supply input for FET gate drivers. Internally connected to VBSTx by PN diodes.



FUNCTIONAL BLOCK DIAGRAM





DETAILED DESCRIPTION

PWM OPERATION

The main control loop of the switching mode power supply (SMPS) is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports a proprietary D-CAP Mode. D-CAP Mode uses an internal compensation circuit and is suitable for low external component-count configuration, with appropriate amount of ESR at the output capacitor(s). The output voltage is monitored at a feedback point voltage. The reference voltage at the feedback point is a combination of a fixed 0.750-V precision reference and a synchronized, precision 15-mV ramp signal. Lower output voltages in notebook systems (e.g., 1.05 V, 1.5 V) require extremely low output ripple. By providing a ramp signal, the TPS59124 is easier to use in low-output ripple systems. The combination of the precision ramp and reference yield an effective target reference of 0.758 V. The accuracy of this effective reference remains 1.3% over line and temperature.

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or becomes *ON* state. This MOSFET is turned off, or becomes *OFF* state, after the internal one-shot timer expires. This one shot is determined by the converter's input voltage, VIN, and the output voltage, VOUT, to keep the frequency fairly constant over the input voltage range; hence, it is called adaptive on-time control (see PWM Frequency and Adaptive On-time Control). The high-side MOSFET is turned on again when feedback information indicates insufficient output voltage, and inductor current information indicates a below-the-over-current limit condition. Repeating operation in this manner, the controller regulates the output voltage. The synchronous low-side MOSFET is turned on each *OFF* state to keep the conduction loss at a minimum. The low-side MOSFET is turned off when the inductor current information detects zero level. This enables seamless transition to the reduced frequency operation at light-load conditions so that high efficiency is kept over a broad range of load current.

LIGHT-LOAD CONDITION

TPS59124 automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increase of Vout ripple or load regulation. Detail operation is described as follows. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its *valley* touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when this zero inductor current is detected. As the load current is further decreased, the converter runs in discontinuous conduction mode and it takes longer and longer to discharge the output capacitor to the level that requires the next *ON* cycle. The *ON* time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light-load operation, $I_{OUT(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated in Equation 1.

$$I_{OUT(LL)} \approx \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

where

- *f* is the PWM switching frequency

Switching frequency versus output current in the light-load condition is a function of L, *f*, V_{IN}, and V_{OUT}, but it decreases almost proportional to the output current from the $I_{OUT(LL)}$ given in Equation 1.

It should be noted that in the PWM control path is a small ramp . This ramp is transparent in normal, continuous conduction mode and does not measurably affect the regulation voltage. However, in discontinuous, light-load mode, an upward shift in regulation voltage of about 0.75% will be observed. The variation of this shift minimally affects the reference tolerance. Therefore, the reference value in skip mode is 0.764 V ±1.3% over line and temperature.

DETAILED DESCRIPTION (continued)

LOW-SIDE DRIVER

The low-side driver is designed to drive high current low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistances, which are 4 Ω for V5IN to DRVLx, and 1 Ω for DRVLx to PGNDx. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. A 5-V bias voltage is delivered from V5IN supply. The instantaneous drive current is supplied by an input capacitor connected between V5IN and GND. The average drive current is equal to the gate charge at Vgs = 5 V times switching frequency. This gate drive current, as well as the high-side gate drive current times 5 V, makes the driving power that needs to be dissipated from TPS59124 package.

HIGH-SIDE DRIVER

The high-side driver is designed to drive high-current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, 5-V bias voltage is delivered from V5IN supply. The average drive current is also calculated by the gate charge at Vgs = 5 V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between VBSTx and LLx pins. The drive capability is represented by its internal resistances, which are 5 Ω for VBSTx to DRVHx and 1.5 Ω for DRVHx to LLx.

PWM FREQUENCY AND ADAPTIVE ON-TIME CONTROL

TPS59124 employs adaptive on-time control scheme and does not have a dedicated oscillator on board. However, the part runs with pseudo-constant frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The frequencies are set by TONSEL terminal connection as Table 1. The on-time is controlled inverse proportional to the input voltage and proportional to the output voltage so that the duty ratio is kept as V_{OUT}/V_{IN} technically with the same cycle time. Although the TPS59124 does not have a pin connected to V_{IN}, the input voltage is monitored at LLx pin during the *ON* state. This helps pin count reduction to make the part compact without sacrificing its performance.

Table 1. On-Time Selection Switching Frequencies

TONSEL CONNECTION	SWITCHING FREQUENCY (kHz)(1)	
	CH1	CH2
GND	240	300
FLOAT (Open)	300	360
V5FILT	360	420

(1) Frequencies are approximate.

SOFT START

The TPS59124 has an internal, 1.2-ms, voltage servo soft start for each channel. When the ENx pin becomes high, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start-up. As TPS59124 shares one DAC with both channels, if ENx pin is set to high while another channel is starting up, soft start is postponed until another channel soft start has completed. If both of EN1 and EN2 are set high at a same time, both channels start up at same time.

POWER GOOD

The TPS59124 has power-good output for both switcher channels. The power-good function is activated after soft start has finished. If the output voltage becomes within ±5% of the target value, internal comparators detect power good state and the power good signal becomes high after a 510-μs internal delay. During start-up, this internal delay starts after 1.7 times internal soft-start time to avoid a glitch of power-good signal. If the feedback voltage goes outside of ±10% of the target value, the power-good signal becomes low after 10-μs internal delay.

Also note that if the feedback voltage goes +10% above target value and the power-good signal flags low, then the loop attempts to correct the output by turning on the low-side driver (forced PWM mode). After the feedback voltage returns to be within +5% of the target value and the power-good signal goes high, the controller returns back to auto-skip mode.

DETAILED DESCRIPTION (continued)

OUTPUT DISCHARGE CONTROL

TPS59124 discharges the output when ENx is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). TPS59124 discharges outputs using an internal, 10-Ω MOSFET which is connected to VOx and PGNDx. The external low-side MOSFET is not turned on for the output discharge operation to avoid the possibility of causing negative voltage at the output. Output discharge time constant is a function of the output capacitance and the resistance of the internal discharge MOSFET. This discharge ensures that, on restart, the regulated voltage always starts from zero volts. In case a SMPS is restarted before discharge completion, discharge is terminated and the switching resumes after the reference level, ramped up by an internal DAC, comes back to the remaining output voltage.

CURRENT PROTECTION

TPS59124 has cycle-by-cycle over-current limiting control. The inductor current is monitored during the *OFF* state and the controller keeps the *OFF* state during the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS59124 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. TRIPx pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. TRIPx terminal sources 10-μA I_{TRIP} current and the trip level is set to the OCL trip voltage V_{TRIP} as shown in Equation 2.

$$V_{TRIP}\,(mV) = R_{TRIP}\,(k\Omega) \times 10\,(\mu A) \tag{2}$$

The trip level should be in the range of 30 mV to 200 mV over all operational temperatures. The inductor current is monitored by the voltage between PGNDx pin and LLx pin so that LLx pin should be connected to the drain terminal of the low-side MOSFET. I_{TRIP} has 4200 ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. PGNDx is used as the positive current sensing node so that PGNDx should be connected to the source terminal of the low-side MOSFET. As the comparison is done during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at over-current threshold, I_{OCL}, can be calculated as follows;

$$I_{OCL} = \left(\frac{V_{TRIP}}{R_{DS(on)}} + \frac{I_{RIPPLE}}{2} \right) = \frac{V_{TRIP}}{R_{DS(on)}} + \left(\frac{1}{2 \times L \times f} \right) \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{3}$$

In an over-current condition, the current to the load exceeds the current to the output capacitor; thus, the output voltage tends to fall off (droop). Eventually it crosses the undervoltage protection threshold and shuts down.

OVERVOLTAGE/UNDERVOLTAGE PROTECTION

TPS59124 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 115% of the target voltage, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

Also, the TPS59124 monitors VOx voltage directly and if it becomes greater than 5.75 V, the TPS59124 turns off the top MOSFET driver, and shuts off both drivers of the other channel.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 32 μs, TPS59124 latches OFF both top and bottom MOSFET drivers, and shuts off both drivers of the other channel. This function is enabled after 1.7 times soft-start delay time, approximately 2 ms, to ensure start-up properly.

UVLO PROTECTION

TPS59124 has V5FILT undervoltage lock-out protection (UVLO). When the V5FILT voltage is lower than UVLO threshold voltage, the TPS59124 is shut off. This is non-latch protection.

THERMAL SHUTDOWN

TPS59124 monitors its own temperature. If the temperature exceeds the threshold value (typically 160°C), the switchers are shut off as both DRVH and DRVL at low; the output discharge function is enabled. TPS59124 is shut off. This is non-latch protection.

TYPICAL CHARACTERISTICS

V5FILT SUPPLY CURRENT
vs
JUNCTION TEMPERATURE

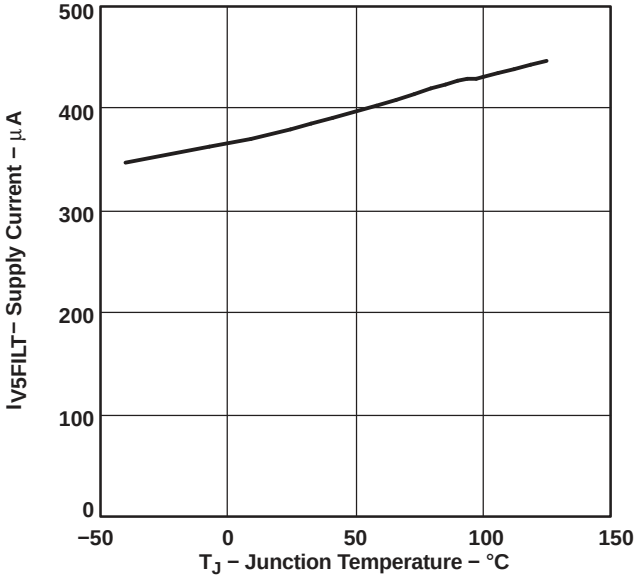


Figure 1.

V5FILT SHUTDOWN CURRENT
vs
JUNCTION TEMPERATURE

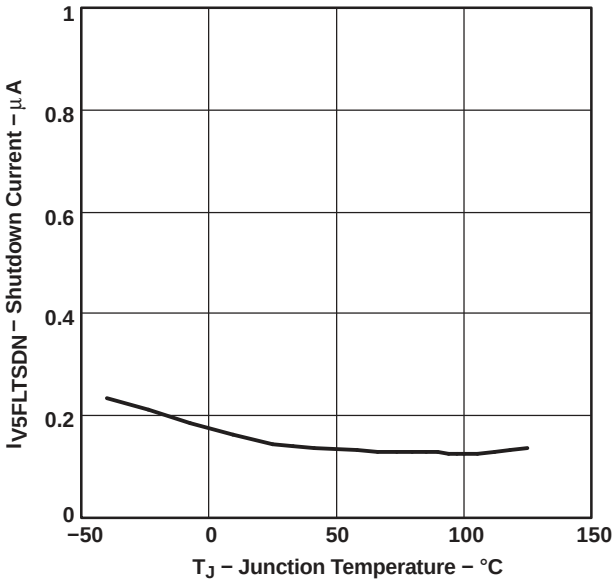


Figure 2.

V5IN SHUTDOWN CURRENT
vs
JUNCTION TEMPERATURE

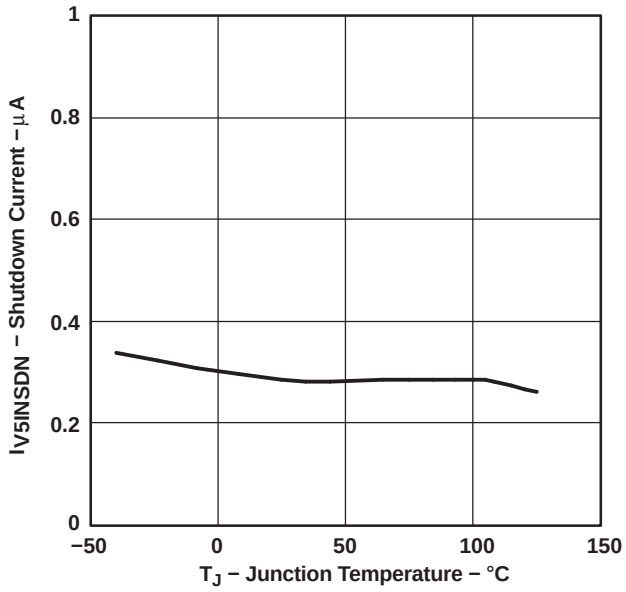


Figure 3.

TRIP SOURCE CURRENT
vs
JUNCTION TEMPERATURE

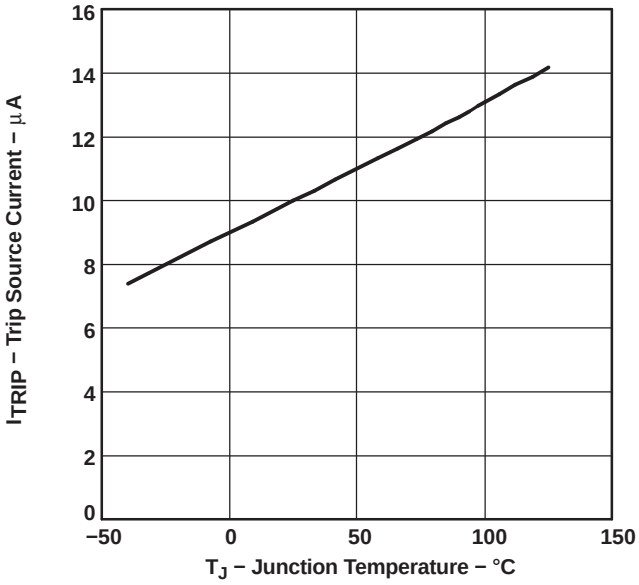


Figure 4.

TYPICAL CHARACTERISTICS (continued)

OVP/UVP THRESHOLD
vs
JUNCTION TEMPERATURE

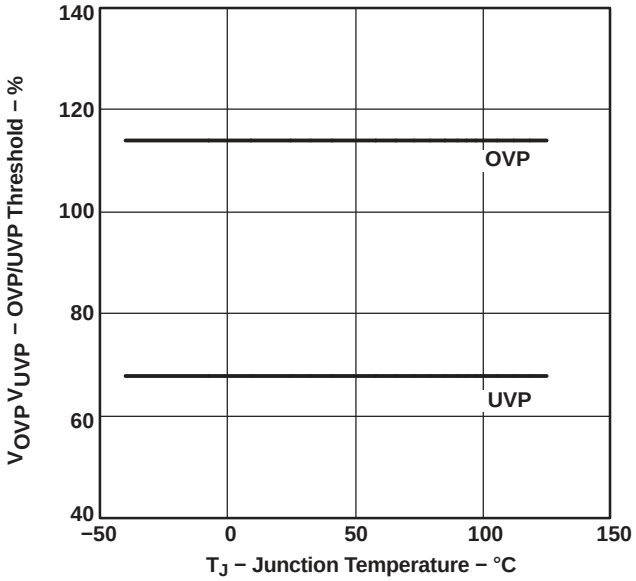


Figure 5.

SWITCHING FREQUENCY (SLOW)
vs
INPUT VOLTAGE

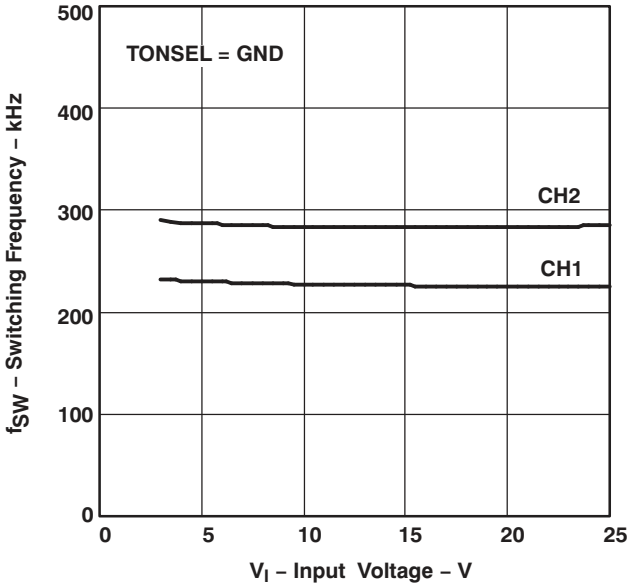


Figure 6. (1)

SWITCHING FREQUENCY (MED)
vs
INPUT VOLTAGE

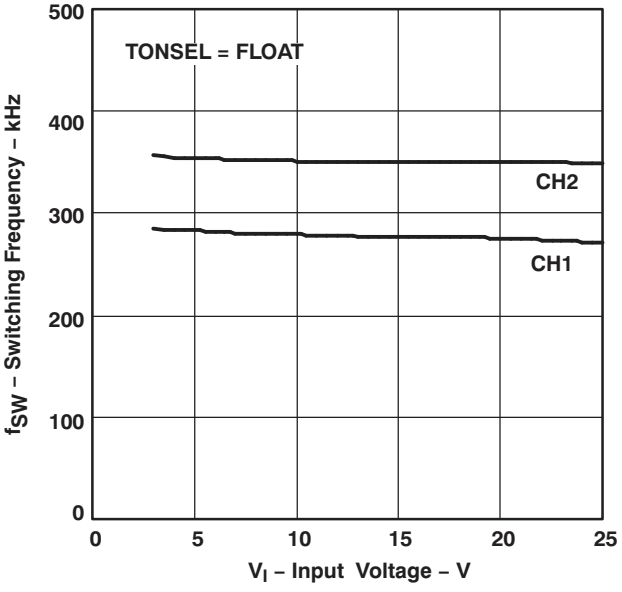


Figure 7.

SWITCHING FREQUENCY (FAST)
vs
INPUT VOLTAGE

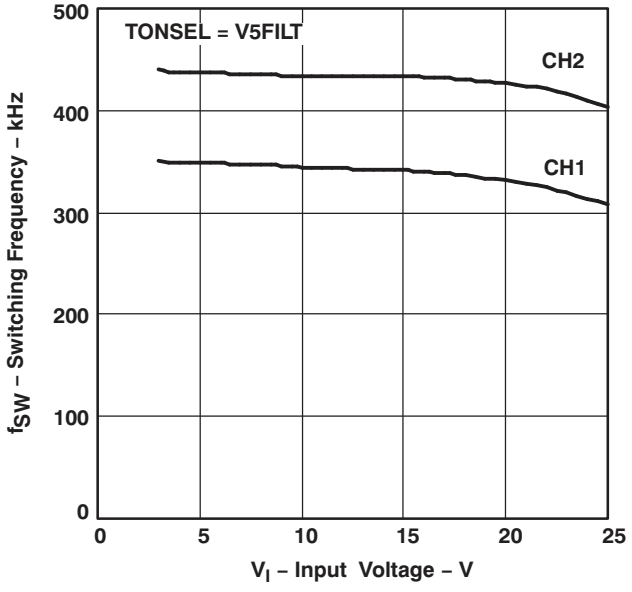


Figure 8.

(1) The data of Figure 6–Figure 8 are measured from the Typical Application Circuit of Figure 25 and Table 2.

TYPICAL CHARACTERISTICS (continued)

SWITCHING FREQUENCY (SLOW)
vs
OUTPUT CURRENT

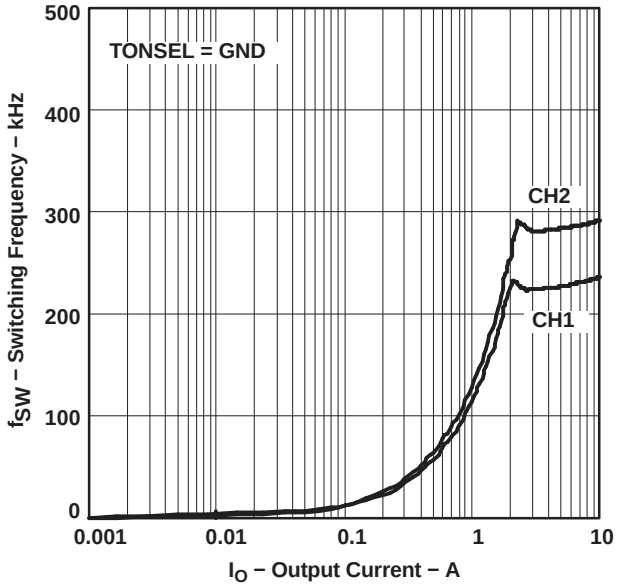


Figure 9. (2)

SWITCHING FREQUENCY (MED)
vs
OUTPUT CURRENT

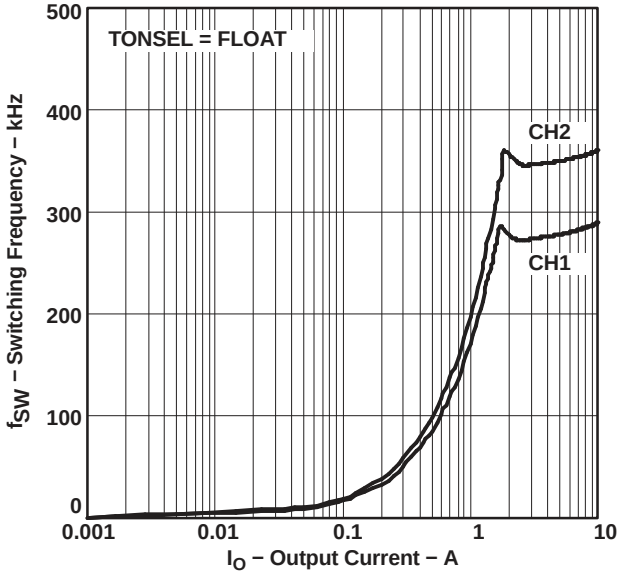


Figure 10.

SWITCHING FREQUENCY (FAST)
vs
OUTPUT CURRENT

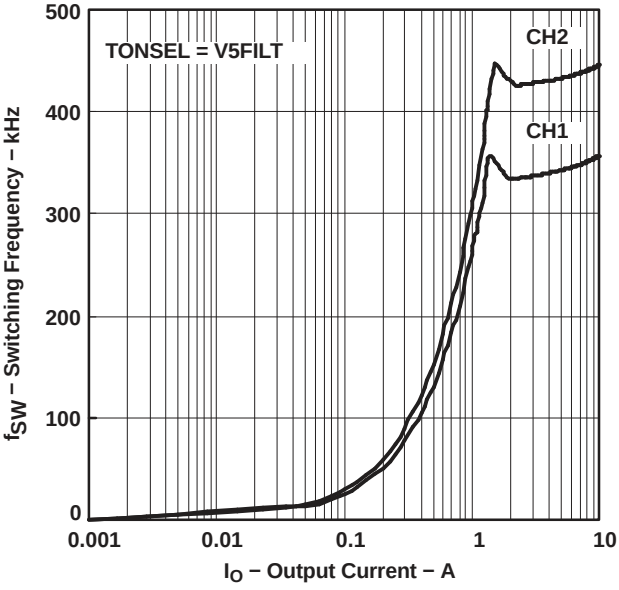


Figure 11.

1.05-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

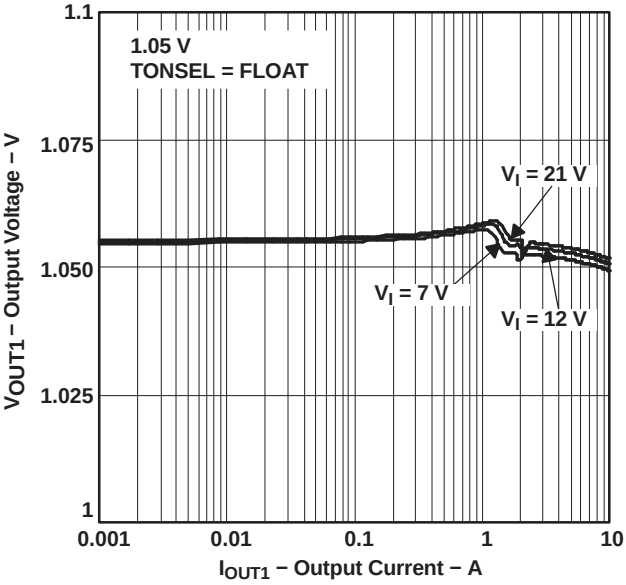


Figure 12.

(2) The data of Figure 9–Figure 12 are measured from the Typical Application Circuit of Figure 25 and Table 2.

TYPICAL CHARACTERISTICS (continued)

1.5-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

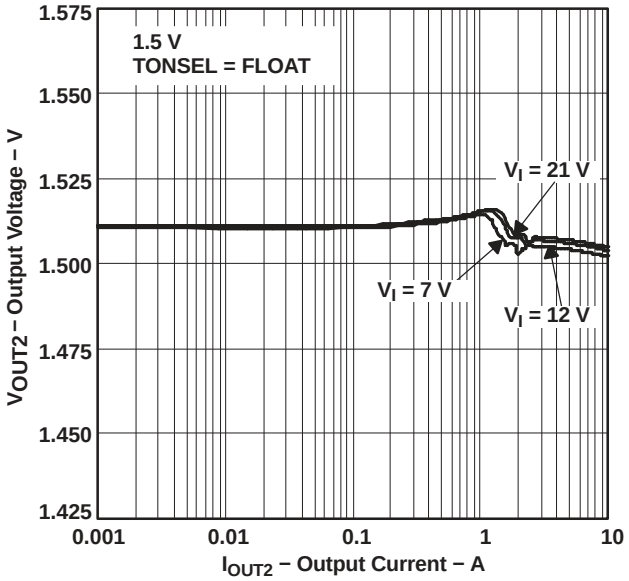


Figure 13. (3)

1.05-V OUTPUT VOLTAGE
vs
INPUT VOLTAGE

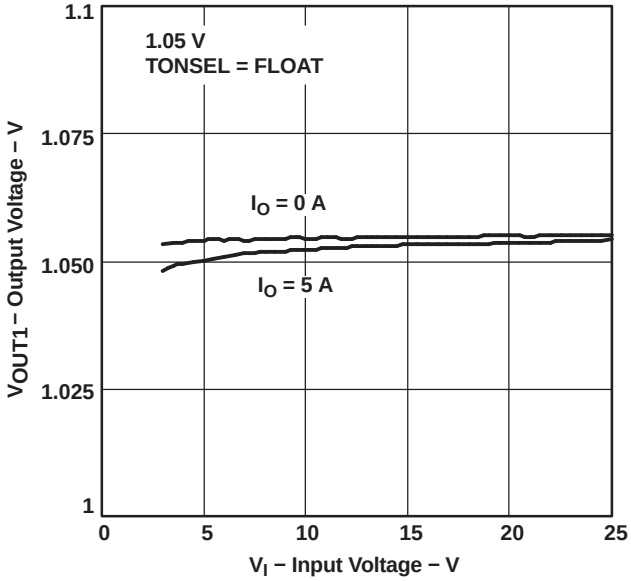


Figure 14.

1.5-V OUTPUT VOLTAGE
vs
INPUT VOLTAGE

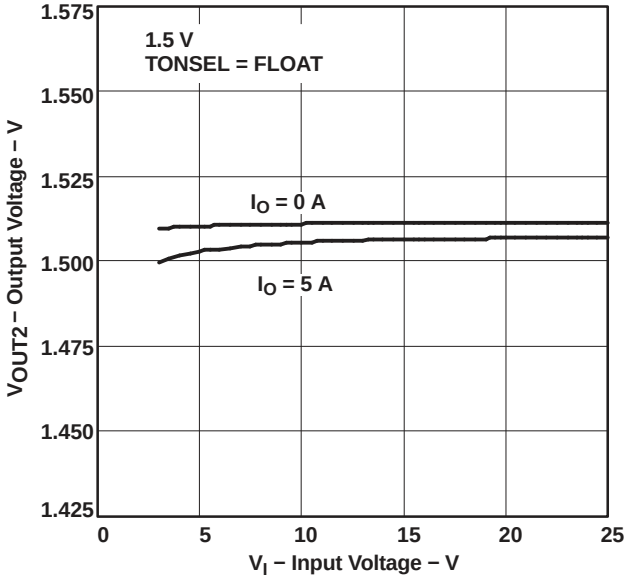


Figure 15.

1.05-V EFFICIENCY
vs
OUTPUT CURRENT

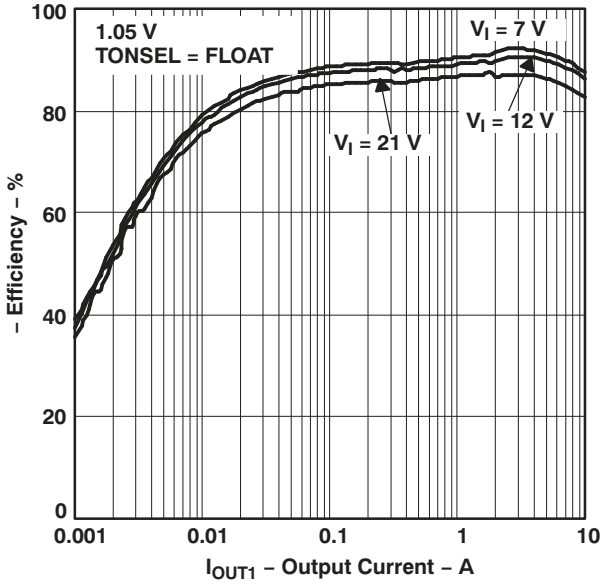


Figure 16.

(3) The data of Figure 13–Figure 16 are measured from the Typical Application Circuit of Figure 25 and Table 2

TYPICAL CHARACTERISTICS (continued)

1.5-V EFFICIENCY
vs
OUTPUT CURRENT

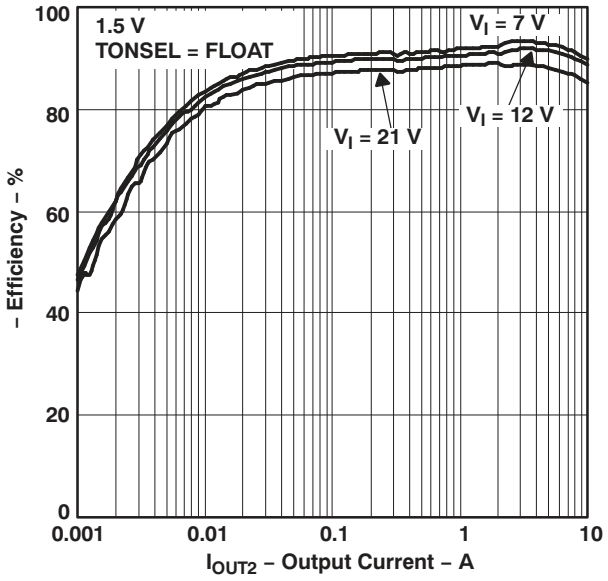
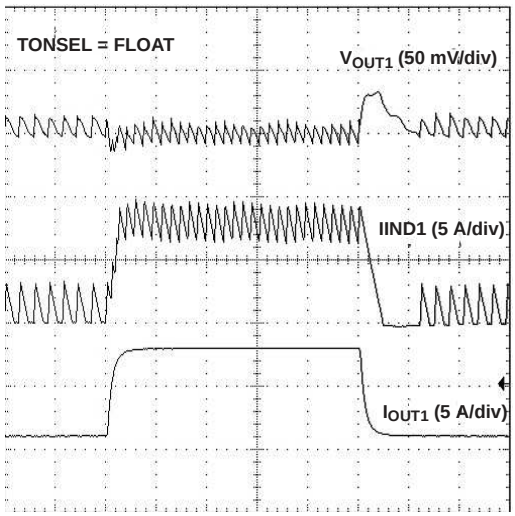


Figure 17. (4)

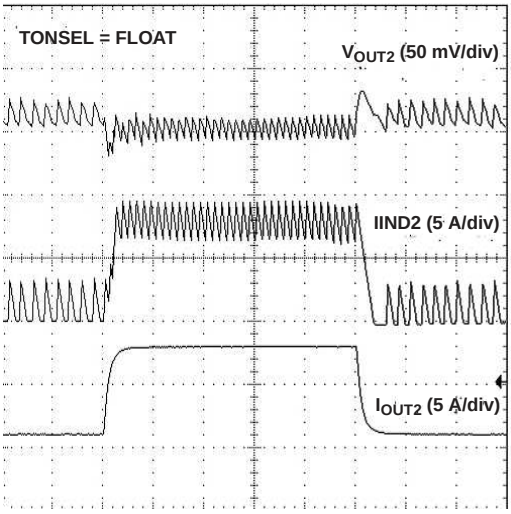
1.05-V LOAD TRANSIENT RESPONSE



t – Time – 20 μs/div

Figure 18.

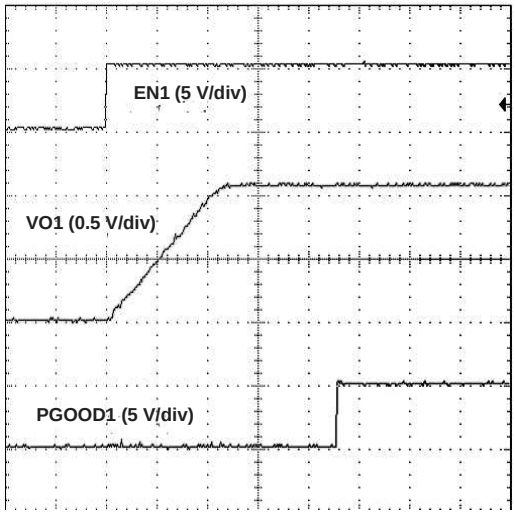
1.5-V LOAD TRANSIENT RESPONSE



t – Time – 20 μs/div

Figure 19.

1.05-V START-UP WAVEFORMS



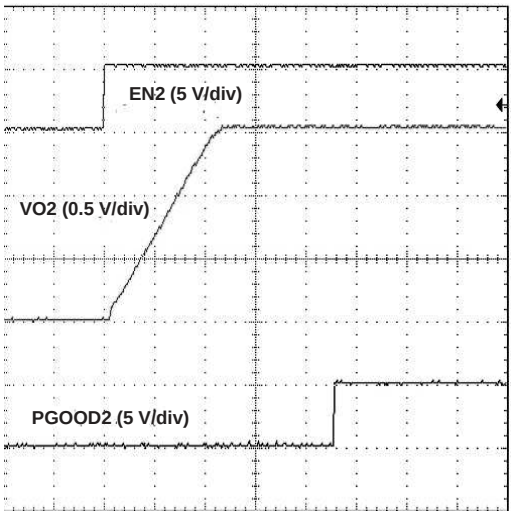
t – Time – 500 μs/div

Figure 20.

(4) The data of Figure 17–Figure 20 are measured from the Typical Application Circuit of Figure 25 and Table 2

TYPICAL CHARACTERISTICS (continued)

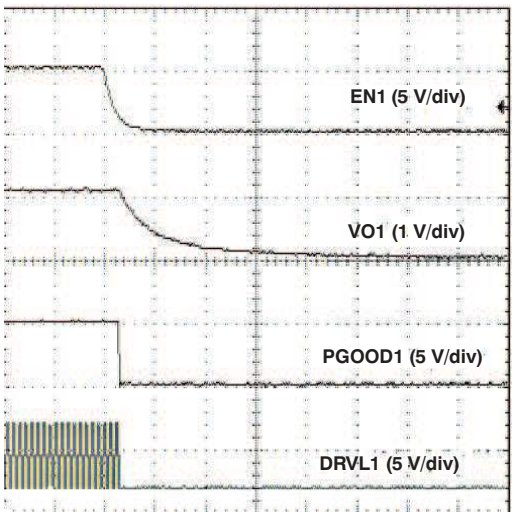
1.5-V START-UP WAVEFORMS



t – Time – 500 μs/div

Figure 21. (5)

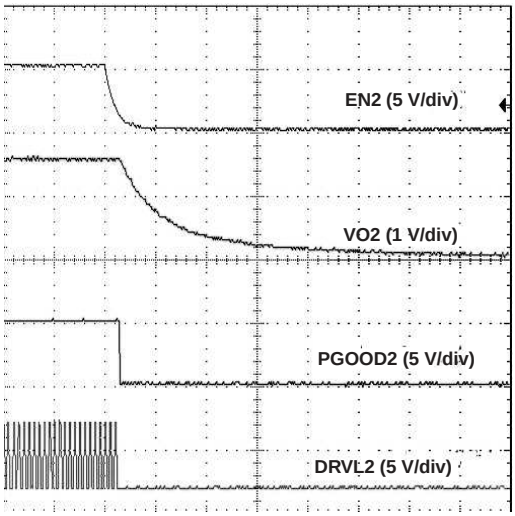
1.05-V DISCHARGE WAVEFORMS



t – Time –1 ms/div

Figure 22.

1.5-V DISCHARGE WAVEFORMS



t – Time – 1 ms/div

Figure 23.

(5) The data of Figure 21–Figure 23 are measured from the Typical Application Circuit of Figure 25 and Table 2

APPLICATION INFORMATION

LOOP COMPENSATION AND EXTERNAL PARTS SELECTION

A buck converter system using D-CAP Mode can be simplified as shown in Figure 24.

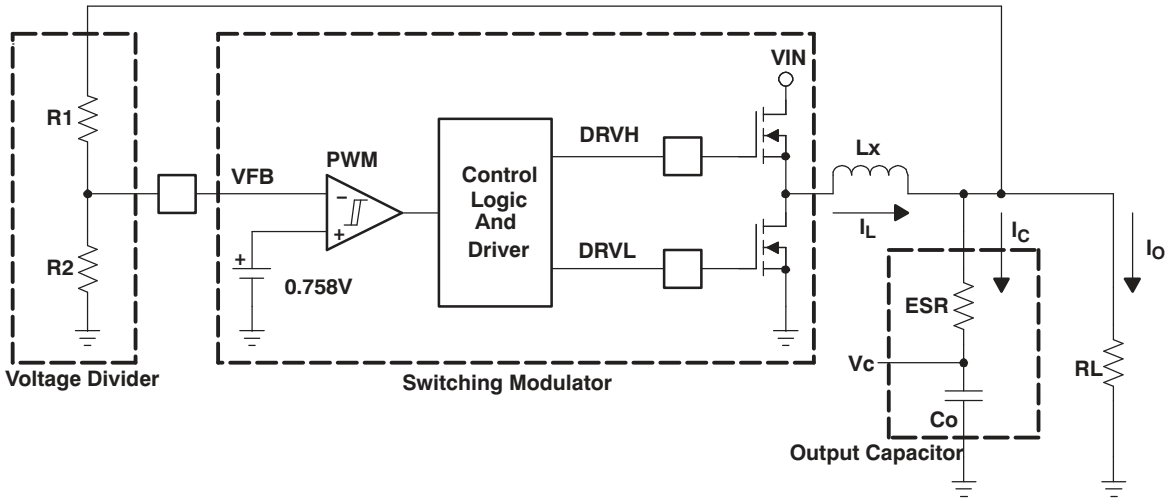


Figure 24. Simplifying the Modulator

The output voltage is compared with an internal reference voltage after divider resistors, R1 and R2. The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The DC output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increase.

For loop stability, the 0-dB frequency, f_0, defined in Equation 4 needs to be lower than 1/4 of the switching frequency.

$$f_O = \frac{1}{2\pi \times ESR \times Co} \le \frac{f_{SW}}{4} \tag{4}$$

Because f_0 is determined solely by the output capacitor's characteristics, the loop stability of D-CAP Mode is determined by the capacitor chemistry. For example, specialty polymer capacitors (SP-CAP) have output capacitance, C_{OUT} in the order of several 100 µF and ESR in range of 10 mΩ. These make f_0 in the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this operational mode.

Although D-CAP Mode provides many advantages such as ease-of-use, minimum external components configuration, and extremely short response time, a sufficient amount of feedback signal must be provided by an external circuit to reduce jitter level because there is no error amplifier in the loop. The required signal level is approximately 10 mV at the comparing point (VFB terminal). This gives V_{RIPPLE} at the output node as shown in Equation 5.

$$V_{RIPPLE} = \left(\frac{V_{OUT}}{0.758}\right) \times 10(mV) \tag{5}$$

The output capacitor ESR should meet this requirement.

The external components selection is much simpler in D-CAP Mode.

1. Determine the value of R1 and R2.

   Recommended R2 value is from 10 kΩ to 100 kΩ. Determine R1 using Equation 6.

$$R1 = \left(\frac{V_{OUT} + 0.758}{0.758} \right) \times R2 \tag{6}$$

2. Choose inductor.

   The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases the output ripple voltage, improves S/N ratio, and contributes to a stable operation.

$$L1 = \frac{1}{I_{IND(ripple)} \times f} \times \left(\frac{\left(V_{IN(max)} - V_{OUT} \right) \times V_{OUT}}{V_{IN(max)}} \right) = \frac{3}{I_{OUT(max)} \times f} \times \left(\frac{\left(V_{IN(max)} - V_{OUT} \right) \times V_{OUT}}{V_{IN(max)}} \right) \tag{7}$$

   The inductor also requires a low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 8.

$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{L \times f} \times \left(\frac{\left(V_{IN(max)} - V_{OUT} \right) \times V_{OUT}}{V_{IN(max)}} \right) \tag{8}$$

3. Choose output capacitor(s).

   Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine ESR to meet the required ripple voltage indicated previously. A quick approximation is shown in Equation 9.

$$ESR = \frac{V_{OUT} \times 0.01}{I_{IRIPPLE}} \approx \frac{V_{OUT}}{I_{OUT(max)}} \times 30\,(m\Omega) \tag{9}$$

LAYOUT CONSIDERATIONS

Certain points must be considered before starting a layout using the TPS59124.

- Connect RC low-pass filter from V5IN to V5FILT, 1-μF and 3.3-Ω are recommended. Place the filter capacitor close to the device, within 12 mm (0.5 inch) if possible.
- Connect the over-current setting resistors from TRIPx to GND, and as close as possible to the device. The trace from TRIPx to resistor, and resistor to GND, should avoid coupling to high-voltage switching node.
- The discharge path (VOx) should have a dedicated trace to the output capacitor(s), separate from the output voltage sensing trace. Use 1,5-mm (60 mils) or wider trace, with no loops. Tie the feedback-current-setting resistor (the resistor between VFBx to GND) close to the device's GND. The trace from this resistor to VFBx pin should be short and thin. Place on the component side and avoid vias between this resistor and the device.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0,65-mm (25 mils) or wider trace.
- All sensitive analog traces and components such as VOx, VFBx, GND, ENx, PGOODx, TRIPx, V5FILT, and TONSEL should be placed away from high-voltage switching nodes such as LLx, DRVLx, DRVHx, or VBSTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Gather ground terminal of VIN capacitor(s), Vout capacitor(s), and source of low-side MOSFETs as close as possible. GND (signal ground) and PGNDx (power ground) should be connected strongly together near the device. PCB trace defined as LLx node, which connects to source of high-side MOSFET, drain of low-side MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
- In order to effectively remove heat from the package, prepare thermal land and solder to the package's thermal pad (PowerPAD™). Two by two or more vias with a 0,33-mm (13 mils) diameter connected from the thermal land to the internal ground plane should be used to help dissipation. Do **NOT** connect PGNDx to this thermal land underneath the package.

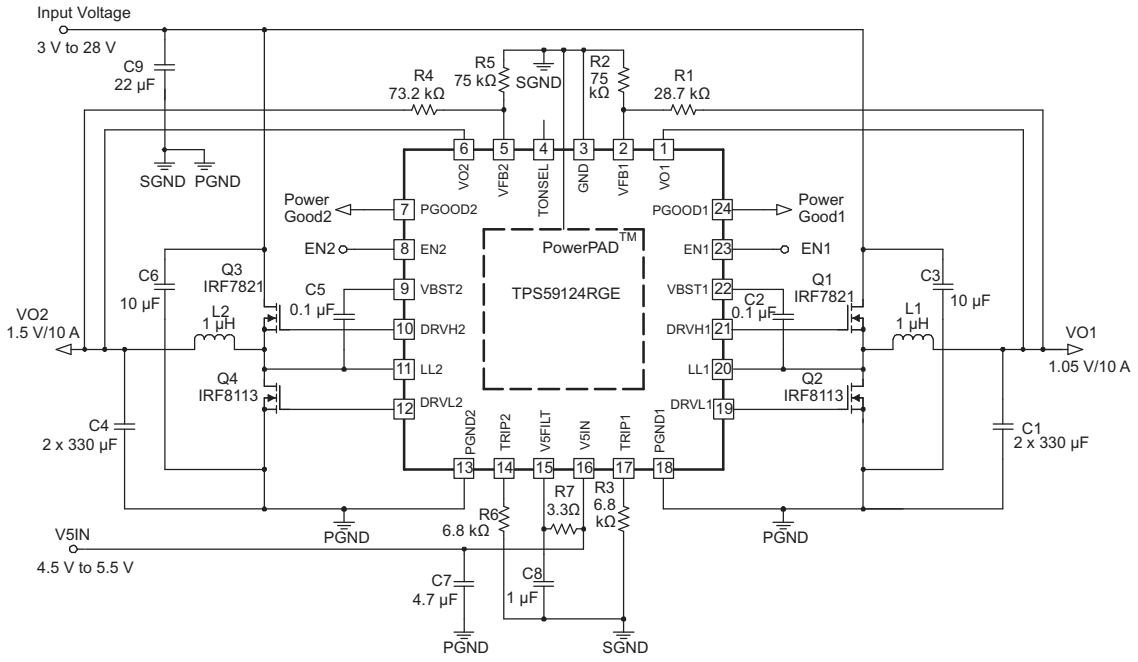


Figure 25. Typical Application Circuit

Table 2. Typical Application Circuit Components

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C1	330 µF, 2.5 V, 15 mΩ	SANYO	2R5TPE330MF
C4	330 µF, 2.5 V, 18 mΩ	SANYO	2R5TPE330MI
L1, L2	1 µH, 2 mΩ	TOKO	FDA1254-1R0M
C3, C6	10 µF, 25 V	TDK	C3225X5R1E106
Q1, Q3	30 V, 13 mΩ	International Rectifier	IRF7821
Q2, Q4	30 V, 7 mΩ	International Rectifier	IRF8113

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS59124RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 59124	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

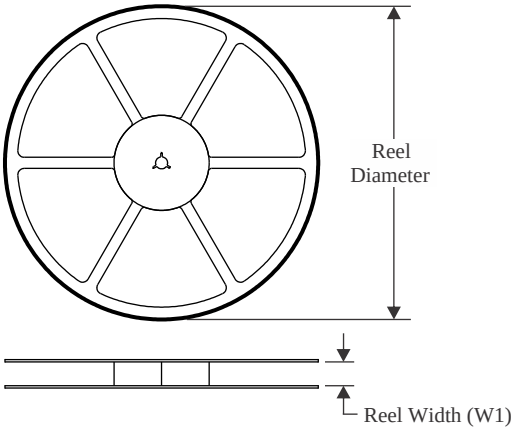
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

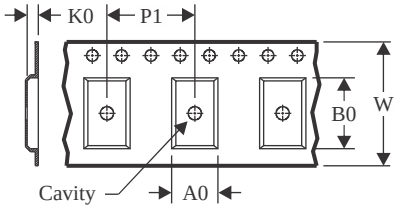
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

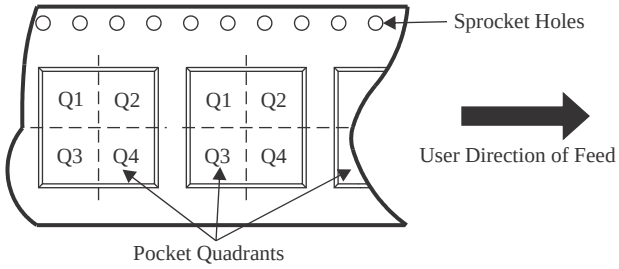


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

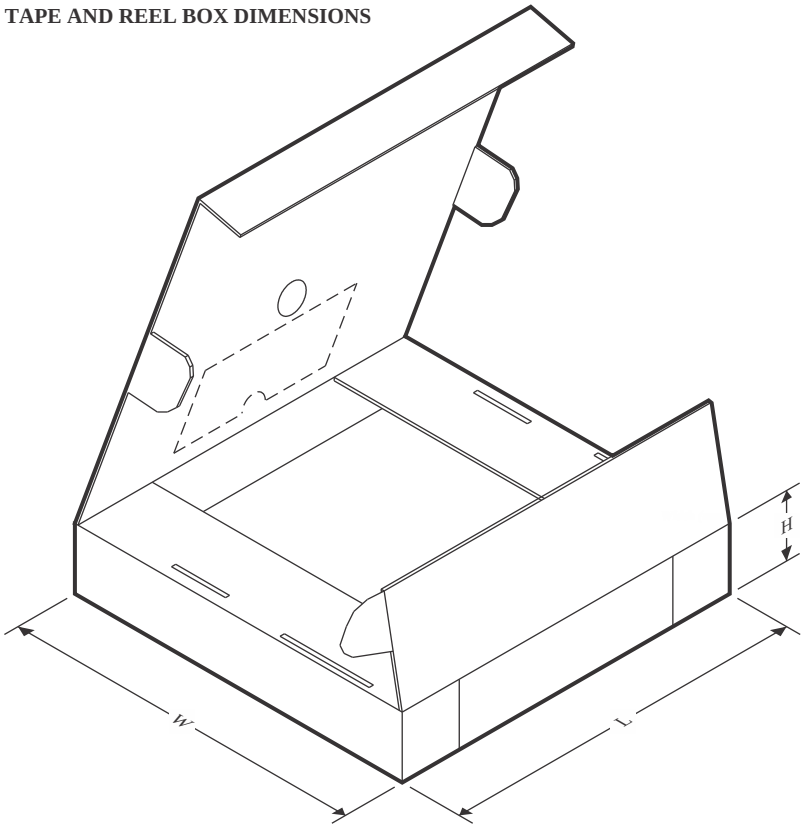
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS59124RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



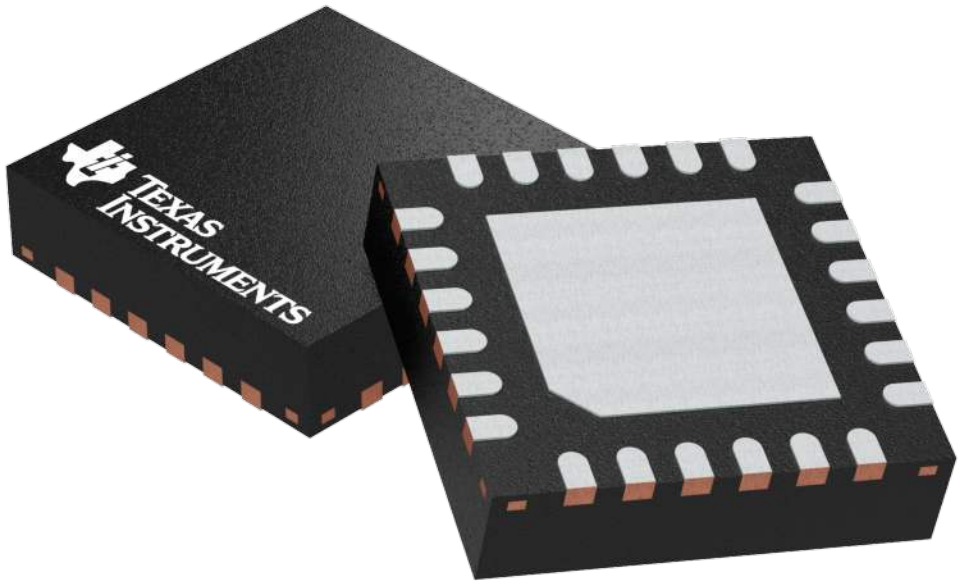
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS59124RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



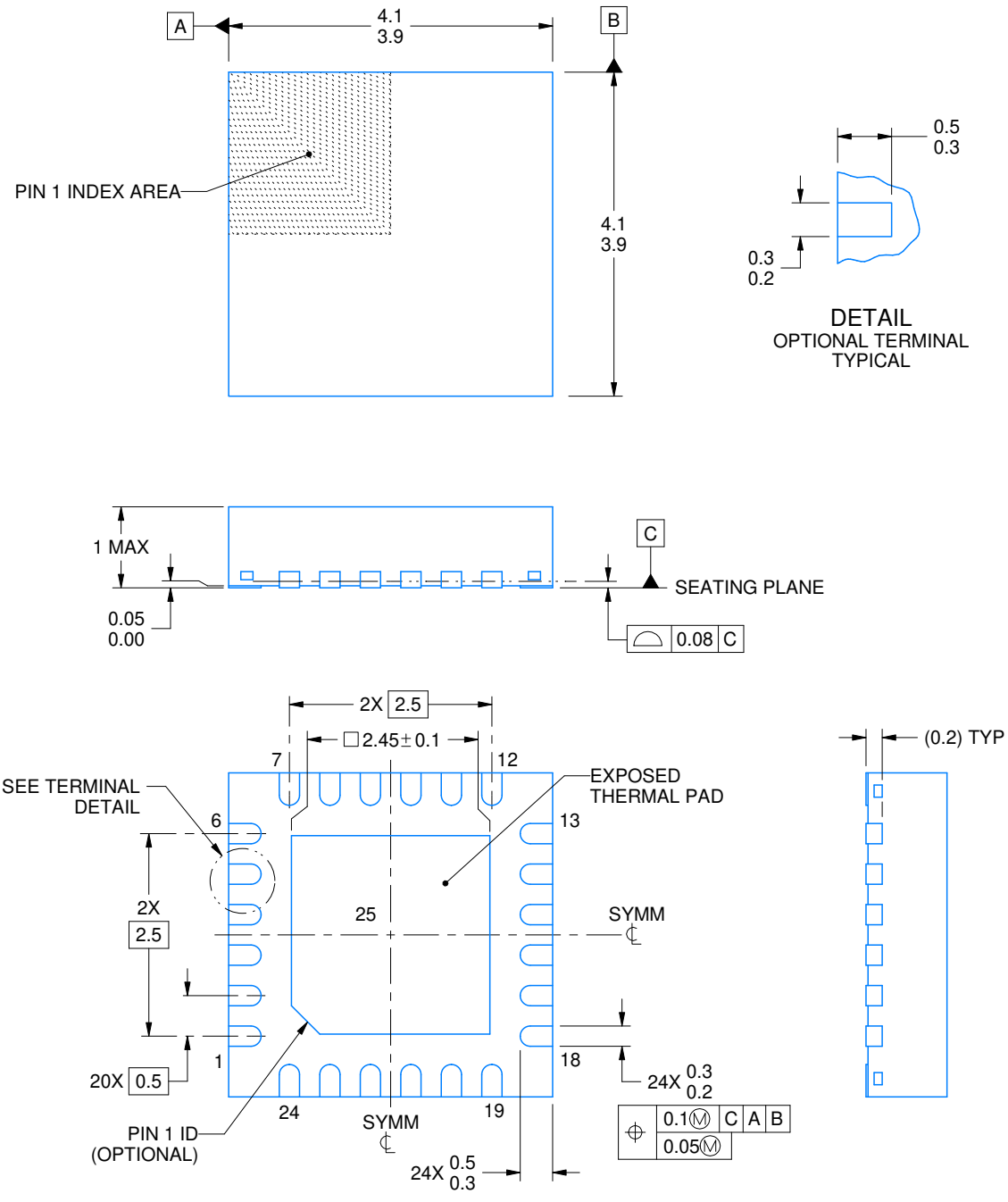
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024B

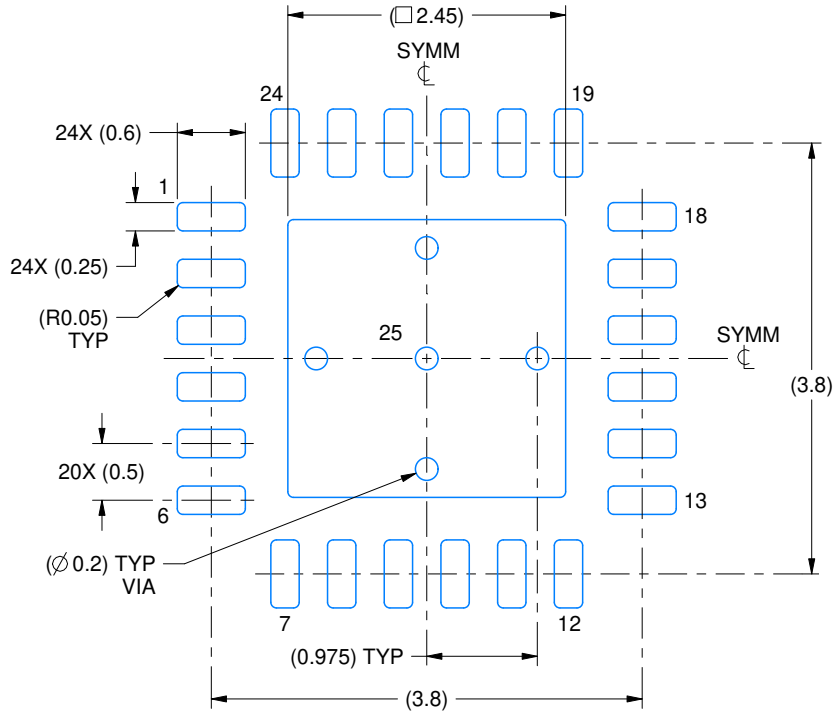
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

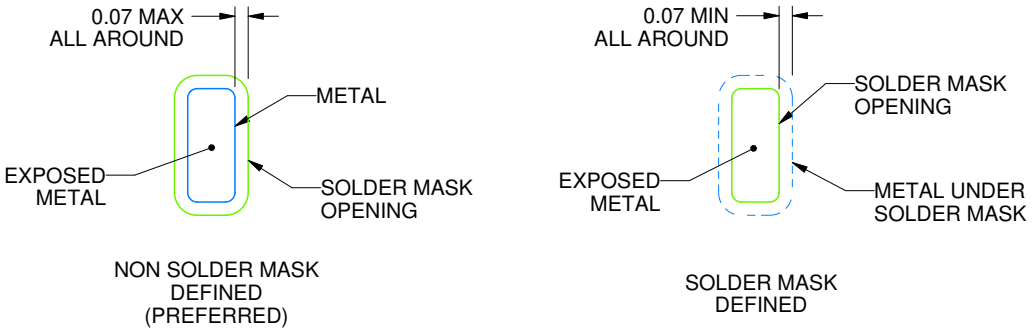


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

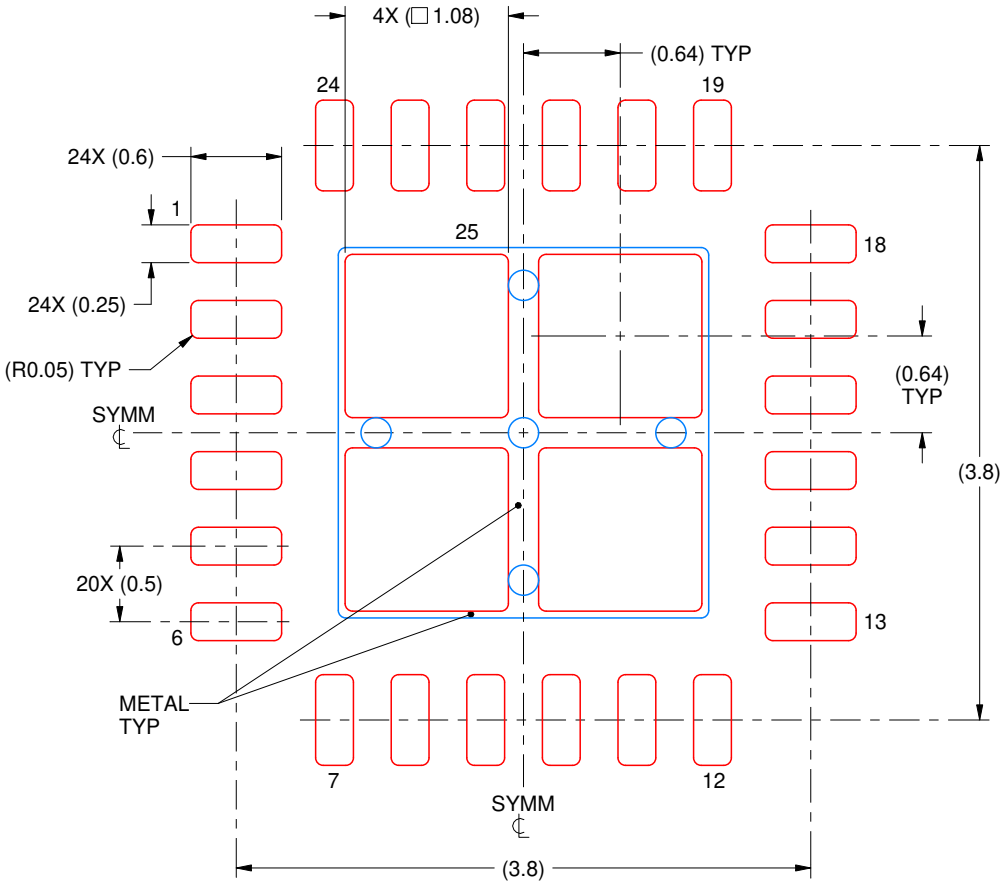
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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