



DM7546/DM8546 TRI-STATE® 8-Bit Universal I/O Shift Registers

General Description

These circuits are TRI-STATE, 8-bit, edge-triggered, universal shift registers which are capable of operating in any of the following modes: shift left, shift right, parallel load, or inhibit. Since the clock is edge-triggered, the control lines which determine the mode of operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Absolute Maximum Ratings (Note 1)

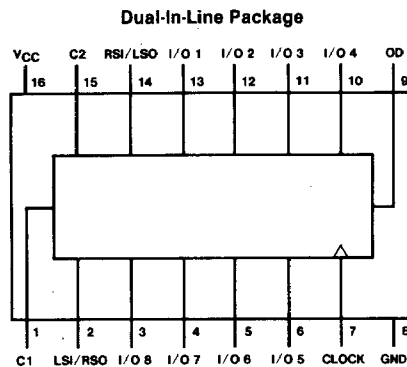
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	- 65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Features

- Positive-edge triggered clock
- "Do nothing" state without gating the clock
- Both parallel and serial data lines are TRI-STATE
- High impedance state does not impede shift mode with parallel outputs

Connection Diagram



TL/F/6587-1

7546 (J)

8546 (N)

Recommended Operating Conditions

Symbol	Parameter	DM7546			DM8546			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			-2			-5.2	mA
I _{OL}	Low Level Output Current			16			16	mA
f _{CLK}	Clock Frequency	0		15	0		15	MHz
t _w	Clock Pulse Width	18	12		18	12		ns
t _{SETUP (HIGH)}	Serial Data	C _L = 50 pF R _L = 400Ω	38	25		38	25	ns
t _{SETUP (HIGH)}	Parallel Data		33	22		33	22	ns
t _{SETUP (LOW)}	Serial Data		21	14		21	14	ns
t _{SETUP (LOW)}	Parallel Data		18	12		18	12	ns
t _{HOLD (HIGH)}	Serial Data		0	-11		0	-11	ns
t _{HOLD (HIGH)}	Parallel Data		0	-11		0	-11	ns
t _{HOLD (LOW)}	Serial Data		0	-22		0	-22	ns
t _{HOLD (LOW)}	Parallel Data		0	-21		0	-21	ns
SETUP AND HOLD TIMES BETWEEN CHANGES IN MODE CONTROL AND CLOCKING								
t _{SETUP}	Parallel Load to Right Shift	C _L = 50 pF R _L = 400Ω	32	21		32	21	ns
t _{SETUP}	Parallel Load to Left Shift		40	27		40	27	ns
t _{SETUP}	Right Shift to Parallel Load		60	40		60	40	ns
t _{SETUP}	Left Shift to Parallel Load		53	35		53	35	ns
t _{SETUP}	Right Shift to Left Shift		33	21		33	21	ns
t _{SETUP}	Left Shift to Right Shift		56	37		56	37	ns
t _{SETUP}	Inhibit to Right Shift		57	38		57	38	ns
t _{SETUP}	Inhibit to Left Shift		65	43		65	43	ns
t _{SETUP}	Right Shift to Inhibit		50	33		50	33	ns
t _{SETUP}	Left Shift to Inhibit		50	32		50	32	ns
t _{HOLD}	Parallel Load to Right Shift		9	6		9	6	ns
t _{HOLD}	Parallel Load to Left Shift		6	4		6	4	ns
t _{HOLD}	Right Shift to Parallel Load		0	-13		0	-13	ns
t _{HOLD}	Left Shift to Parallel Load		0	-46		0	-46	ns
t _{HOLD}	Right Shift to Left Shift		0	-10		0	-10	ns
t _{HOLD}	Left Shift to Right Shift		0	-23		0	-23	ns
t _{HOLD}	Inhibit to Right Shift		0	-18		0	-18	ns
t _{HOLD}	Inhibit to Left Shift		0	-16		0	-16	ns
t _{HOLD}	Right Shift to Inhibit		0	-12		0	-12	ns
t _{HOLD}	Left Shift to Inhibit		0	-29		0	-29	ns
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -12 \text{ mA}$			-1.5	V	
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	2.4			V	
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$			0.4	V	
I_I	Input Current@ Max Input Voltage	$V_{CC} = \text{Max}$, $V_I = 5.5\text{V}$			1	mA	
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.4\text{V}$	C2		80	μA	
			Other		40		
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4\text{V}$	C2		-3.2	mA	
			Other		-1.6		
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	$V_{CC} = \text{Max}$, $V_O = 2.4\text{V}$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$			40	μA	
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	$V_{CC} = \text{Max}$, $V_O = 0.4\text{V}$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$			-40	μA	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	DM75	-30		-70	mA
			DM85	-30		-70	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$	DM75		80	115	mA
			DM85		80	125	

Note 1: All typicals are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

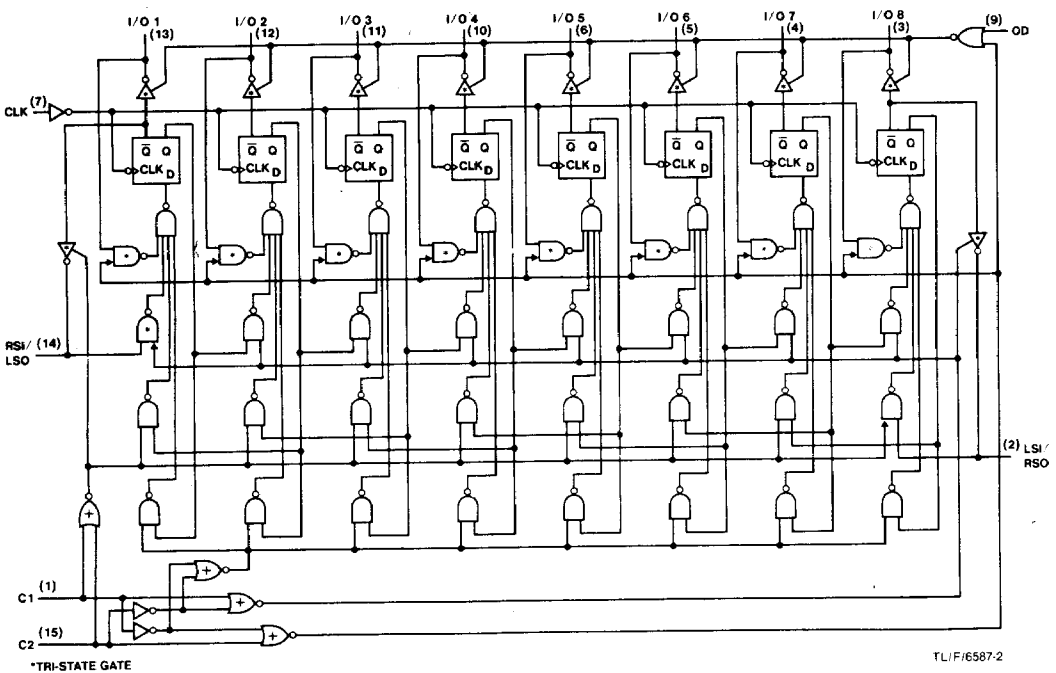
Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5\text{ pF}$			$C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Typ	Max	
t_{MAX} Maximum Clock Frequency					15	22		MHz
t_{PLH} Propagation Delay Time Low to High Level Output						16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output						27	40	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Q					22	33	ns
t_{PZH} Output Enable Time to High Level Output	Mode Control (C1/C2) to Q					13	20	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Q					18	27	ns
t_{PZL} Output Enable Time to Low Level Output	Mode Control (C1/C2) to Q					15	23	ns
t_{PHZ} Output Disable Time from High Level Output	Output Control to Q		5	8				ns
t_{PHZ} Output Disable Time from High Level Output	Mode Control (C1/C2) to Q		9	14				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Control to Q		16	24				ns
t_{PLZ} Output Disable Time from Low Level Output	Mode Control (C1/C2) to Q		17	26				ns

Function Table

OD	C1	C2	Mode of Operation	State of Parallel I/O	State of Serial I/O	
					RSI/LSO	LSI/RSO
L	H	H	Inhibit	QOUT	Hi-Z*	Hi-Z*
H	H	H	Inhibit	Hi-Z*	Hi-Z*	Hi-Z*
X	H	L	Parallel Load	Data In	Hi-Z*	Hi-Z*
L	L	H	Right Shift	QOUT	Data In	QOUT 8
H	L	H	Right Shift	Hi-Z*	Data In	QOUT 8
L	L	L	Left Shift	QOUT	QOUT 1	Data In
H	L	L	Left Shift	Hi-Z*	QOUT 1	Data In

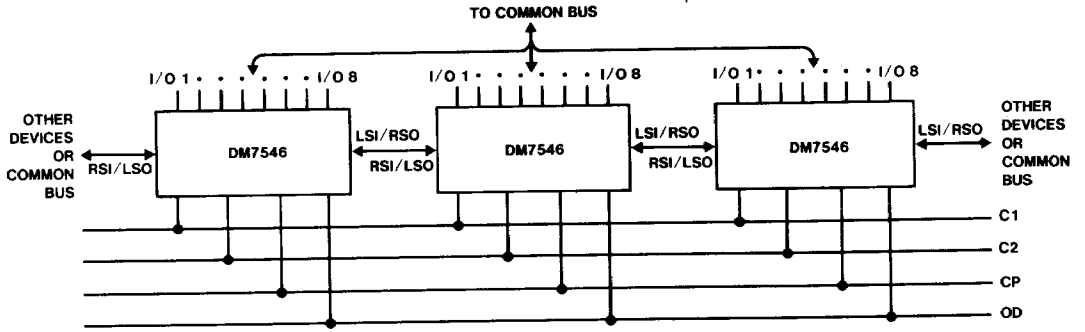
OD = Output Disable (C1, C2 = Mode Controls)
 *Both Input and Output of the I/O pin are in the high impedance state.

Logic Diagram



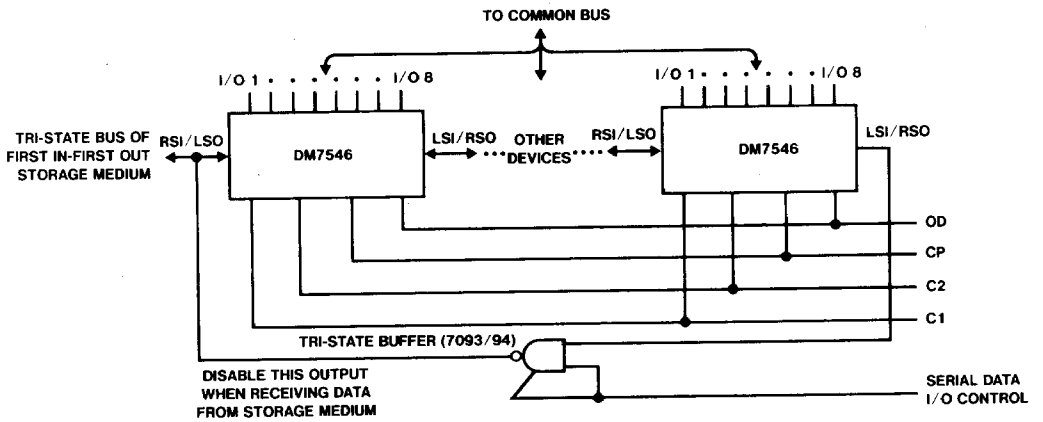
Typical Applications

Cascading Devices



TL/F/6587-3

Serial Data Transfer to a First In-First Out Storage Medium



TL/F/6587-4

Typical Applications (Continued)

Typical Parallel Load, Right Shift, Left Shift and Inhibit Sequences

