REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R222-92.	92-06-19	M. A. FRYE
B	Correction made to the title block on sheet 1. Drawing updated to reflect current requirements. -rrp	03-03-03	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
Rick C. Officer

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COLUMBUS, OHIO 43216
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles E. Besore

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
91-04-29

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, 8-BIT A/D PERIPHERAL WITH SERIAL CONTROL, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-90845**

SHEET 1 OF 13

DSCC FORM 2233
APR 97

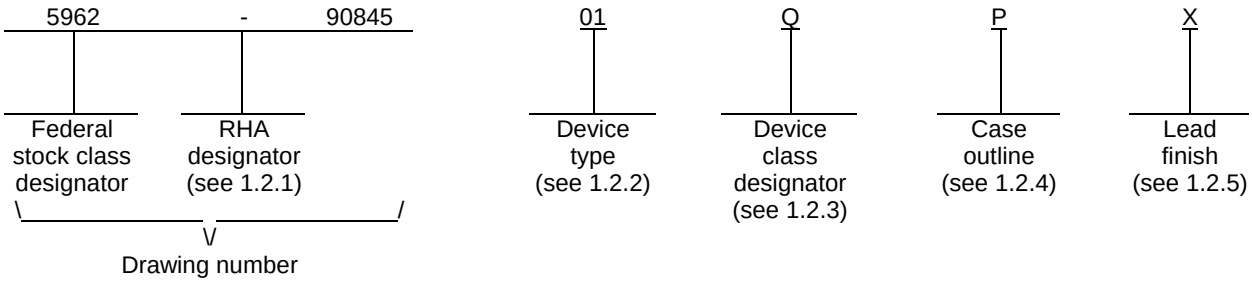
5962-E260-03

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Input/output clock frequency
01	TLC548M	8-bit analog-to-digital peripheral with serial control	2.048 MHz
02	TLC549M	8-bit analog-to-digital peripheral with serial control	1.1 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	+6.5 V 2/
Input voltage range at any input	-0.3 V to V_{CC} + 0.3 V
Output voltage range	-0.3 V to V_{CC} + 0.3 V
Peak input current range (any input)	±10 mA
Peak total input current range (all inputs)	±30 mA
Storage temperature range	-65°C to +150°C
Case temperature for 60 seconds, case 2	+260°C
Lead temperature soldering, 1.6 mm (0.0625) from case for 60 seconds:	
Case P	+300°C
Power dissipation (P_D), ($T_A \leq +25°C$): 3/	
Case P	1050 mW
Case 2	1375 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case P	110°C/W
Case 2	1375°C/W
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4 V minimum, 6 V maximum
Positive reference voltage (V_{REF+})	2.5 V minimum, V_{CC} + 0.1 V maximum 4/
Negative reference voltage (V_{REF-})	-0.1 V minimum, 2.5 V maximum 4/
Differential reference voltage (V_{REF+}), (V_{REF-})	1 V minimum, V_{CC} + 0.2 V maximum 4/
Analog input voltage	0 V minimum, V_{CC} maximum 4/
High level control input voltage (V_{IH})	2 V minimum 5/
Low level control input voltage (V_{IL})	0.8 V maximum 5/
Input/output clock frequency $f_{CLK(I/O)}$: 5/	
Device type 01	0 MHz minimum, 2.048 MHz maximum
Device type 02	0 MHz minimum, 1.1 MHz maximum
Input/output clock high $t_{WH(I/O)}$: 5/	
Device type 01	200 ns minimum
Device type 02	404 ns minimum
Input/output clock low $t_{WL(I/O)}$: 5/	
Device type 01	200 ns minimum
Device type 02	404 ns minimum
Duration of $\overline{CS}$ input high state during conversion $t_{WH(CS)}$	17 ∝s minimum 4/ 5/
Setup time, $\overline{CS}$ low before first I/O clock $t_{SU(CS)}$	1.4 ∝s minimum 5/ 6/
Ambient operating free-air temperature (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltage values are with respect to network ground terminal with the REF- and GND terminal connected together.

3/ Derate 8.4 mW/°C above T_A = +25°C for case P and derate 11.0 mW/°C above T_A = +25°C for case 2.

4/ Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF- convert to all zeros (00000000). For proper operation, the positive reference voltage V_{REF+} must be at least 1 V greater than the negative voltage V_{REF-}. In addition, unadjusted errors may increase as the differential reference voltage V_{REF+} - V_{REF-} falls below 4.75 V.

5/ V_{CC} = 4.75 V to 5.5 V

6/ To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after $\overline{CS}$ falling edge before responding to control input signals. This $\overline{CS}$ setup time is given by the t_{EN} and $t_{SU(CS)}$ specifications.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.75 V, I_{OH} = -360 ∝A	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.75 V, I_{OL} = 3.2 mA	1, 2, 3	All		0.4	V
Off state (high impedance state) output current	I_{OZ}	$V_O = V_{CC}$, V_{CC} = 5.5 V, $\overline{CS}$ at V_{CC}	1, 2, 3	All		10	∝A
		V_O = 0, V_{CC} = 5.5 V, $\overline{CS}$ at V_{CC}				-10	
High level input current, control inputs	I_{IH}	$V_I = V_{CC}$ = 5.5 V	1, 2, 3	All		2.5	∝A
Low level input current, control inputs	I_{IL}	V_I = 0, V_{CC} = 5.5 V	1, 2, 3	All		-2.5	∝A
Analog channel "ON" state input current, during sample cycle	$I_{I(ON)}$	Analog input at V_{CC}, V_{CC} = 5.5 V	1, 2, 3	All		1	∝A
		Analog input at 0 V, V_{CC} = 5.5 V				-1	
Operating supply current	I_{CC}	V_{CC} = 5.5 V, $\overline{CS}$ at 0 V	1, 2, 3	All		3	mA
Supply and reference current	$I_{CC}+I_{REF}$	$V_{REF+} = V_{CC}$ = 5.5 V	1, 2, 3	All		3.25	mA
Linearity error 1/	E_L		1, 2, 3	All		±0.5	LSB
Zero error 2/	E_0		1, 2, 3	All		±0.5	LSB
Full scale error 2/	E_{FS}		1, 2, 3	All		±0.5	LSB
Total unadjusted error 3/	E_U		1, 2, 3	All		±0.5	LSB
Input capacitance	C_{IN}	Analog inputs, see 4.4.1c	4	All		55	pF
		Control inputs, see 4.4.1c				15	
Conversion time	t_{CONV}	See figure 2	9, 10, 11	All		17	∝s
Total access and conversion time	t_{AC}	See figure 2	9, 10, 11	01		22	∝s
				02		25	
Channel acquisition time (sample cycle)	t_{ACQ}	See figure 2	9, 10, 11	All		4	I/O clock cycle
Time output data remains valid after I/O clock falling edge	t_V	V_{CC} = 5.0 V	9, 10, 11	All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time to data output valid	t_D	I/O clock falling edge, V_{CC} = 5.0 V	9, 10, 11	01		300	ns
				02		400	
Output enable time	t_{EN}	V_{CC} = 5.0 V, See figures 2 and 3	9, 10, 11	All		1.4	∝s
Output disable time	t_{DIS}	V_{CC} = 5.0 V, See figures 2 and 3	9, 01, 11	All		150	ns
Data bus rise time	$t_{R(bus)}$	V_{CC} = 5.0 V, See figures 2 and 3	9, 10, 11	All		300	ns
Data bus fall time	$t_{F(bus)}$	V_{CC} = 5.0 V, See figures 2 and 3	9, 10, 11	All		300	ns

1/ Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
2/ Zero error is the difference between 00000000 and the converted output for zero input voltage; full scale error is the difference between 11111111 and the converted output for full scale input voltage.
3/ Total unadjusted error is the sum of linearity, zero, and full scale errors.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

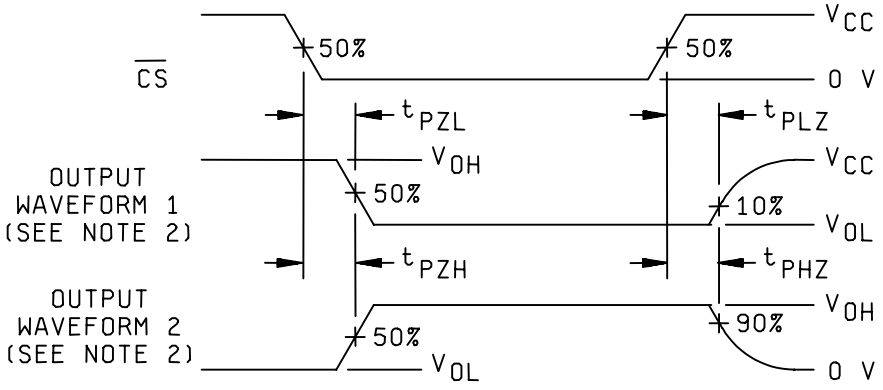
3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

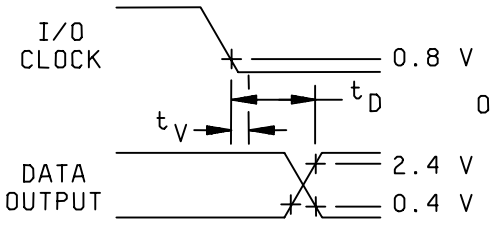
3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

Device types	01 and 02	
Case outlines	P	2
Terminal number	Terminal symbol	
1	REF+	NC
2	ANALOG IN	REF+
3	REF-	NC
4	GND	NC
5	$\overline{CS}$	ANALOG IN
6	DATA OUT	NC
7	I/O CLOCK	REF-
8	V_{CC}	NC
9	----	NC
10	----	GND
11	----	NC
12	----	$\overline{CS}$
13	----	NC
14	----	NC
15	----	DATA OUT
16	----	NC
17	----	I/O CLOCK
18	----	NC
19	----	NC
20	----	V_{CC}

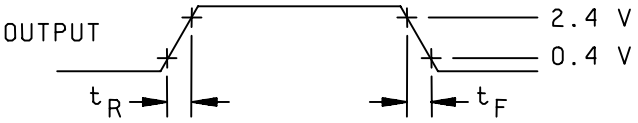
FIGURE 1. Terminal connections.



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES
SEE NOTE 1



VOLTAGE WAVEFORM FOR
DELAY TIMES

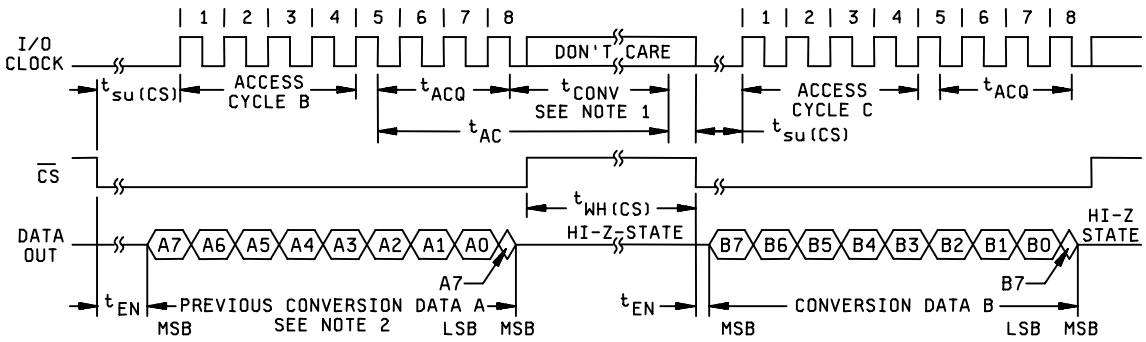


VOLTAGE WAVEFORM FOR
RISE AND FALL TIMES

NOTES:

1. $t_{EN} = t_{PZH}$ or t_{PZL}, $t_{DIS} = t_{PHZ}$ or t_{PLZ}.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

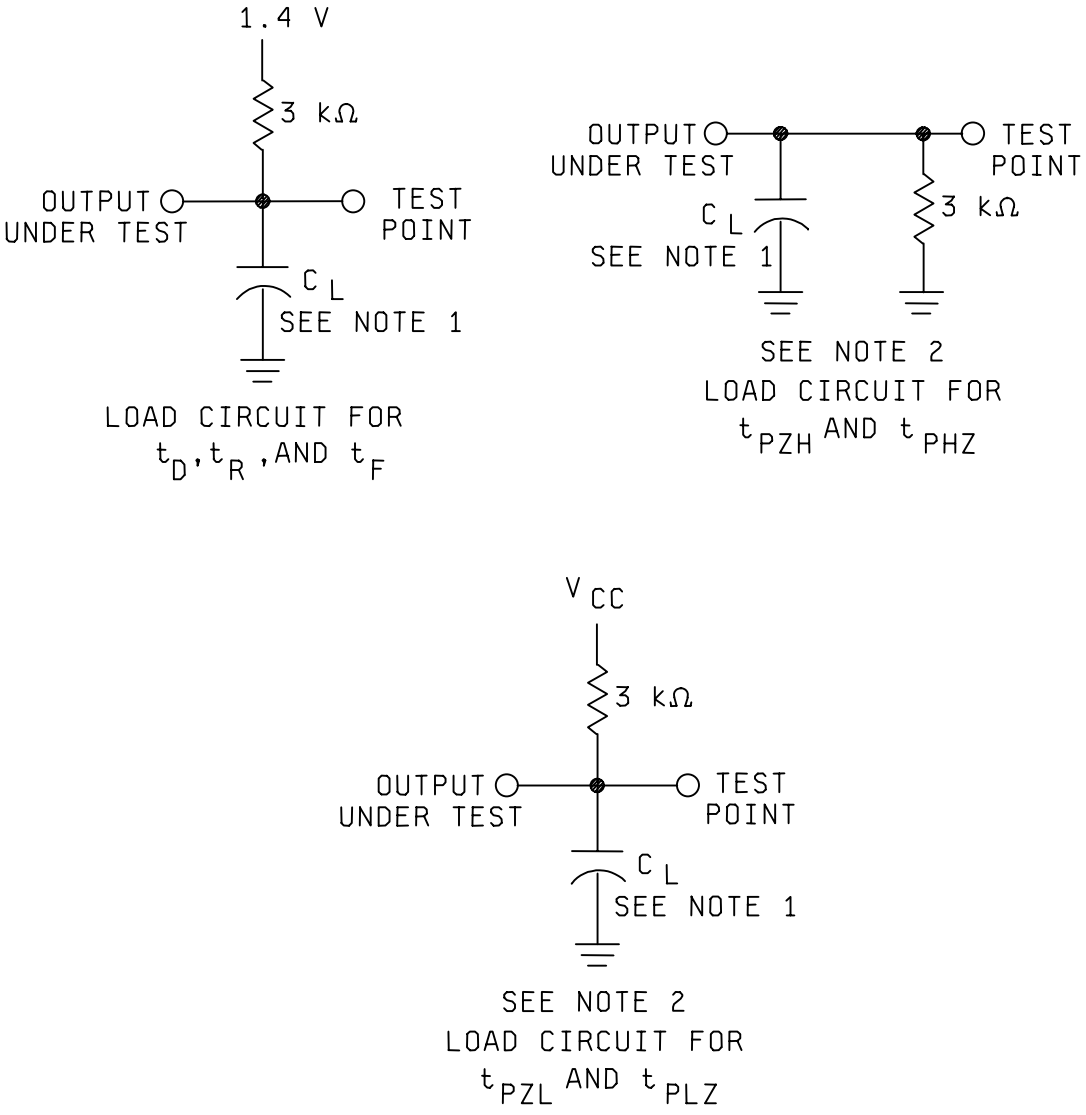
FIGURE 2. Timing waveforms.



NOTES:

1. The conversion cycle, which requires 36 internal system clock periods (17 ∝s maximum), is initiated with the eighth I/O clock pulse trailing edge after $\overline{CS}$ goes low for the channel whose address exists in memory at the time.
2. The most significant bit (A7) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6 – A0) will be clocked out on the first seven I/O clock falling edges. B7 – B0 will follow in the same manner.

FIGURE 2. Timing waveforms – Continued.



NOTES:

1. C_L = 50 pF for device type 01 and 100 pF for device type 02.
   C_L includes jig capacitance.
2. $t_{EN} = t_{PZH}$ or t_{PZL}, $t_{DIS} = t_{PHZ}$ or t_{PLZ}.

FIGURE 3. Test circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	----	----	----
Final electrical parameters (see 4.2)	1,2,3,9,10,11 1/	1,2,3, 1/ 9,10,11	1,2,3, 1/ 2/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,4,9,10,11	1,2,3,4, 9,10,11	1,2,3,4, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	----
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9	1,4,9

1/ PDA applies to subgroup 1.
2/ Delta limits in accordance with table IIB shall be computed with reference to the previous interim electrical parameters.

Table IIB. Delta limits at +25°C.

Parameter	Device type
	All
E_L	±10% of specified value in table I

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-03-03

Approved sources of supply for SMD 5962-90845 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9084501MPA	3/	TLC548MJGB
5962-9084501M2A	3/	TLC548MFKB
5962-9084502MPA	3/	TLC549MJGB
5962-9084502M2A	3/	TLC549MFKB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.