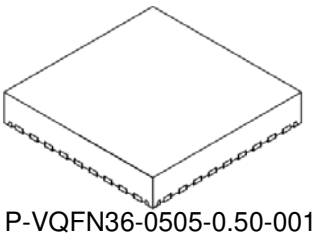
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB6605FTG

3-phase Full-wave Sine-wave Brushless Motor Controller

TB6605FTG is a 3-phase full-wave sine-wave PWM brushless motor control IC.
Sine-wave PWM driving with 2-phase modulation enables driving in high efficiency and low noise condition.

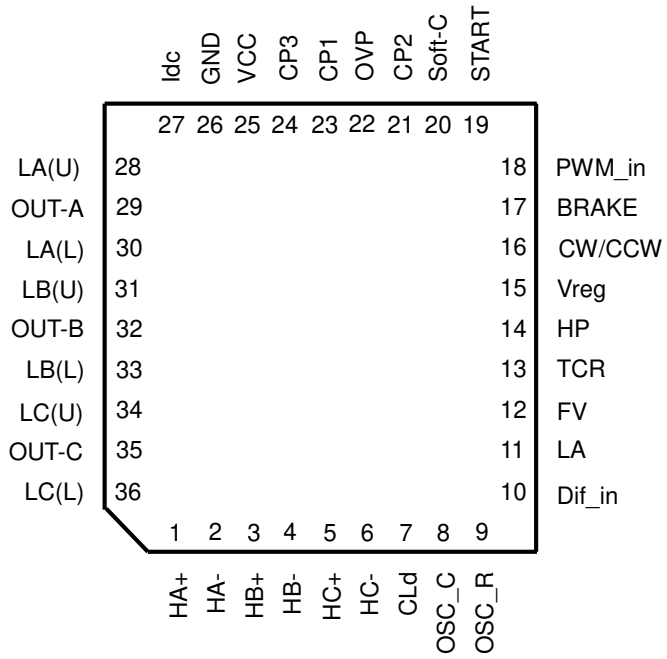


P-VQFN36-0505-0.50-001

Weight: 0.08 g (typ.)

Features

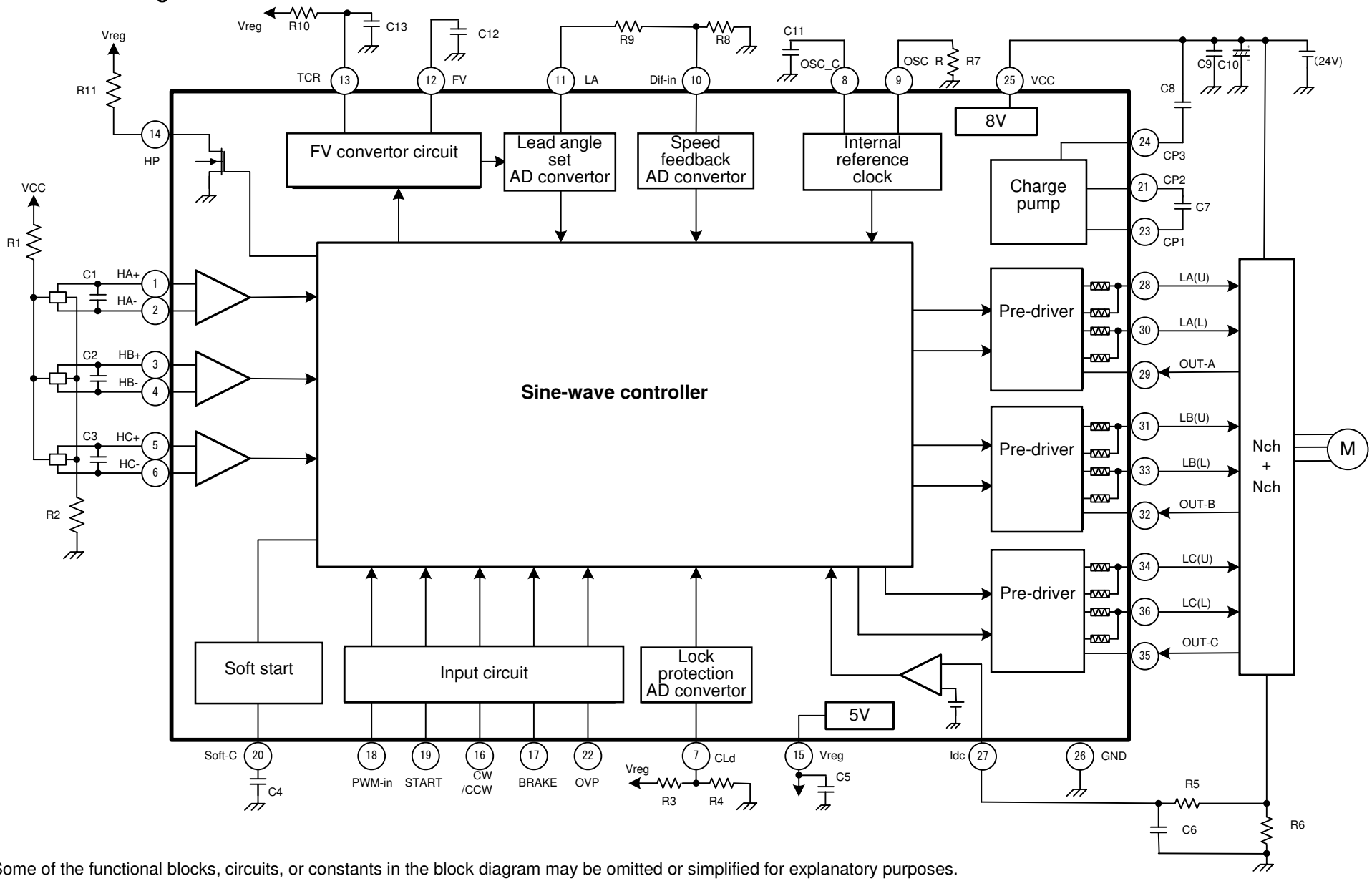
- Sine-wave PWM driving system
- 2-phase modulation system with low switching loss
- Upper Nch – Lower Nch FET
- Dead time function included
- Brake function included
- Start function included
- Speed command: PWM input type
- Auto lead-angle control function included
  (Lead angle is set based on the speed)
- CW/CCW function included
- Lock protection function included
- Output signal of hall pulse monitor included



This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

The IC should be installed correctly. Otherwise, the IC or peripheral parts and devices may be degraded or permanently damaged.

1.1.1. Block Diagram



Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

1.1.2. Pin Description

No.	Name	Description	Note
1	HA+	Hall signal (Phase-A +) input	Hall element (Phase-A) signal + input
2	HA-	Hall signal (Phase-A -) input	Hall element (Phase-A) signal - input
3	HB+	Hall signal (Phase-B +) input	Hall element (Phase-B) signal + input
4	HB-	Hall signal (Phase-B -) input	Hall element (Phase-B) signal - input
5	HC+	Hall signal (Phase-C +) input	Hall element (Phase-C) signal + input
6	HC-	Hall signal (Phase-C -) input	Hall element (Phase-C) signal - input
7	CLd	Lock protection circuit setting pin	Voltage input
8	OSC_C	Internal reference clock setting C connecting	External capacitor between GND and OSC_C.
9	OSC_R	Internal reference clock setting R connecting	External resistor between GND and OSC_R.
10	Dif_in	Speed feedback input	-
11	LA	Lead angle setting voltage input	Input lead angle ADC
12	FV	Smoothing pin of MMV output	External capacitor
13	TCR	CR pin of MMV	External resistor and capacitor
14	HP	Output signal of hall pulse monitor	HA monitor of signal after it makes it to binary
15	Vreg	5V Power voltage source	Connecting capacitor to GND against 5 V output
16	CW/CCW	CW/CCW switching pin	H**:** Reverse/L**:** Forward, Pull up resistor of 50 kΩ (typ.)
17	BRAKE	Brake signal input	L**:** Brake (All phases of lower side**:** ON), Pull up resistor of 50 kΩ (typ.)
18	PWM_in	PWM signal input for speed command	Pull up resistor of 50 kΩ (typ.)
19	START	Start signal input	L**:** Start, H**:** Stop, Pull up resistor of 50 kΩ (typ.)
20	Soft-C	Capacitor pin for soft start	External capacitor
21	CP2	Charge pump 2	For upper side Nch FET gate voltage
22	OVP	Switching pin for avoiding voltage booster	Pull up resistor of 50 kΩ (typ.) TEST pin is held concurrently, TEST mode**:** Vref + 0.7 V (= 5.7 V) or more
23	CP1	Charge pump 1	For upper side Nch FET gate voltage
24	CP3	Charge pump 3	For upper side Nch FET gate voltage
25	VCC	Logic Supply voltage pin	V_{CC} (opr.) = 9 to 28 V
26	GND	Ground pin	-
27	Idc	Output current detection signal input pin	Into gate block function when over 0.25 V (typ.)
28	LA (U)	Phase-A driving signal output (U)	Phase-A output FET gate (for upper-side Nch)
29	OUT-A	Phase-A motor pin	-
30	LA (L)	Phase-A driving signal output (L)	Phase-A output FET gate (for lower-side Nch)
31	LB (U)	Phase-B driving signal output (U)	Phase-B output FET gate (for upper-side Nch)
32	OUT-B	Phase-B motor pin	-
33	LB (L)	Phase-B driving signal output (L)	Phase-B output FET gate (for lower-side Nch)
34	LC (U)	Phase-C driving signal output (U)	Phase-C output FET gate (for upper-side Nch)
35	OUT-C	Phase-C motor pin	-
36	LC (L)	Phase-C driving signal output (L)	Phase-C output FET gate (for lower-side Nch)

** Metal exposed part on the 4 corners and the underside are connected electrically each other.
Although pin assignment is considered to avoid the distraction from pin-pin or pin-metal area shortage, use in the state of the metal area on 4 corners and underside is opened electrically.
(If connected to ground, there is a possibility for distraction with shortage.)

1.1.3. Absolute maximum ratings (Ta = 25°C)

Characteristics	Symbol	Rating		Unit
Supply voltage	$V_{CC}1$	30	(Note. 1)	V
	$V_{CC}2$	32	(Note. 2)	
Input voltage	V_{IN}	5.5	(Note. 3)	V
		Vreg	(Note. 4)	
Output voltage	V_{OUT}	5.5	(Note. 5)	V
		30	(Note. 6)	
		40	(Note. 7)	
Output current	I_{OUT}	10	(Note. 8)	mA
		20	(Note. 9)	
		10	(Note. 10)	
		2	(Note. 11)	
Power dissipation	P_D	1.56	(Note. 12)	W
Operation temperature	T_{opr}	−30 to 85		°C
Storage temperature	T_{stg}	−55 to 150		°C

Note 1**:** Vcc (in normal operation)

Note 2**:** Vcc (When 8 V charge pump is disabled, without external C for the charge pump)

* In normal operation, absolute maximum rating is Vcc1, as charge pump function is necessary for the operation.

Note. 3**:** CW/CCW, START, BRAKE, and PWM-in

Note. 4**:** OVP

Note. 5**:** HP

Note. 6**:** OUT-A, OUT-B, and OUT-C

Note. 7**:** LA (U), LB (U), and LC (U)

Note. 8**:** LA(U),LB(U),LC(U), LA(L),LB(L), and LC(L) source current

Note. 9**:** LA(U),LB(U),LC(U), LA(L),LB(L), and LC(L) sink current

Note. 10**:** Vreg

Note. 11**:** HP

Note. 12**:** Mounted on PCB (Glass epoxy 76.2 mm × 114.3 mm × 1.6 mm, Cu area 60 %, single layer)

Absolute maximum rating is the standard without any exception even in a moment.
If the IC is operated in a condition beyond the rating, destruction, degeneration or damaging of IC or external parts possibly occurs. Design to avoid the condition beyond the rating in any operating condition.
Operate within the condition described in next table “Operating condition”.

1.1.4. Operating condition (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage (Note. 1)	V_{CC}	9 to 28	V
PWM input signal for speed command (PWM_in) (Note. 2)	PWM_in	10 to 100	kHz
Internal reference clock frequency (Note. 3)	fx	2 to 8	MHz

(Note. 1)**:** OUT-A, OUT-B, and OUT-C pins should be rating voltage (30 V) or less.
(Note. 2)**:** Output PWM frequency does not change depending on PWM-in frequency.
Output PWM is configured depending on the internal reference clock frequency.
(Note. 3)**:** Please configure the external constant number including variation.

1.1.5. Description for operation

1. Sine-wave PWM driving

1.1.5.1. < Energization mode switching >

When starting, TB6605FTG operates rectangle driving of 120° energization signal with position detect signal.
After f (frequency every 1 phase of position detect signal (hall element signal)) goes beyond fH (setting frequency), at HA falling timing next-after IC counts 6 times of hall signal switching edges, the operation mode is switched to 180° energization mode.
(About Hall input signal, see 8. Hall amplifier circuit.)

The Setting Frequency fH is determined as next.

Setting frequency**:** $fH = fx \div (2^{10} \times 64 \times 6)$

The fx is internal reference clock determined with OSC_R and OSC_C.

When fx = 4 MHz, fH = 10.15 Hz,

fx = 5 MHz, fH = 12.7 Hz, and

fx = 6 MHz, fH = 15.25 Hz.

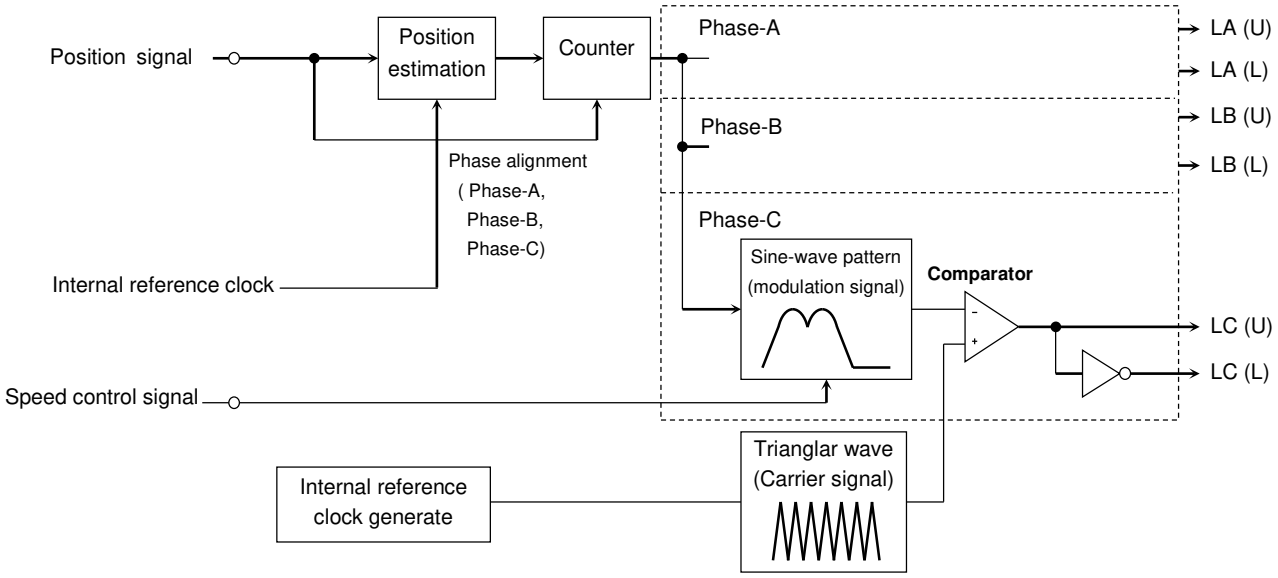
1.1.5.2. (Mode Table)

Rotating state	Driving mode
$f_H > f$	Rectangle driving (120° energization)
$f_H < f$	Sinusoidal wave PWM driving (180°energization)

*To avoid malfunction from noise, IC operates in 120° energization mode when f is higher than normal possible frequency.
(When fx = 5 MHz, if over 1 kHz, IC operates in rectangle 120° energization mode.)

<Operation Flow>

The following figure is actually processed digitally with the image chart in the IC.



<180° energization >

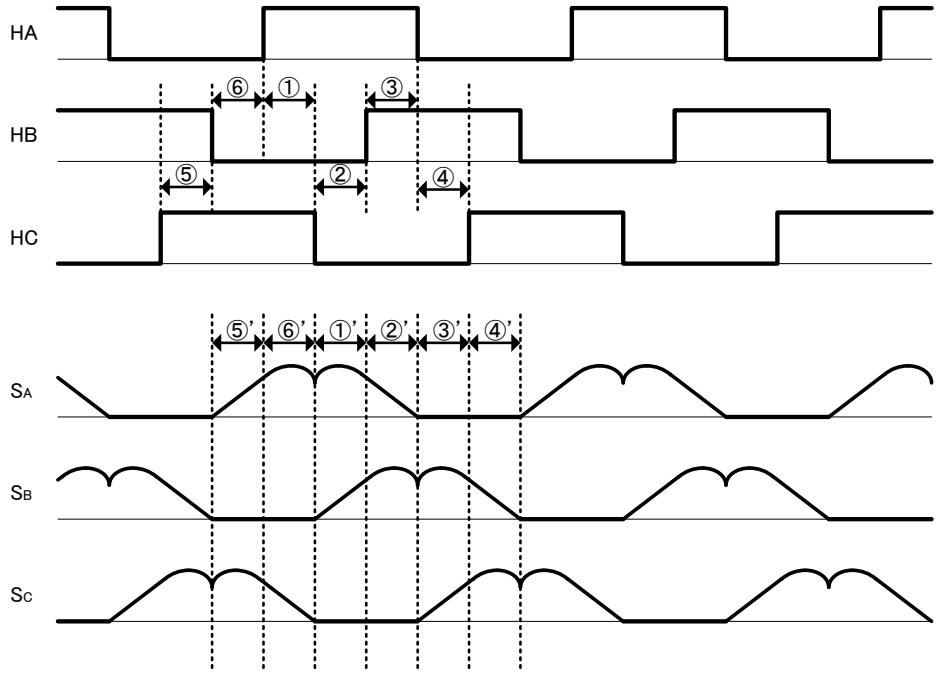
●60° modulation-60° reset is operated.

The modulation signal is created from position detect signal. Sinusoidal PWM signal is created from comparing this modulation wave to triangular wave.

IC counts the time between one zero-cross timing to next zero-cross timing of 3 position detect signals (60° electrical angle), and use this time as next 60° phase length.

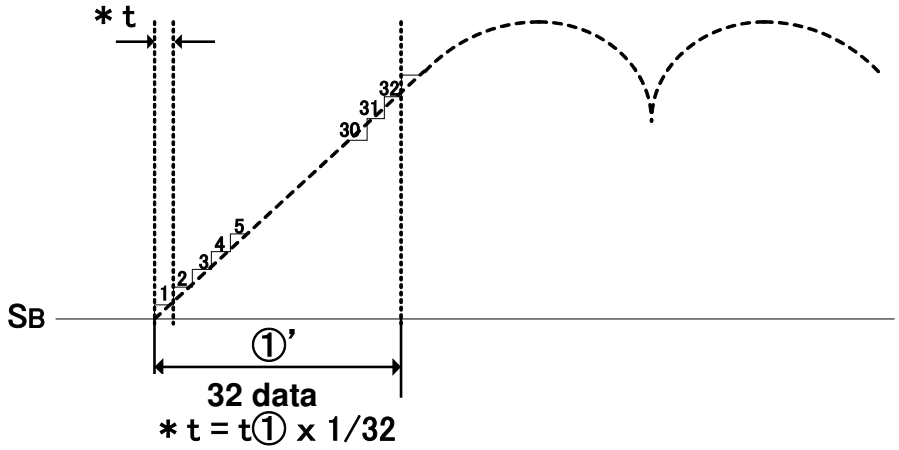
The 60° phase length of the modulation signal is from 32 data, and time length for 1 data is 1/32 of time length of the previous 60° phase length, so modulation wave advances with this length.

The following modulation signals of S_A, S_B, and S_C are actually processed digitally with the image chart in the IC.



On this picture, modulation wave ①' data progresses by 1/32 time length of ① (from HA: ⌐↑ to HC: ⌐↓).
Also, modulation wave ②' data progresses by 1/32 time length of ② (from HC: ⌐↓ to HB: ⌐↑).
If next zero-cross point does not come even 32 data finished, next 32 data progresses on same time length by next zero-cross point comes.

The following figure is actually processed digitally with the image chart in the IC.



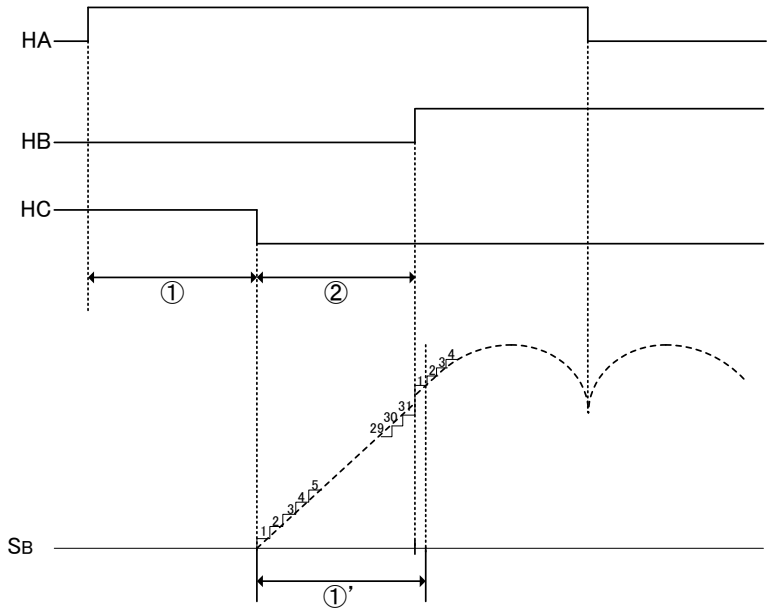
At the same time, phase alignment with the modulation wave is done on every zero-cross timing of position detect signal. On every 60° electrical angle, the modulation wave is reset in synchronization with up or down edge of position detect signal (hall amplifier output signal).

So if the next zero-cross timing comes before the end of 32 data for 60° phase because of the lag of zero-cross timing of position detect signal, the data will be reset and next data for 60° phase will be started.

In such case, the modulation wave has discontinuous point on reset timing.

*Carrier, Reset, Reset of 60°

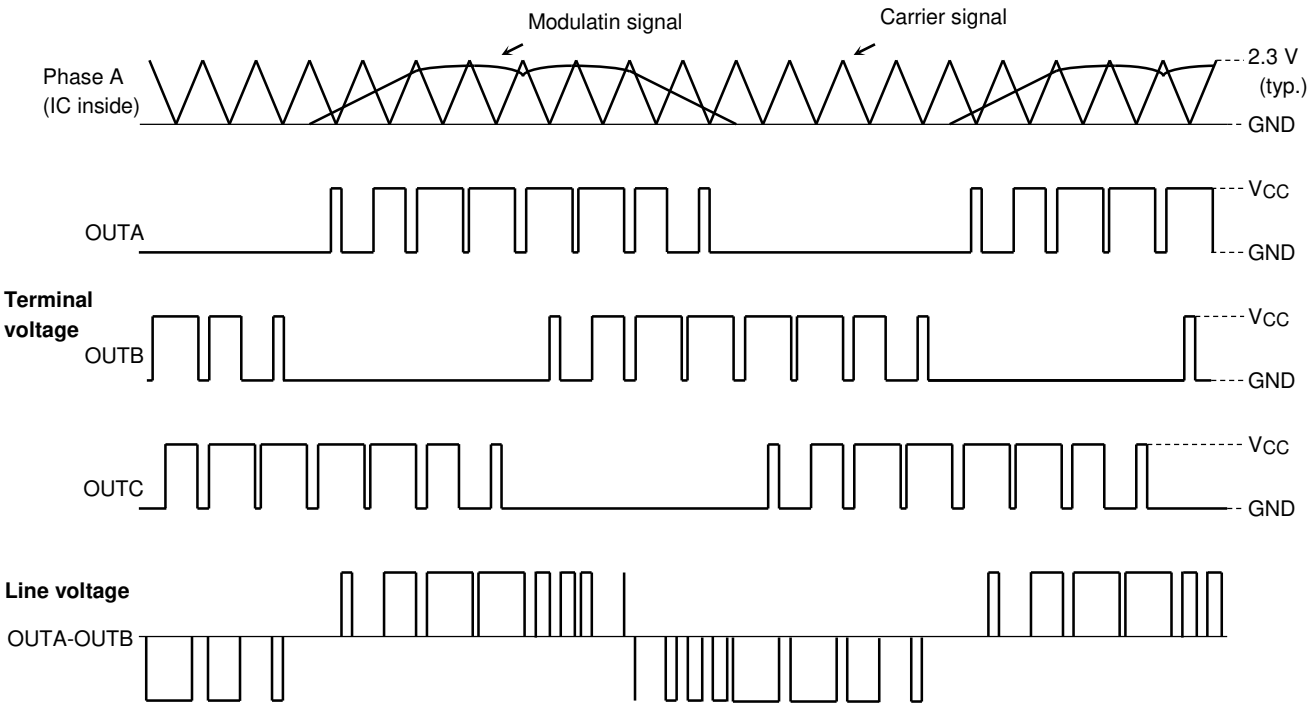
: The following figure is actually processed digitally with the image chart in the IC.



Timing charts may be simplified for explanatory purposes.

1.1.5.3. (Operation waveform for sinusoidal PWM driving)

The following modulation signals and carrier signals are actually processed digitally with the image chart in the IC.

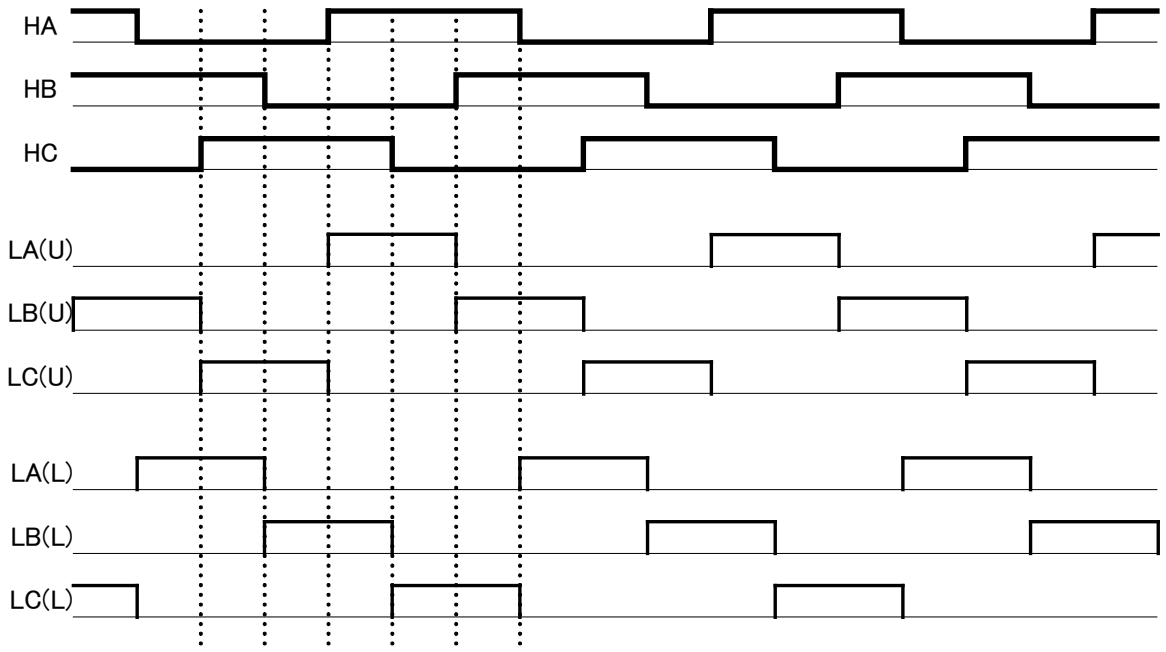


Timing charts may be simplified for explanatory purposes.

<120° energization>

●In 120° energization, output states of three position detect signals (HA, HB, and HC) are confirmed and turned on at the below timing.

(In forward rotation; Upper side**:** PWM timing, Lower side**:** full-on timing)



Timing charts may be simplified for explanatory purposes.

(Example case)

Hx (Hall signal)**:** H = 1 and L = 0;

OUTx (output)**:** Upper side PWM timing H = 1, Lower side ON timing L = -1, and both OFF timing M = 0

<Clockwise>

OUTA = HA – HB

OUTB = HB – HC

OUTC = HC – HA

<Counter clockwise>

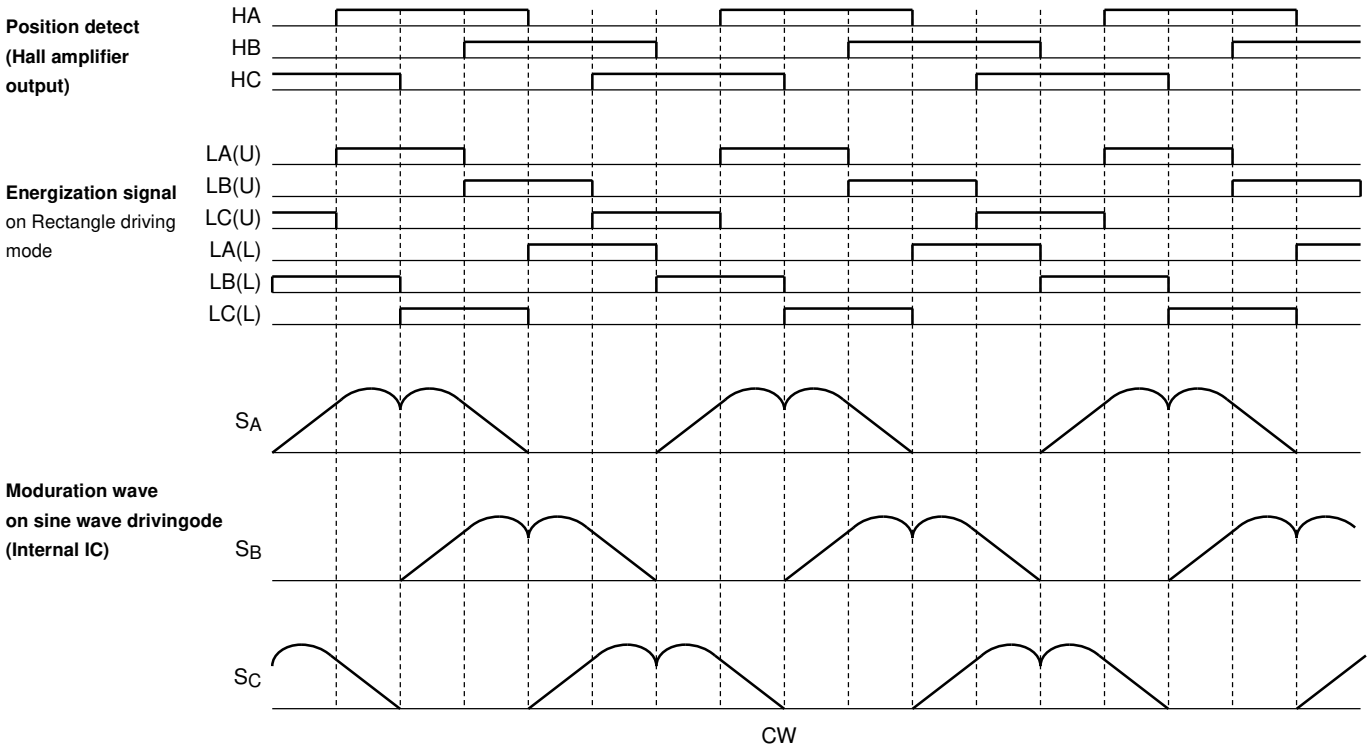
OUTA = – (HA – HB)

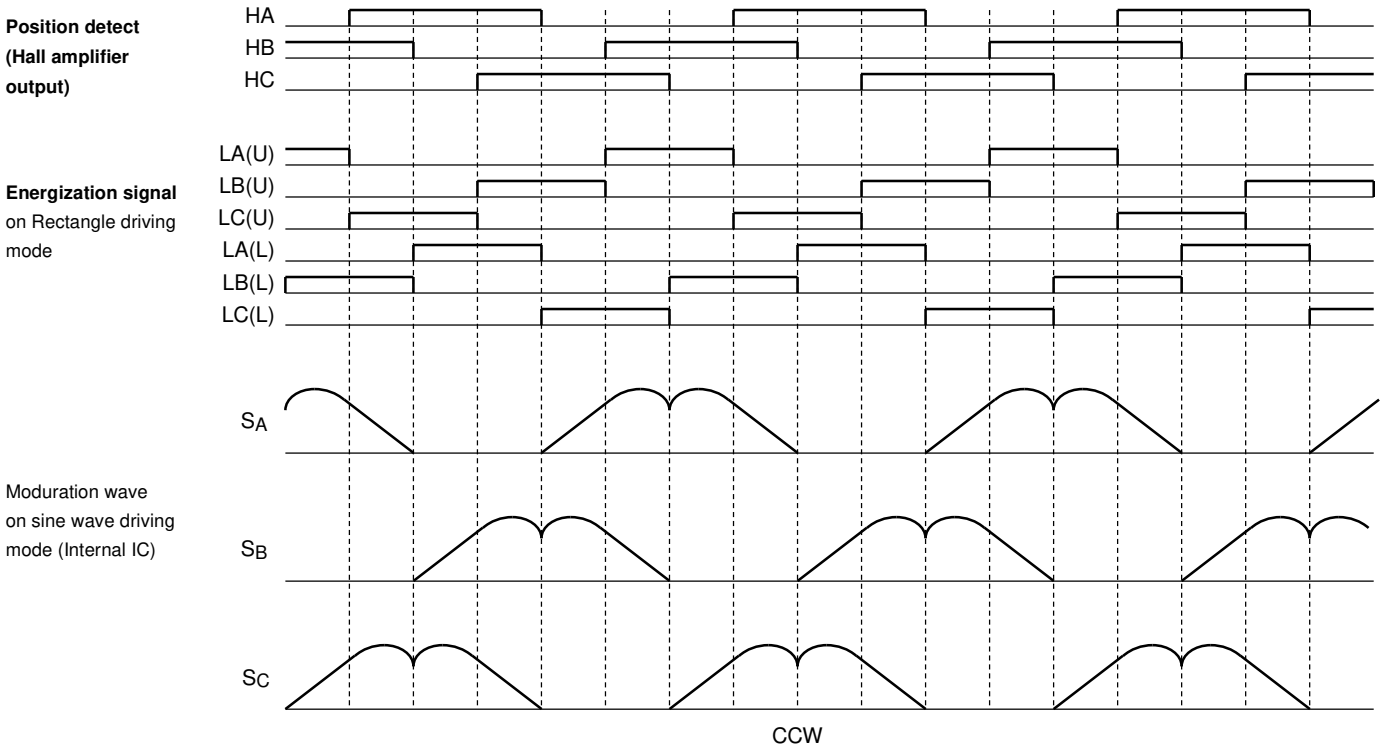
OUTB = – (HB – HC)

OUTC = – (HC – HA)

1.1.6. Timing chart

Timing charts may be simplified for explanatory purposes.
The following modulation signals are actually processed digitally with the image chart in the IC.





* HA, HB, and HC**:** Hall amplifier outputs

2. Internal reference clock

・IC generates reference clock internally with external C and R. Following parameters are configured by this reference clock.
(1) Output PWM frequency
(2) Dead time
(3) Lock detecting time
・Internal reference clock should be set within the range of 2 MHz (min) to 8 MHz (max) including variation.
・Each parameters should be set within the below range in consideration of variation of internal reference clock frequency.

Setting range of internal reference clock frequency	2.3 MHz (min)	5 MHz(typ.)	7.2 MHz (max)
Setting range of Output PWM frequency	9.2 kHz	20.1 kHz	29.0 kHz
Setting range of dead time	2.6 μs	1.2 μs	0.8 μs
Setting range of lock detecting time (5 seconds setting)	10.78 s	4.96 s	3.44 s

(*) When C = 47 pF and R = 10 kΩ, fx = 5 MHz (typ.).

・The approximate formula of external C and R and internal reference clock frequency fx is as follows;

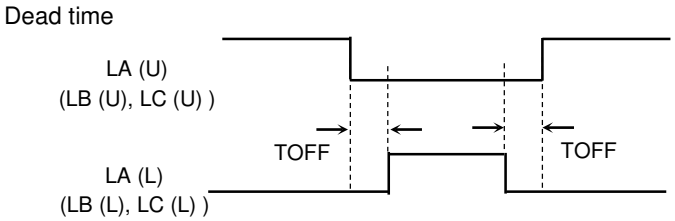
$$fx = \frac{6.1}{1.85 \times C_{[pF]} \times 10^{-12} \times R_{[\Omega]} + 350 \times 10^{-9}} [Hz]$$

3. Outout PWM frequency

Output PWM frequency is switched depending on the internal reference clock.
fx**:** Internal reference clock
PWM frequency f_{PWM} = fx/248 (= triangle-wave frequency)
fx = 4 MHz**:** f_{PWM} = 16.1 kHz
fx = 5 MHz**:** f_{PWM} = 20.1 kHz
fx = 6 MHz**:** f_{PWM} = 24.2 kHz

4. Dead time setting circuit

Dead time on driving signal output is created to avoid same-timing ON of upper and lower output power FET because TB6605FTG controls output FET using PWM with synchronous commute system.



fx**:** internal reference clock
dead time td = (1/fx) × 6
(Ex.)
fx = 4 MHz**:** td = 1.5 μs
fx = 5 MHz **:** td = 1.2 μs
fx = 6 MHz **:** td = 1.0 μs

5. Charge pump (step-up voltage circuit)

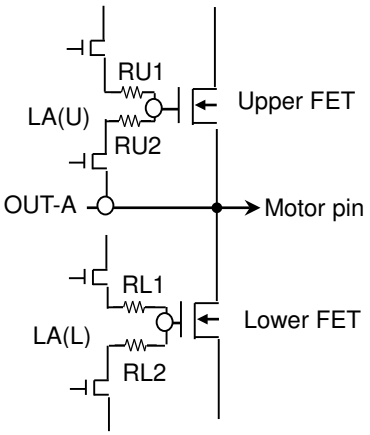
TB6605FTG is for Nch + Nch external output FET system. So charge pump circuit is included to generate voltage for upper Nch Gate voltage.
Step-up voltage is Vcc+ (8 V). Gate voltage of upper FET is Vcc+ (7.75 V).
Voltage step-up is done on the 1/16 frequency of internal reference clock fx.
If fx = 5 MHz, charge pump frequency is 313 kHz.

6. Motor output pin

During PWM operation, source voltage of external upper Nch FET swings from ground level to V_{CC} level.
As external Nch FET VGS (max) = 20 V, internal clump circuit is prepared to avoid that higher voltage is applied to VGS.

7. External FET gate driving output

To suppress the switching noise on FET driving, source and sink output for FET driving is configured as right figure.
Next value resistors are built in the output portion to control the output FET.

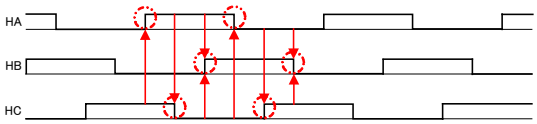


Built-in Resistor

Upper side source	RU1 = 1 kΩ (typ.)
Upper side sink	RU2 = 100 Ω (typ.)
Lower side source	RL1 = 1 kΩ (typ.)
Lower side sink	RU2 = 100 Ω (typ.)

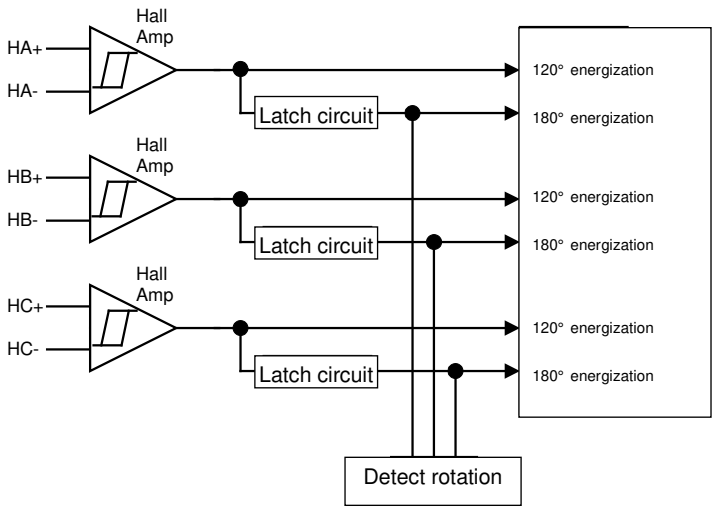
8. Hall amplifier circuit

- Input the hall element output signal. If noise exists in the input signal, connect a capacitor between the input pins.
  Common mode input voltage range, VCMRH = 0.5 V to 3.4 V.
- Hall element signal is formed into square waveform by hall amplifier and input to internal logic.
- If all hall input is opened, all output for motor will be Hi-impedance.



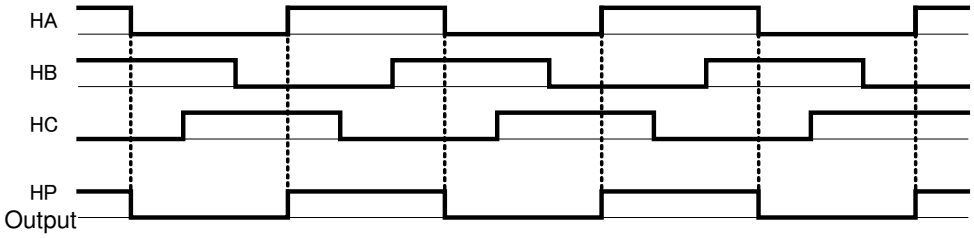
Timing charts may be simplified for explanatory purposes.

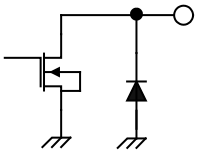
- To avoid a chattering or a malfunction during the 180° energization mode, latch circuit is included. It detects the hall signal state of other phase, checks the L/H level and if the level is adequate, and so it goes to latch state.
  Rotating direction is detected and confirmed at the same time, with detection of 3 phase hall signals.
  Hall amplifier has input hysteresis (16 mV (typ.)). During 120° energization operation, malfunction is avoided by only its hysteresis. Latch circuit is not used.



9. HP Output

HP signal (Hall pulse signal) is outputted from HP pin.
HP = HA signal after it makes it to binary.

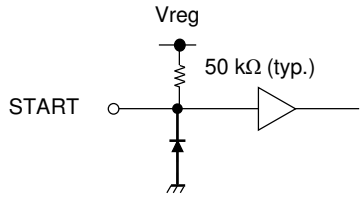




HP output is open-drain output.
Output capability**:** HP (on) 0.5 V (max) @Iout = 2 mA

When START = High, HP output is off. It is fixed to high by pulling up the resistor.

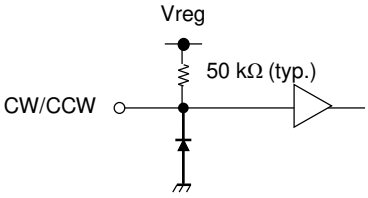
10. Start/Standby Circuit



START pin is TTL input and includes 5 V pull-up resistor inside.

START input	Mode
H	Standby
L	Start

11. CW/CCW Circuit



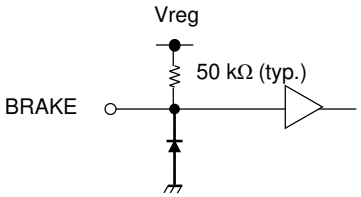
CW/CCW pin is TTL input and includes 5 V pull-up resistor inside.

CW/CCW input	Mode
H	CCW
L	CW

CW**:** Hall element signal $HA^+ \rightarrow HB^+ \rightarrow HC^+$

*Note**:** Refer to timing chart of page 9.
*Note**:** Output FET could be destroyed with counter torque, if switched CW/CCW suddenly.

12. Brake



BRAKE pin is TTL input and includes 5V pull-up resistor inside.

START	BRAKE	Mode
L	L	Active/Brake
L	H	Active/Normal
H	L / H	STBY

In the brake mode, all lower outputs of three-phase outputs are turned on. When over current is detected while BRAKE is low, the state of BRAKE = L is taken priority.

*Note**:** Output FET could be destroyed, if switched from high speed rotating to brake-on suddenly.

*On next state, Output-off has higher priority so brake function does not work.

Vcc is lower than the voltage monitoring level, charge pump is not working for driving upper side Nch FET.

Thermal shut down function is working.

*On next state, brake function works if BRAKE = L.

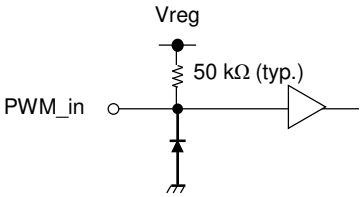
Vcc voltage bounce protection is working, over-current limitation circuit is working.

13. Speed Command (PWM-in)

PWM signal is inputted to the PWM-in pin externally as a speed command

Sine-wave PWM modulation signal is controlled by its duty.

The higher the ON duty of PWM becomes, the higher the duty of output PWM becomes and the faster the rotation speed becomes.



PWM_in pin is TTL input and includes 5V pull-up resistor inside.

The mode moves to the Low active. The longer the term of low becomes, the longer the term of ON becomes.

・PWM control range**:** Recognizing 0 to 100%.

・Resolution**:** 20 kHz 0.4%, 40 kHz 0.8%

However, when PWM-in duty is recognized in 180°energization mode, the variation of this recognition (±0.4% (PWM-in = 20 kHz)), which is generated from the non-synchronous with the internal clock, is ignored and cancelled.

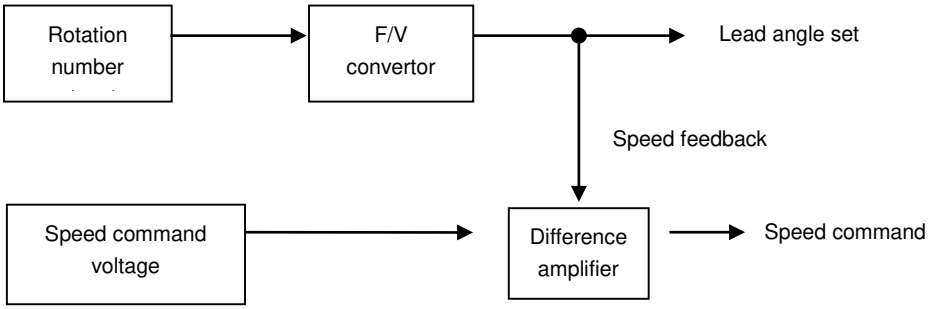
・PWM-in = 0%**:** Output is off, Releasing lock protection.

*Output PWM frequency does not change depending on the PWM-in frequency.

Output PWM is configured depending on the internal reference clock.

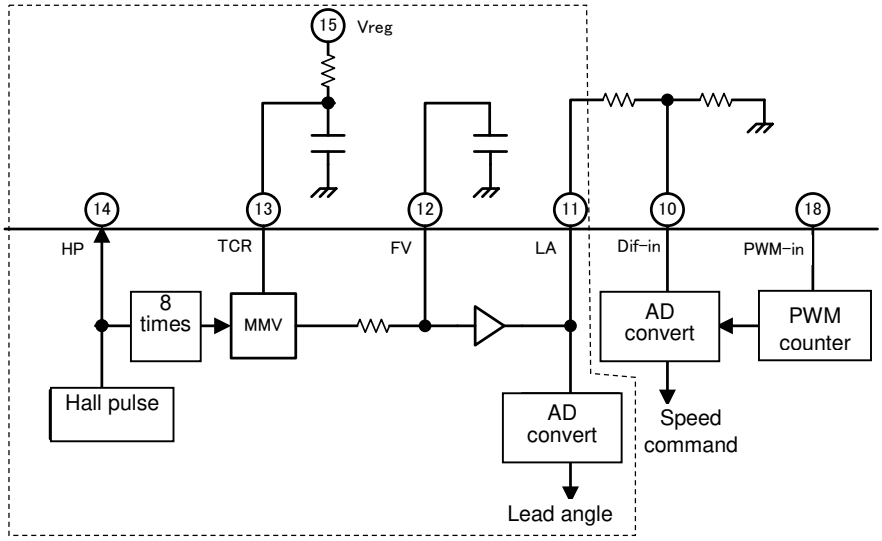
14. Speed feedback and Lead angle control

To improve the linearity of the rotation number for speed command input, function of feedback rotation number to speed command voltage is included. However, speed feedback reduces the rotation number.



15. Lead angle control

Lead angle converts the hall signal between F and V and configures it with the voltage depending on the rotation number.



・Frequency range of hall signal (single phase)**:** Minimum value – 12.7 Hz Maximum value – 1 kHz

・F/V converting is carried by using MMV (mono stable multi vibrator circuit).

Octuple signal of one hall signal is generated as an input signal of MMV.

Pulse width is determined by external C and R of TCR pin. MMV output is smoothed by the internal resistor and the filter of external capacitor of FV pin. FV output is clumped at 3 V.

Octuple signal (FV output) of HP is generated after the mode is switched to 180°energization drive. And FV is not outputted for 13.1 ms (@fx = 5 MHz) or less after it changes into 180°energization drive.

・External constant number of TCR pin is set based on the below formula.

External constant number**:** CR = 0.6/(8×f×ln(5/4))

(Ex.)

When lead angle is maximum at Hall = 1kHz,

C×100k = 0.6/ (8×1000×220m) →C = 3400 pF, R = 100 kΩ

The value of R is recommended around 100 kΩ. The value of C is recommended less than 0.1 μF.

*This formula is an ideal one. The error margin occurs in the expression because it loses an internal element in the IC actually.

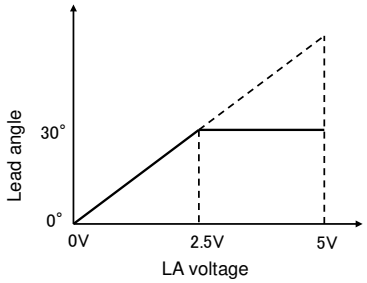
・LA voltage is AD converted and lead angle is configured.

Phase of energization signal can be leaded by inputting voltage whose range is 0 to 2.5 V (16 steps).

0 V → 0°

2.5 V →30° (Including input of 2.5 V or more.)

<Reference value>



・LA voltage is clumped at 30° (Max.) of lead angle.

Input voltage is not clumped. It is clumped at 30° setting internal logically.

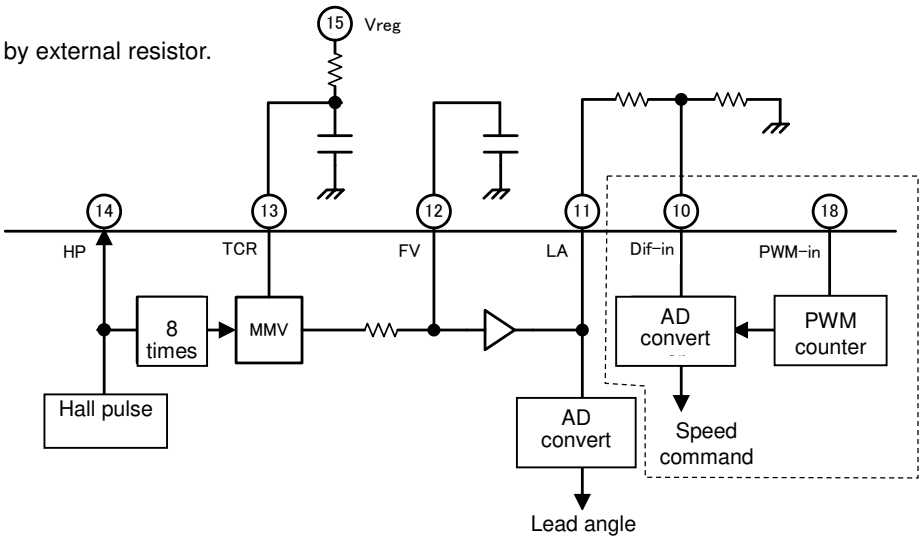
・Timing of lead angle reflection.

The timing of the reflection of lead angle is reflected once per 16 cycles of hall signal Ha.

・It does not have the hysteresis voltage of LA.

16. Speed feedback pin (Dif-In)

・Dif_in feedbacks speed signal (F/V conversion voltage) which is read from HP signal.
・Range of hall signal (single phase)**:** Min. – 12.7 Hz Max. – 1 kHz
・Range of Dif_in input**:** 0 to 3 V
・Resolution 1/256 11 mV/step
・LA voltage of feedback is adjusted by external resistor.



17. Lock protection circuit

・This is the function to turn off the output power FET when motor is locked.
・Voltage of CLd pin switches latch mode (1s/5s/10s) and auto recovery mode (1s/5s/10s). In the auto recovery mode, the operation recovers with three times of lock detecting time.
The voltage of CLd shown below is under the condition the voltage of Vreg is 5 V. Please set the voltage of CLd by dividing the resistance voltage of Vreg (resistance accuracy**:** 5 % or less).

CLd voltage			Mode
Min (V)	Typ. (V)	Max (V)	
0	0	0.4	Without lock protection
0.65	0.71	0.77	Auto recovery mode, Lock detecting time**:** 10s
1.05	1.13	1.22	Auto recovery mode, Lock detecting time**:** 5s
1.53	1.63	1.75	Auto recovery mode, Lock detecting time**:** 1s
1.99	2.12	2.24	Latch mode, Lock detecting time**:** 10s
2.47	2.60	2.72	Latch mode, Lock detecting time**:** 5s
2.95	Vref	Vref	Latch mode, Lock detecting time**:** 1s

・CLd pin should not be open, set to above voltage.
Capacitor should be connected to CLd pin to reduce noise.
・When CLd voltage is configured by resistance divider, please set the Vreg supply by the resistance divider. The value of 5% or less should be used.
・When hall pulse signal (HP) is detected and the edge of HP signal is not generated within lock detecting time, upper and lower of output power FET are turned off.
Latch mode is released in the mode of stop, brake or the state of PWM-in = 0 % in the timing of PWM frequency.
・Lock detecting time and recovery time is based on the output PWM frequency fPWM.
It depends on the internal reference clock frequency fx.
fPWM = fx/248
Lock detecting time (tlock) and the recovery time (trev) are calculated from below formula.
tlock = tsel/(fPWM/10001)
trev = 3×tlock
tsel**:** Setting 1s**:** tsel = 2, Setting 5s**:** tsel = 10, Setting 10s**:** tsel = 20
・For example; fx = 5 MHz,
Setting 1s**:** tlock = 0.99s, trev = 2.97s
Setting 5s**:** tlock = 4.96s, trev = 14.88s
Setting 10s**:** tlock = 9.92s, trev = 29.76s

18. Soft start function (Optional function)

●How to operate

・Soft start function starts by controlling the speed command voltage which is inputted by PWM.

・Sped command (PWM signal) is switched with 32 steps.
The external capacitor of soft_c pin is used as a clock of 32 steps.
16 cycles of the oscillation frequency of soft_c pin is recognized as one step.

・External capacitor**:** 5 seconds in connecting the capacitor of 0.016 μF.

・Maximum of set time**:** 5 seconds, Time variation**:** 5 ± 1 seconds
Relational equation of soft start time and external capacitor is as follows;
$Tsoft(s) = 16 \times 32/(0.0018 \times 10^{3} \times C^{-0.981})$
C**:** external capacitor (μF)

*In case torque is very small, the error becomes larger because of the remainder of the division.

●Vreg /Soft_c pin**:** Short /Open

・Please short-circuit soft_c pin to Vreg in order not to start soft start.

・When soft_c pin is open, do not make the circuit open to avoid the error from the noise.

・Connect the capacitor of 1000 pF or more to start soft start.

●The condition of operating soft start

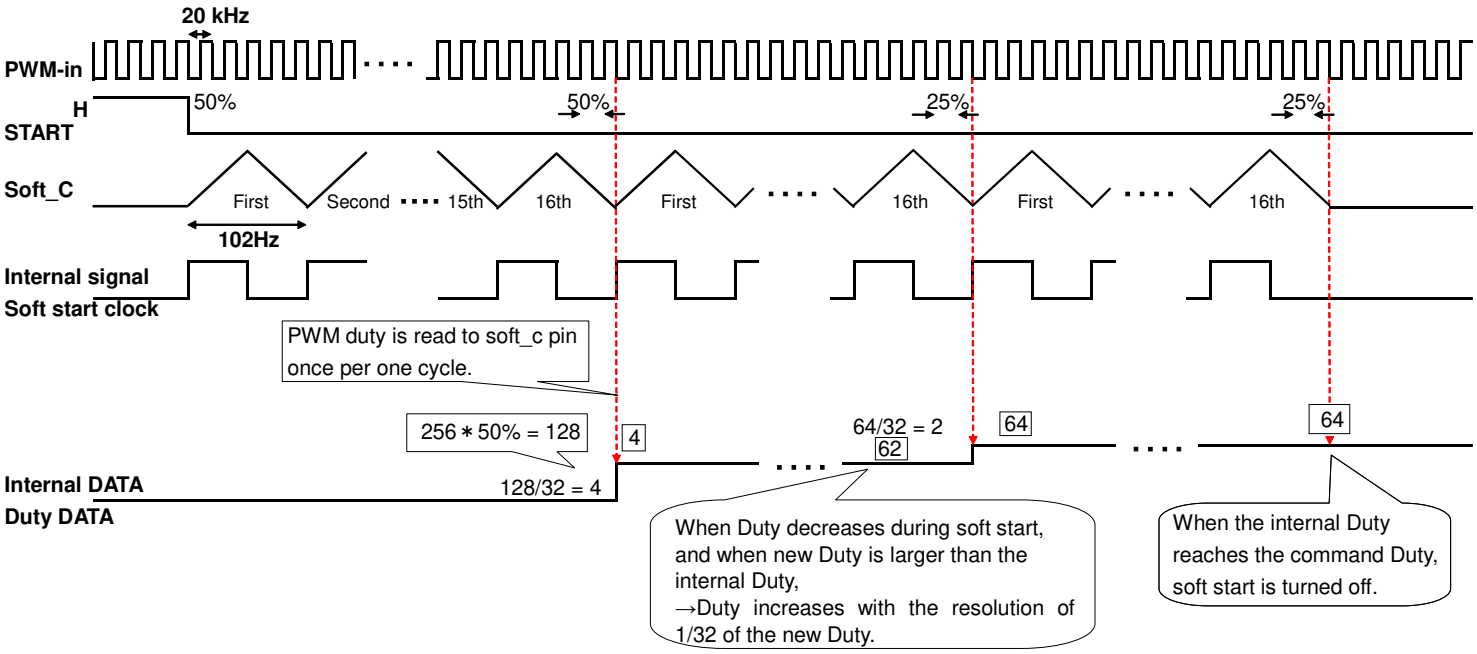
・Controlling outputs of START pin and BRAKE pin.

・Re-starting the motor operation by the start pin and the brake pin in the motor lock protection drive (latch mode).

・Recovering automatically in the motor lock protection drive (auto recovery mode).

・PWM-in frequency changing as follows; PWM-in frequency < 5 kHz ⇒ PWM-in frequency > 5 kHz.

・When the PWM input is delayed, soft start is delayed of its amount because the recognition is delayed.

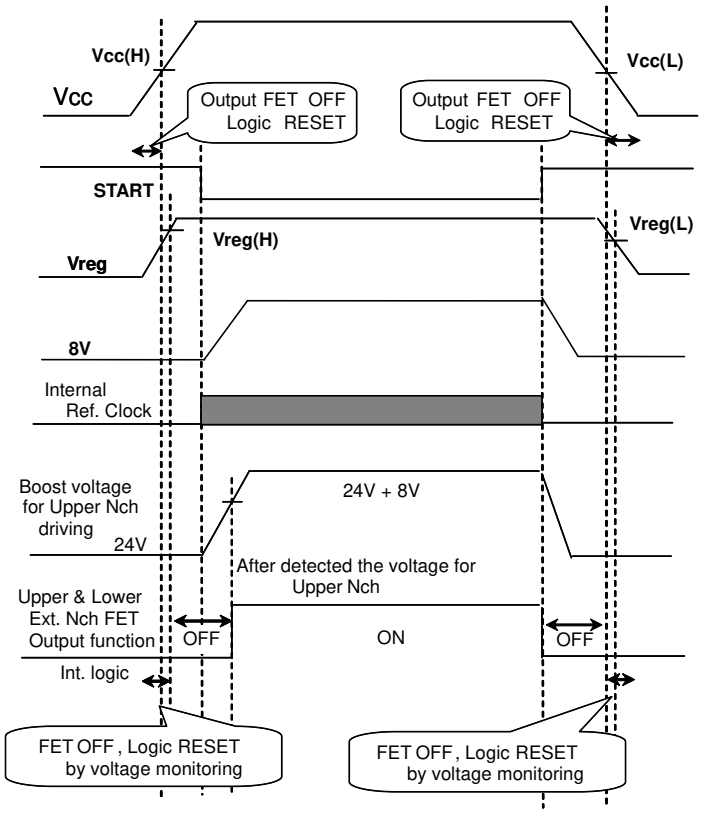


19. Supply voltage monitoring circuit

TB6605FTG includes monitoring function for Vreg and Vcc voltage.

Vcc supply voltage (24 V, ext-applied)
・Vcc(H) ≤ 8.2 V (typ.) Vcc(L) ≤ 7.5 V (typ.)
(Power ON)
In Vcc supply voltage rising, when the voltage is lower than 8.2 V (typ.), external FET (Upper and Lower) is off and internal logic is reset.
(Power OFF)
In Vcc supply voltage falling, when the voltage is lower than 7.5 V (typ.), external FET is off and internal logic is reset.
* TB6605FTG includes another Vcc monitoring function for avoid the voltage bounce.
(See the explanation for voltage bounce avoidance.)

Vreg voltage (5 V, internal reference voltage)
・Vreg(H) ≤ 4.1 V (typ.) Vreg(L) ≤ 3.8 V (typ.)
(Power ON)
Vreg rises when Vcc rises.
When Vreg voltage is lower than 4.1 V, external FET is off and internal logic is reset.
(Power OFF)
Vreg falls when Vcc falls.
When Vreg voltage is lower than 3.8 V, external FET is off and internal logic is reset.



Right picture shows a general operation example.
If Vreg voltage becomes some level from some input signal, Vreg monitoring function works.
If supply voltage is cut in motor rotating state, Vcc monitoring function works.

20. Supply voltage (Vcc) bounce protection function

TB6605FTG includes avoidance function of supply voltage bounce phenomenon in a sharp deceleration state. If this function works, driving mode is changed from synchronous rectification state to 120° driving (Upper side PWM) state.

Switching the energization mode uses following two judgments;

voltage (described below) and frequency (overflow). In avoiding supply voltage bounce phenomenon, both judgments are used.

Avoiding supply voltage is switched between 12 V and 24 V by OVP pin.

OVP pin includes pull-up resistor of 5 V. High**:** 24 V spec., Low**:** 12 V spec.

*OVP pin should not been controlled by external power supply.

24 V spec.**:** Short-circuit to Vreg pin or open.

12 V spec.**:** Short-circuit to GND.

(1)12 V spec.

(1)-1 Conditions of “Synchronous rectification (180° energization) ⇒ Upper PWM (120° energization)”

Vcc is monitored. Vcc reaches upper operation guarantee voltage or more (Vcc > 15.5 V (typ.)).
Judging voltage is defined as follows (including IC variation);
14.5 V (min) 15.5 V (typ.) 16.5 V (max)

(1)-2 Conditions of “Upper PWM (120° energization) ⇒ Synchronous rectification (180° energization)”

Vcc is monitored. Vcc falls upper operation guarantee voltage or less (Vcc < 14.5 V (typ.)).
When margin of ±10 % is expected for 24 V power supply, it becomes 26.4 V (max).
Recovery voltage is as follows;
13.5 V (min) 14.5 V (typ.) 15.5 V (max)

(2)24 V spec.

(2)-1 Conditions of “Synchronous rectification (180° energization) ⇒ Upper PWM(120° energization)”.

Vcc is monitored. Vcc reaches upper operation guarantee voltage or more (Vcc > 28.5 V (typ.)).
Judging voltage is defined as follows (including IC variation);
27.5 V (min) 28.5 V (typ.) 29.5 V (max)

(2)-2 Conditions of “Upper PWM (120° energization) ⇒ Synchronous rectification (180° energization)”

Vcc is monitored. Vcc falls upper operation guarantee voltage or less (Vcc < 27.5 V (typ.)).
When margin of ±10% is expected for 24 V power supply, it becomes 26.4 V (max).
Recovery voltage is as follows;
26.5 V (min) 27.5 V (typ.) 28.5 V (max)

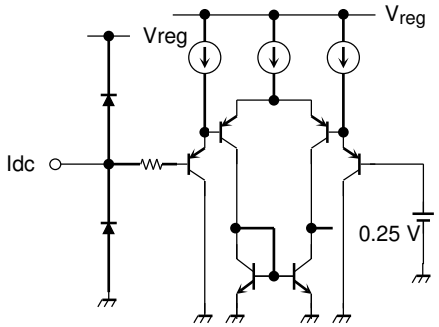
21. Constant voltage circuit

・ Vreg

5 V voltage for internal logic bias is outputted from Vreg pin.

Connect capacitor (recommended value**:** 1 μF) between Vreg pin and GND to avoid the oscillation or noise absolutely.

22. Over current limitation circuit



When over current limitation circuit reference voltage become higher than 0.25 V (typ.), all upper side power FET attached external is off.

The off mode is cleared on every career triangle wave timing.

(Detect→ Off on synchronous rectification part, PWM Duty = 0. The channel that lowers side full-on keeps on state.)

Note**:** I_{dc} pin has high sensitivity as it is input to analog comparator directly, so add a filter comprised of C, R externally to prevent malfunctions from noise of output current chopping.

23. Thermal shutdown circuit

If junction temperature become higher than TSD (ON) = 160 °C (typ.), external output power FET become off. The temperature hysteresis is 15 °C (typ.). The operation is recovered automatically if the junction temperature falls.

These functions are to prevent irregular state from output shortage etc. temporally, and do not guarantee that IC is not destroyed.

Priority of each function and mode

(1) Thermal shutdown circuit > (2) Dead time setting > (3) Short brake (BRAKE = L) > (4) Over current limitation circuit

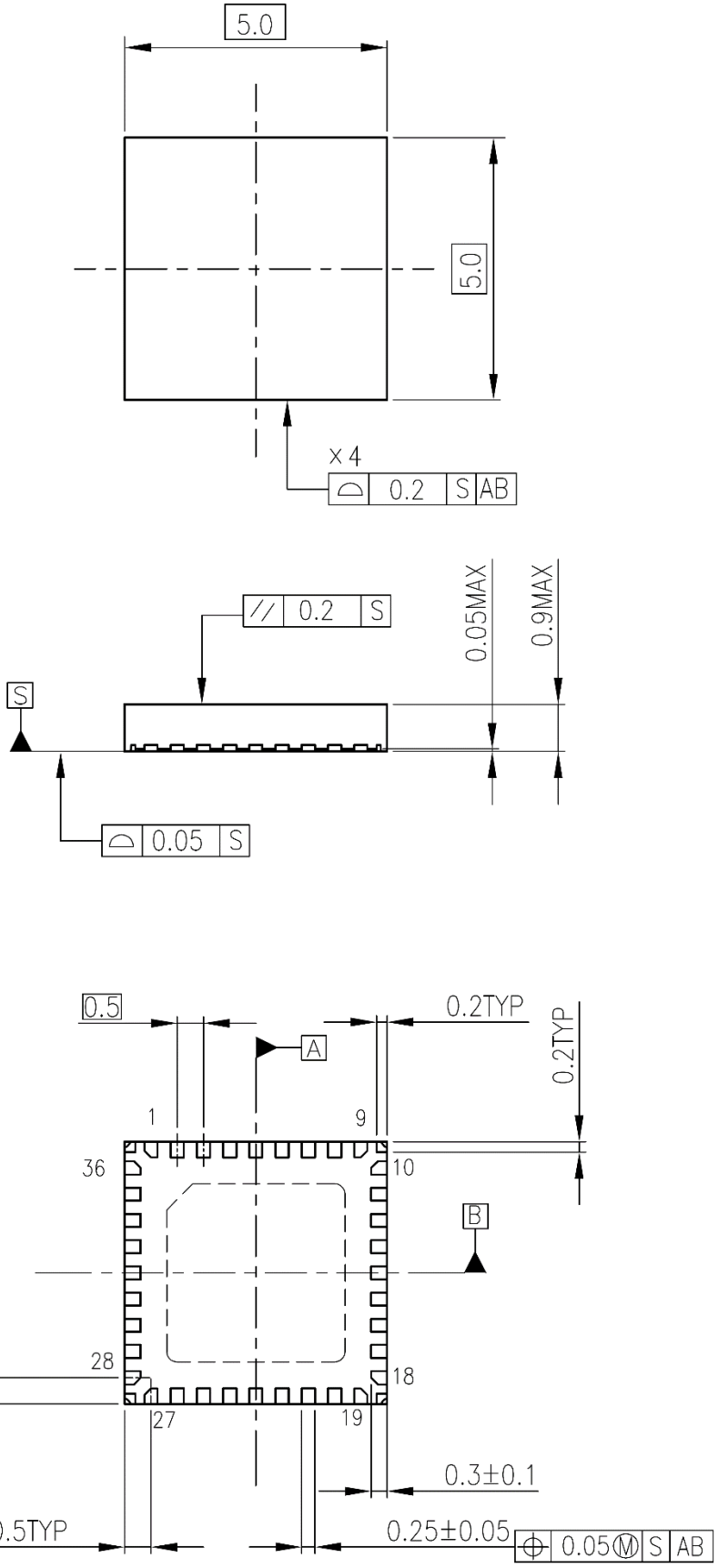
Electrical characteristics (V_{CC} = 24 V, Ta = 25°C)

Characteristics		Symbol	Test condition	Min.	Typ.	Max.	unit
Supply current		I_{CC1}	START	3.5	4.6	6.5	mA
		I_{CC2}	STOP	1.0	1.7	2.5	
Hall Amp	Common mode input voltage range	VCMRH	-	0.5	-	3.4	V
	Input amplitude range	VH	-	50	-	-	mVpp
	Input hysteresis	VhysH	-	8	16	24	mV
	Input current	IinH	VCMRH = 2.5 V, single phase	0	-	1	μA
HP output	Output ON voltage	VO(HP)	I(HP) = 2 mA	-	-	0.5	V
Control input circuit	Input voltage 1(H)	Vin1(H)	CW/CCW,BRAKE,START, PWM-in	2.2	-	5.5	V
	Input voltage 2(H)	Vin2(H)	OVP	2.2	-	Vreg	
	Input voltage (L)	Vin(L)	CW/CCW,BRAKE,START, PWM-in,OVP	0	-	0.8	
	Input current (H)	Iin1(H)	CW/CCW,BRAKE,START ,CLd, Dif-in, PWM-in, Vin = Vreg	0	-	1	μA
	Input current (L)	Iin1(L)	CW/CCW,BRAKE,START PWM-in, Vin = GND	70	100	150	
		Iin2(L)	DIf-In, CLd = GND	0	-	1	
Charge pump voltage		VG	CP1-CP2: 0.047 μF, CP3: 0.1 μF	Vcc+7	Vcc+8	Vcc+9	V
Energization signal output voltage		VO (U)-(H)	LA (U)/LB (U)/LC (U),Io = 1 mA	VG −1.5	-	VG	V
		VO (U)-(L)	LA (U)/LB (U)/LC (U), Io = 5 mA	0.1	-	0.825	
		VO (L)-(H)	LA (L) /LB (L) /LC (L), Io = 1 mA	6.9	7.7	8.5	
		VO (L)-(L)	LA (L) /LB (L) /LC (L), Io = 5 mA	0.1	-	0.775	
Internal voltage source output		Vreg	Ireg = 10 mA	4.5	5.0	5.5	V
Over current limitation circuit reference voltage		Vdc	-	0.23	0.25	0.27	V
Internal reference clock frequency		fx	R = 10 kΩ, C = 47 pF	4.5	5.0	5.5	MHz
Dead time		TOFF1	R = 10 kΩ, C = 47 pF	0.9	1.2	1.5	μs
		TOFF2	R = 10 kΩ, C = 47 pF	0.9	1.2	1.5	
Lead angle control circuit	Upper side clump lead angle	ACLH	-	-	29	-	°

Package dimensions

P-VQFN36-0505-0.50-001

Unit: mm



Weight: 0.08 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

(5) Others

Utmost care is necessary in the design of the output, V_{CC}, VM, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.

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