VTM™ Current Multiplier

VTM48Ex120y025A0R

High-Efficiency, Bidirectional Sine Amplitude Converter

Features & Benefits

- 48V_{DC} to 12V_{DC} 25A bidirectional current multiplier
- Can power a load connected to either the primary or secondary side
- High efficiency (>96%) reduces system power consumption
- High density (85A/in^3)
- "Full Chip" VI Chip® package enables surface mount, low-impedance interconnect to system board
- Contains built-in protection features against:
  - Overvoltage Lockout
  - Overcurrent
  - Short Circuit
  - Overtemperature
- Provides enable / disable control, internal temperature monitoring
- ZVS / ZCS resonant Sine Amplitude Converter topology
- Less than 50°C temperature rise at full load in typical applications

Typical Applications

- High-End Computing Systems
- Automated Test Equipment
- High-Density Power Supplies
- Communications Systems

Product Ratings	
V_{PRI} = 26 – 55V	I_{SEC} = 25A (Nominal)
V_{SEC} = 6.5 – 13.8V (No Load)	K = 1/4

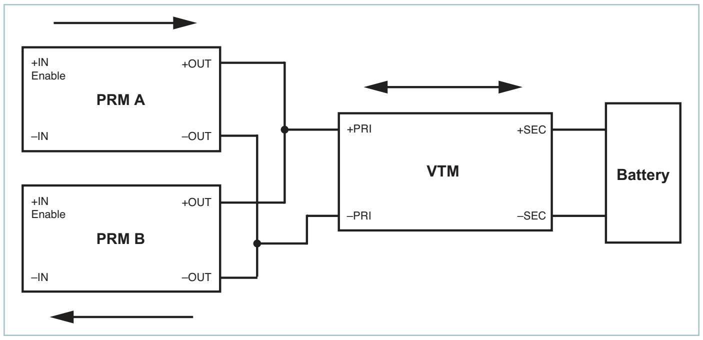
Product Description

The VI Chip® bidirectional current multiplier is a Sine Amplitude Converter (SAC™) operating from a 26 to 55V_{DC} primary source or a 6.5 to 13.8V_{DC} secondary source to power a load. The bidirectional Sine Amplitude Converter isolates and transforms voltage at a secondary:primary ratio of 1/4. The SAC offers a low AC impedance beyond the bandwidth of most downstream regulators; therefore for a step-down conversion; capacitance normally at the load can be located at the source to the Sine Amplitude Converter to enable a reduction in size of capacitors. Since the K factor of the VTM48EF120T025A0R is 1/4, the capacitance value on the primary side can be reduced by a factor of 16 in an application where the source is located on the primary side, resulting in savings of board area, materials and total system cost.

The VTM48EF120T025A0R is provided in a VI Chip package compatible with standard pick-and-place and surface mount assembly processes. The co-molded VI Chip package provides enhanced thermal management due to a large thermal interface area and superior thermal conductivity. The high conversion efficiency of the VTM48EF120T025A0R increases overall system efficiency and lowers operating costs compared to conventional approaches.

The VTM48EF120T025A0R enables the utilization of Factorized Power Architecture™ which provides efficiency and size benefits by lowering conversion and distribution losses and promoting high-density point-of-load conversion.

Typical Application



Part Numbering

Product Number	Package Style (x)	Product Grade (y)
VTM48Ex120y025A0R	**F** = J-Lead	**T** = –40 to 125°C
	T = Through hole	**M** = –55 to 125°C

For Storage and Operating Temperatures see General Characteristics Section

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	MPRI	Max	Unit
+PRI to –PRI		–1.0	60	V_{DC}
PC to –PRI		–0.3	20	V_{DC}
TM to –PRI		–0.3	7	V_{DC}
VC to –PRI		–0.3	20	V_{DC}
+PRI / –PRI to +SEC / –SEC (hipot)			2250	V_{DC}
+SEC to –SEC		–1.0	16	V_{DC}

Primary-Source Electrical Specifications

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C < T_J < 125°C (T-Grade). All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain						
Primary Voltage Range	V_{PRI}	No external VC applied	**26**		**55**	V_{DC}
		VC applied	**0**		**55**	
V_{PRI} Slew Rate	dV_{PRI} / dt				**1**	V / µs
V_{PRI} UV Turn Off	V_{PRI_UV}	Module latched shutdown, No external VC applied, I_{SEC} = 25A		24	**26**	V
No Load Power Dissipation	P_{NL}	V_{PRI} = 48V	**3**		**15.0**	W
		V_{PRI} = 26 – 55V			**17**	
		V_{PRI} = 48V, T_C = 25°C		5.3	6.5	
		V_{PRI} = 26 – 55V, T_C = 25°C			9	
Inrush Current Peak	I_{INRP}	VC enable, V_{PRI} = 48V, C_{SEC} = 1000µF, R_{LOAD} = 471mΩ		10	**20**	A
DC Primary Current	I_{PRI_DC}				**7**	A
Transfer Ratio	K	$K = V_{SEC} / V_{PRI}$, I_{SEC} = 0A		1/4		V / V
Secondary Voltage	V_{SEC}	$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R_{SEC}$				V
Secondary Current (Average)	I_{SEC_AVG}				**25**	A
Secondary Current (Peak)	I_{SEC_PK}	t_{PEAK} < 10ms, $I_{SEC\_AVG} \leq$ 25A			**37.5**	A
Secondary Power (Average)	P_{SEC_AVG}	$I_{SEC\_AVG} \leq$ 25A			**300**	W
Efficiency (Ambient)	η_{AMB}	V_{PRI} = 48V, I_{SEC} = 25A	95.0	96.0		%
		V_{PRI} = 26 – 55V, I_{SEC} = 25A	93.0			
		V_{PRI} = 48V, I_{SEC} = 12.5A	94.5	95.5		
Efficiency (Hot)	η_{HOT}	V_{PRI} = 48V, T_C = 100°C, I_{SEC} = 25A	94.5	95.6		%
Efficiency (Over Load Range)	$\eta_{20\%}$	5A < I_{SEC} < 25A	**80.0**			%

Primary-Source Electrical Specifications (Cont.)

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C < T_J < 125°C (T-Grade). All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain (Cont.)						
Secondary Resistance (Cold)	R_{SEC_COLD}	T_C = –40°C, I_{SEC} = 25A	4.9	7.5	12.0	mΩ
Secondary Resistance (Ambient)	R_{SEC_AMB}	T_C = 25°C, I_{SEC} = 25A	6.3	9.0	14.0	mΩ
Secondary Resistance (Hot)	R_{SEC_HOT}	T_C = 100°C, I_{SEC} = 25A	8.8	11.5	16.0	mΩ
Switching Frequency	F_{SW}		**1.85**	1.95	**2.05**	MHz
Secondary Ripple Frequency	F_{SW_RP}		**3.70**	3.90	**4.10**	MHz
Secondary Voltage Ripple	V_{SEC_PP}	C_{SEC} = 0F, I_{SEC} = 25A, V_{PRI} = 48V, 20MHz BW		150	**285**	mV
Secondary Inductance (Parasitic)	L_{SEC_PAR}	Frequency up to 30MHz, Simulated J-lead model		600		pH
Secondary Capacitance (Internal)	C_{SEC_INT}	Effective Value at 12V_{SEC}		47		µF
Secondary Capacitance (External)	C_{SEC_EXT}	VTM Standalone Operation. V_{PRI} pre-applied, VC enable			1000	µF
Protection						
Primary Overvoltage Lockout	V_{PRI_OVLO+}	Module latched shutdown	**55.1**	58.5	**60.0**	V
Primary Overvoltage Lockout Response Time Constant	t_{OVLO}	Effective internal RC filter		8		µs
Secondary Overcurrent Trip	I_{OCP_SEC}		**39**	47		A
Secondary Short Circuit Protection Trip Current	I_{SCP_SEC}		39			A
Secondary Overcurrent Response Time Constant	t_{OCP_SEC}	Effective internal RC filter (Integrative)		5.3		ms
Secondary Short Circuit Protection Response Time	t_{SCP_SEC}	From detection to cessation of switching (Instantaneous)		1		µs
Thermal Shutdown Set Point	T_{J_OTP}		125	130	135	°C

Secondary-Source Electrical Specifications

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C < T_J < 125°C (T-Grade). All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain						
Secondary Voltage Range	V_{SEC}	No external VC applied	**6.5**		**13.75**	V_{DC}
		VC applied	**0**		**13.75**	
V_{SEC} Slew Rate	dV_{SEC} / dt				**1**	V / µs
V_{SEC} UV Turn Off	V_{SEC_UV}	Module latched shutdown, No external VC applied, I_{PRI} = 6.3A		6.0	**6.5**	V
No Load Power Dissipation	P_{NL_SEC}	V_{SEC} = 12V	**3**		**15.0**	W
		V_{SEC} = 6.5 – 13.75V			**17.0**	
		V_{SEC} = 12V, T_C = 25°C		5.3	**6.5**	
		V_{SEC} = 6.5 – 13.75V, T_C = 25°C			9.0	
Inrush Current Peak	$I_{NR\_SEC\_P}$	VC enable, V_{SEC} = 12V, C_{PRI} = 63µF, R_{LOAD} = 7mΩ		40	**80**	A
DC Secondary Current	I_{SEC_DC}				**28.0**	A
Primary Voltage	V_{PRI}	$V_{PRI} = V_{SEC} / K - I_{PRI} \bullet R_{PRI}$				V
Primary Current (Average)	I_{PRI_AVG}				**6.3**	A
Primary Current (Peak)	I_{PRI_PK}	t_{PEAK} < 10ms, $I_{PRI\_AVG} \leq$ 6.3A			**9.4**	A
Primary Power (Average)	P_{PRI_AVG}	$I_{PRI\_AVG} \leq$ 6.3A			**300**	W
Efficiency (Ambient)	η_{AMB}	V_{SEC} = 12V, I_{PRI} = 6.3A	95	96.0		%
		V_{SEC} = 6.5 – 13.75V, I_{PRI} = 6.3A	93			
		V_{SEC} = 12V, I_{PRI} = 3.1A	94.5	95.5		
Efficiency (Hot)	η_{HOT}	V_{SEC} = 12V, T_C = 100°C, I_{PRI} = 6.3A	94.5	95.6		%
Efficiency (Over Load Range)	$\eta_{20\%}$	1.3A < I_{PRI} < 6.3A	**80.0**			%
Primary Resistance (Cold)	R_{PRI_COLD}	T_C = –40°C, I_{PRI} = 6.3A	145	165	185	mΩ
Primary Resistance (Ambient)	R_{PRI_AMB}	T_C = 25°C, I_{PRI} = 6.3A	165	195	225	mΩ
Primary Resistance (Hot)	R_{PRI_HOT}	T_C = 100°C, I_{PRI} = 6.3A	200	238	275	mΩ
Primary Voltage Ripple	V_{PRI_PP}	C_{PRI} = 0F, I_{PRI} = 6.3A, V_{SEC} = 12V, 6.5MHz BW			**650**	mV
Primary Capacitance (External)	C_{PRI_EXT}	VTM Standalone Operation. V_{SEC} pre-applied, VC enable			63	µF
Protection						
Secondary Overvoltage Lockout	V_{SEC_OVLO+}	Module latched shutdown	14.5	14.8	15.0	V
Secondary Overvoltage Lockout Response Time Constant	t_{OVLO_SEC}	Effective internal RC filter		8		µs
Primary Overcurrent Trip	I_{OCP_PRI}		**7**	9	**14**	A
Primary Short Circuit Protection Trip Current	I_{SCP_PRI}		7			A
Primary Overcurrent Response Time Constant	t_{OCP_PRI}	Effective internal RC filter (Integrative)		5.3		ms
Primary Short Circuit Protection Response Time	t_{SCP_PRI}	From detection to cessation of switching (Instantaneous)		1		µs

Signal Characteristics

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_J < 125°C (T-Grade). All other specifications are at T_J = 25°C unless otherwise noted.

VTM Control: VC

- Referenced to –PRI
- Used to wake up powertrain circuit.
- A minimum of 11.5V must be applied indefinitely for V_{PRI} < 26V to ensure normal operation.
- VC slew rate must be within range for a successful start.
- PRM™ VC can be used as valid wake-up signal source.
- Internal Resistance used in “Adaptive Loop” compensation.
- VC voltage may be continuously applied.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
ANALOG INPUT	Steady	External VC Voltage	V_{VC_EXT}	Required for start up and operation below 26V.	**11.5**		**16.5**	V
		VC Current Draw	I_{VC}	VC = 11.5V, V_{PRI} = 0V		130	**150**	mA
				VC = 11.5V, V_{PRI} > 26V		25		
				VC = 16.5V, V_{PRI} > 26V		115		
				Fault mode. VC > 11.5V		60		
		VC Internal Diode Rating	D_{VC_INT}			100		V
		VC Internal Resistor	$R_{VC\text{-}INT}$			0.511		kΩ
		VC Internal Resistor Temperature Coefficient	T_{VC_COEFF}				3900	ppm/°C
	Start Up	VC Start-Up Pulse	V_{VC_SP}	t_{PEAK} < 18ms			20	V
		VC Slew Rate	dVC/dt	Required for proper start up	**0.02**		**0.25**	V / µs
		VC Inrush Current	I_{INR_VC}	VC = 16.5V, dVC/dt = 0.25V/µs			**1**	A
	Transitional	VC to V_{SEC} Turn-On Delay	t_{ON}	V_{PRI} pre-applied, PC floating, VC enable, C_{PC} = 0µF			**500**	µs
		VC to PC Delay	t_{VC_PC}	VC = 11.5V to PC high, V_{PRI} = 0V, dVC/dt = 0.25V/µs		75	125	µs
		Internal VC Capacitance	C_{VC_INT}	VC = 0V		3.2		µF

Primary Control: PC

- Referenced to –PRI
- The PC pin enables and disables the VTM. When held below 2V, the VTM will be disabled.
- PC pin outputs 5V during normal operation. PC pin is equal to 2.5V during fault mode given V_{PRI} > 26V or VC > 11.5V.
- After successful start up and under no-fault condition, PC can be used as a 5V regulated voltage source with a 2mA maximum current.
- Module will shutdown when pulled low with an impedance less than 400Ω.
- In an array of VTMs, connect PC pin to synchronize start up.
- PC pin cannot sink current and will not disable other modules during fault mode.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
ANALOG OUTPUT	Steady	PC Voltage	V_{PC}		**4.7**	5.0	**5.3**	V
		PC Source Current	I_{PC_OP}				2	mA
		PC Resistance (Internal)	R_{PC_INT}	Internal pull-down resistor	**50**	150	**400**	kΩ
	Start Up	PC Source Current	I_{PC_EN}		**50**	100	**300**	µA
		PC Capacitance (Internal)	C_{PC_INT}				**1000**	pF
		PC Resistance (External)	R_{PC_S}		**60**			kΩ
DIGITAL INPUT / OUTPUT	Enable	PC Voltage	V_{PC_EN}		**2**	2.5	**3**	V
	Disable	PC Voltage (Disable)	V_{PC_DIS}				**2**	V
		PC Pull-Down Current	I_{PC_PD}		**5.1**			mA
	Transitional	PC Disable Time	$t_{PC\_DIS\_T}$			5		µs
		PC Fault-Response Time	t_{FR_PC}	From fault to PC = 2V		100		µs

Signal Characteristics (Cont.)

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_J < 125°C (T-Grade). All other specifications are at T_J = 25°C unless otherwise noted.

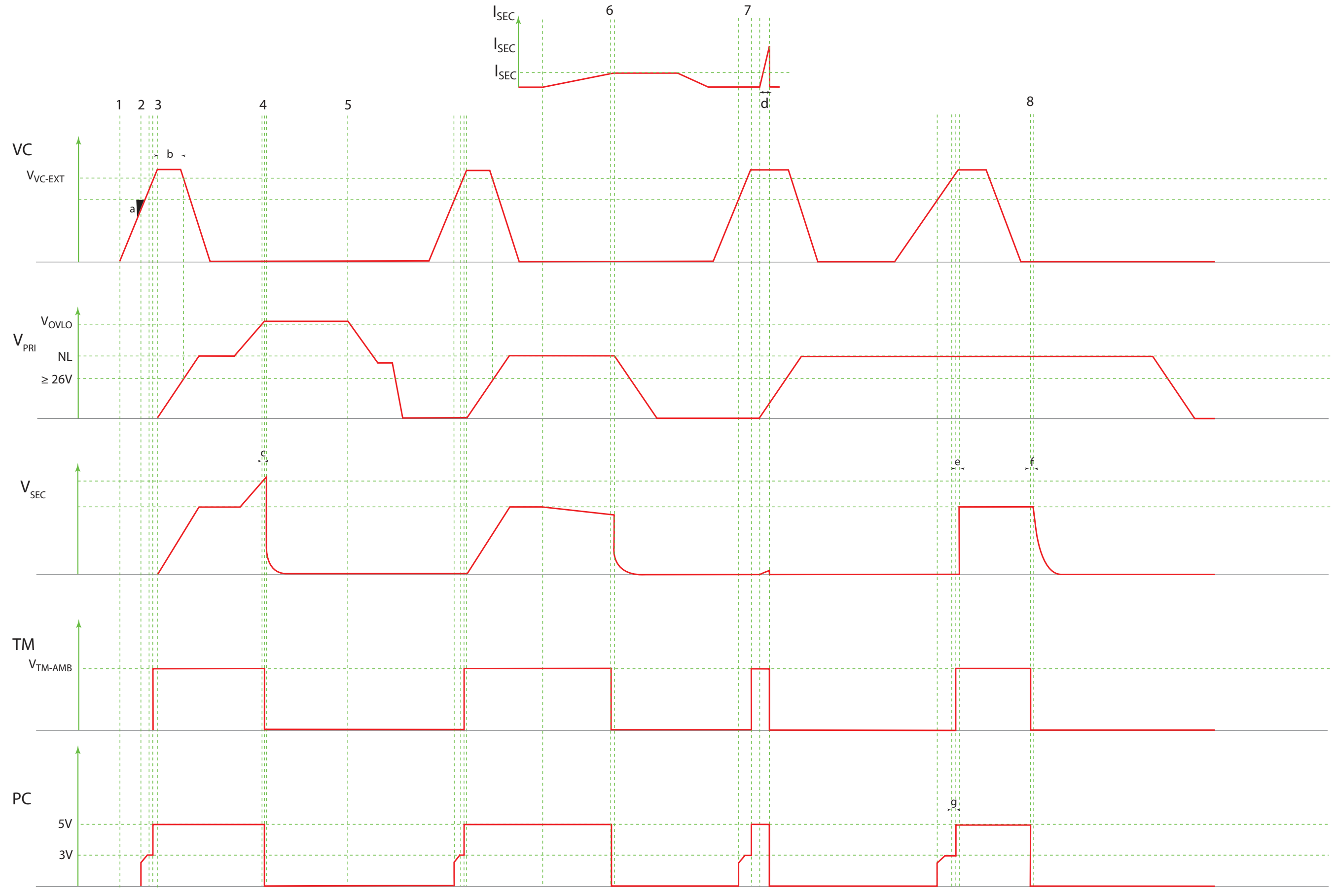
Temperature Monitor: TM

- Referenced to –PRI
- The TM pin monitors the internal temperature of the VTM controller IC within an accuracy of ±5°C.
- Can be used as a "Power Good" flag to verify that the VTM is operating.
- The TM pin has a room-temperature set point of 3V and approximate gain of 10mV/°C.
- Output drives Temperature Shutdown comparator.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
ANALOG OUTPUT	Steady	TM Voltage	V_{TM_AMB}	T_J controller = 27°C	2.95	3.00	3.05	V
		TM Source Current	I_{TM}				**100**	µA
		TM Gain	A_{TM}			10		mV/°C
		TM Voltage Ripple	V_{TM_PP}	C_{TM} = 0F, V_{PRI} = 48V, I_{SEC} = 25A		120	**200**	mV
DIGITAL OUTPUT (FAULT FLAG)	Disable	TM Voltage	V_{TM_DIS}			0		V
	Transitional	TM Resistance (Internal)	R_{TM_INT}	Internal pull-down resistor	**25**	40	**50**	kΩ
		TM Capacitance (External)	C_{TM_EXT}				**50**	pF
		TM Fault-Response Time	t_{FR_TM}	From fault to TM = 1.5V		10		µs

Timing Diagram

Power sourced from the primary side.



a: VC slew rate (dVC/dt)
b: Minimum VC pulse rate
c: t_{OVLO_PIN}
d: t_{OCP_SEC}
e: Secondary turn on delay (t_{ON})
f: PC disable time ($t_{PC\_DIS\_t}$)
g: VC to PC delay (t_{VC_PC})

1. Initiated VC pulse
2. Controller start
3. V_{PRI} ramp up
4. $V_{PRI} = V_{OVLO}$
5. V_{PRI} ramp down no VC pulse
6. Overcurrent, Secondary
7. Start up on short circuit
8. PC driven low

Notes:
– Timing and voltage is not to scale
– Error pulse width is load dependent

Application Characteristics

The following values, typical of an application environment, are collected at T_C = 25°C with power sourced from the primary side unless otherwise noted. See associated figures for general trend data.

Attribute	Symbol	Conditions / Notes	Typ	Unit
Powertrain				
No-Load Power Dissipation	P_{NL}	V_{PRI} = 48V, PC enabled	5.1	W
Efficiency (Ambient)	η_{AMB}	V_{PRI} = 48V, I_{SEC} = 25A	96.1	%
Efficiency (Hot)	η_{HOT}	V_{PRI} = 48V, I_{SEC} = 25A, T_C = 100°C	95.6	%
Secondary Resistance (Cold)	R_{SEC_COLD}	V_{PRI} = 48V, I_{SEC} = 25A, T_C = –40°C	7.3	mΩ
Secondary Resistance (Ambient)	R_{SEC_AMB}	V_{PRI} = 48V, I_{SEC} = 25A	9.3	mΩ
Secondary Resistance (Hot)	R_{SEC_HOT}	V_{PRI} = 48V, I_{SEC} = 25A, T_C = 100°C	11.6	mΩ
Secondary Voltage Ripple	V_{SEC_PP}	C_{SEC} = 0F, I_{SEC} = 25A, V_{PRI} = 48V, 20MHz BW	198	mV
V_{SEC} Transient (Positive)	V_{SEC_TRAN+}	I_{SEC_STEP} = 0 – 25A, V_{PRI} = 48V, I_{SLEW} = 17A/µs	650	mV
V_{SEC} Transient (Negative)	$V_{SEC\_TRAN–}$	I_{SEC_STEP} = 25 – 0A, V_{PRI} = 48V, I_{SLEW} = 212A/µs	310	mV

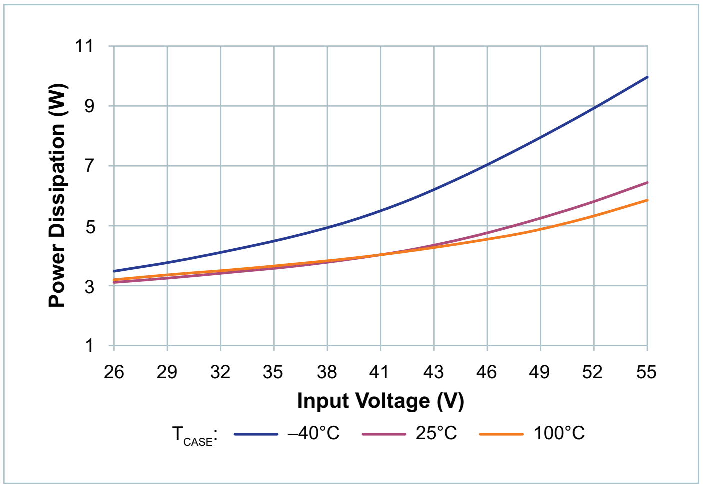


Figure 1 — *No load power dissipation vs. V_{PRI}*

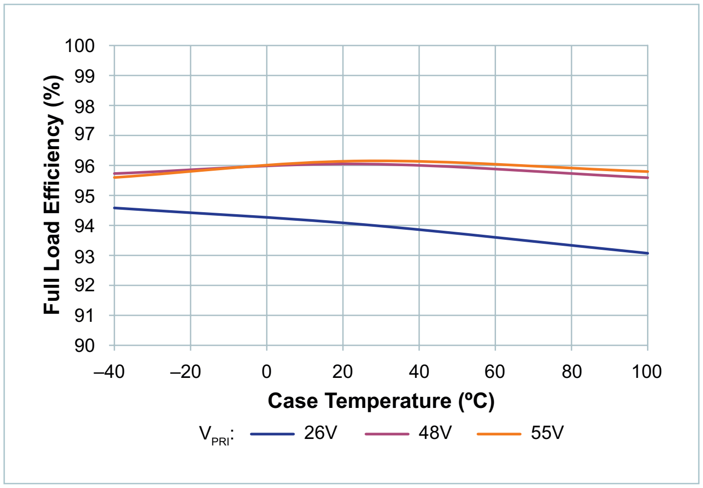


Figure 2 — *Full load efficiency vs. temperature*

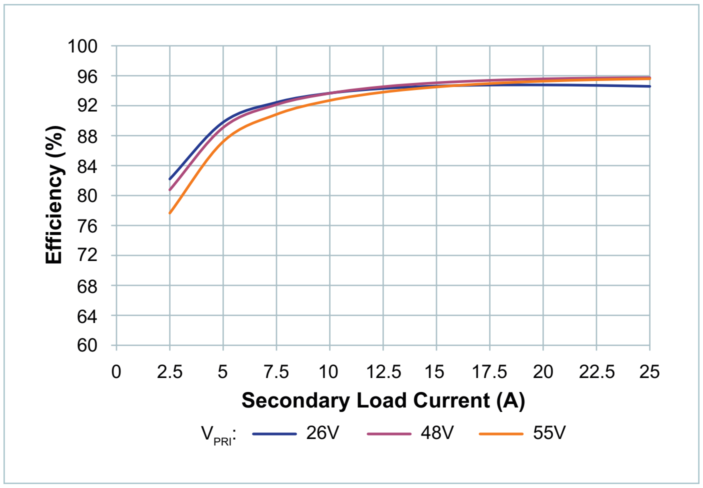


Figure 3 — *Efficiency at –40°C*

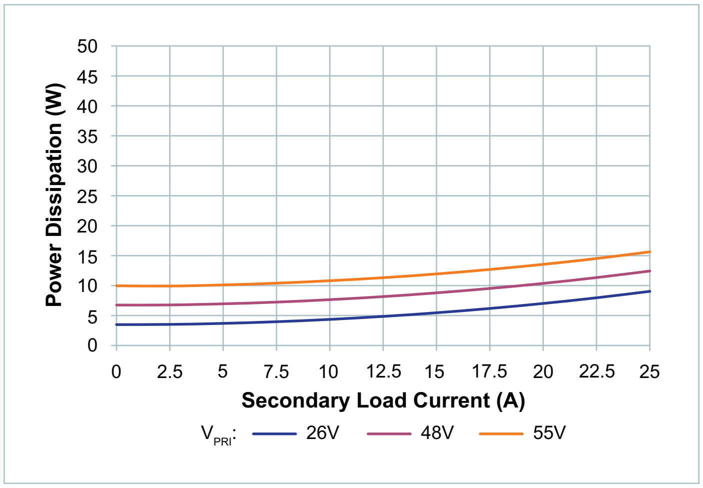


Figure 4 — *Power dissipation at –40°C*

Application Characteristics (Cont.)

The following values, typical of an application environment, are collected at T_C = 25°C with power sourced from the primary side unless otherwise noted. See associated figures for general trend data.

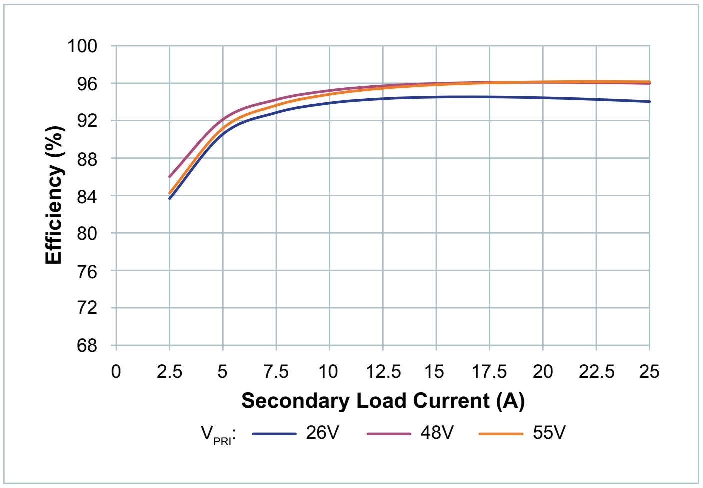


Figure 5 — *Efficiency at 25°C*

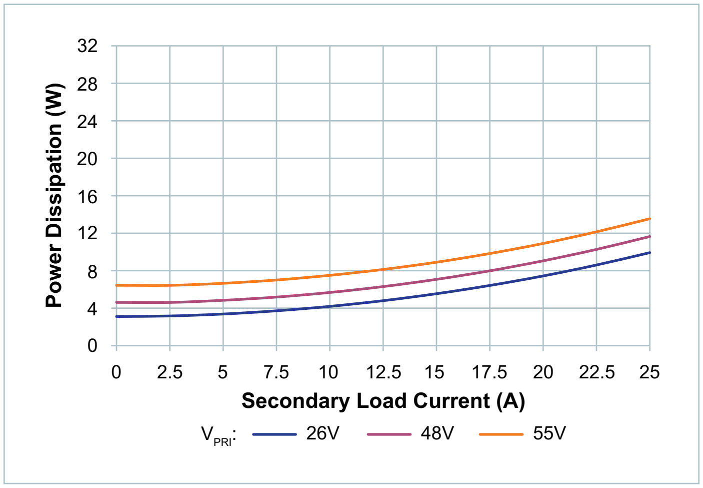


Figure 6 — *Power dissipation at 25°C*

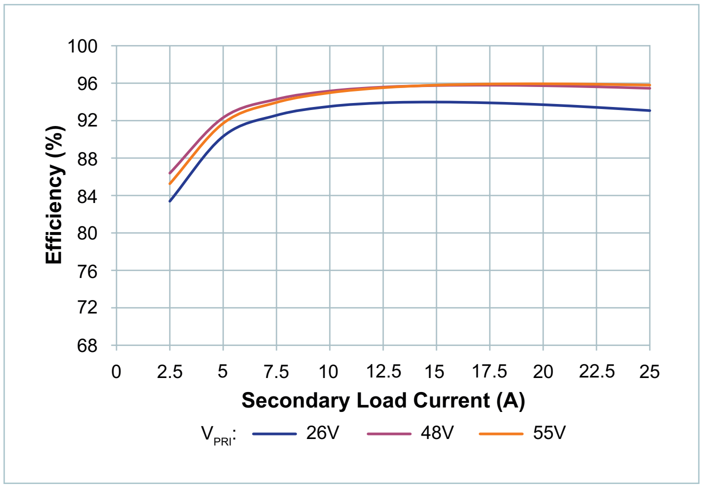


Figure 7 — *Efficiency at 100°C*

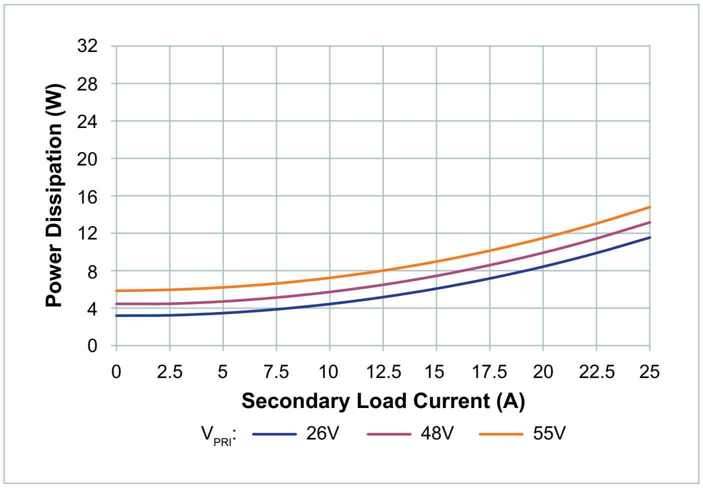


Figure 8 — *Power dissipation at 100°C*

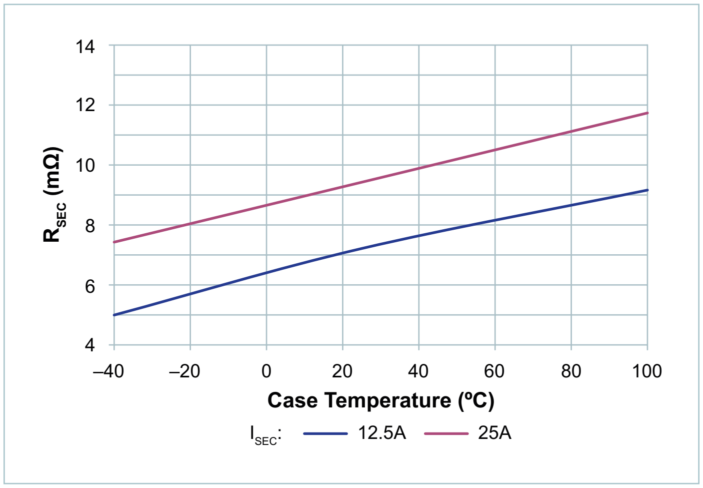


Figure 9 — *R_{SEC} vs. temperature*

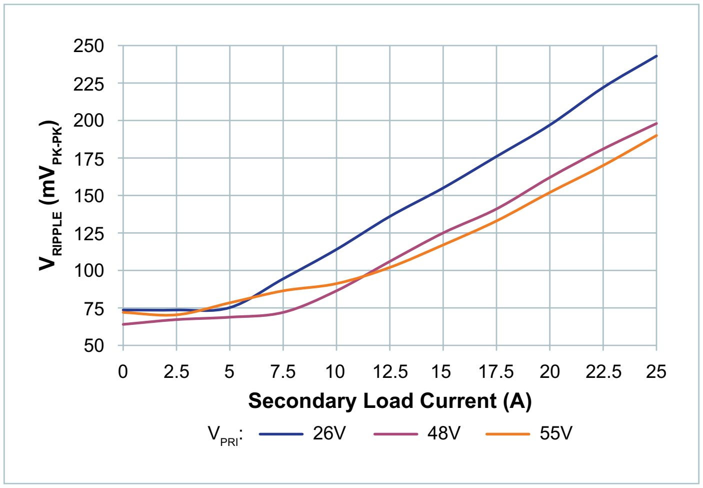


Figure 10 — *V_{RIPPLE} vs. I_{SEC}; No external C_{SEC}. Board mounted module, scope setting: 20MHz analog BW*

Application Characteristics (Cont.)

The following values, typical of an application environment, are collected at T_C = 25°C with power sourced from the primary side unless otherwise noted. See associated figures for general trend data.

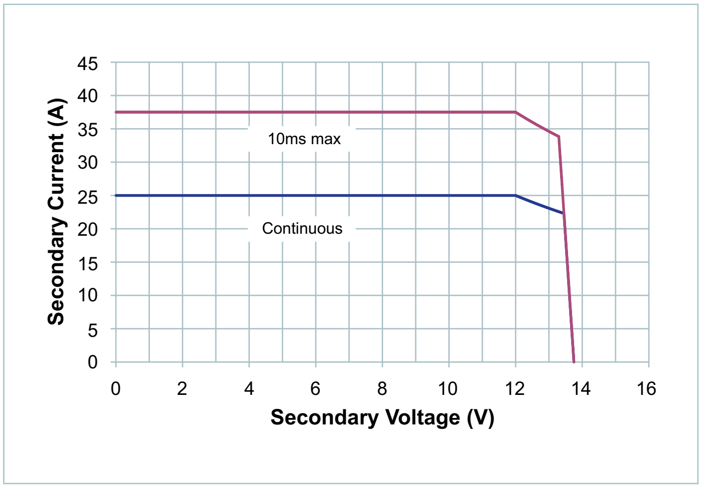


Figure 11 — *Safe operating area*

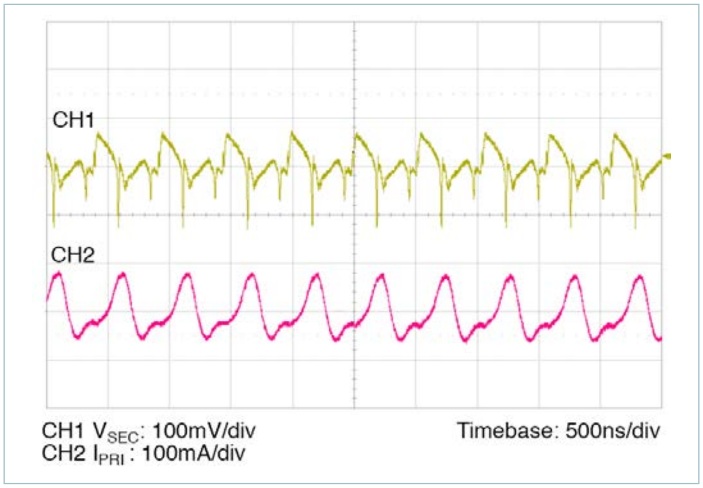


Figure 12 — *Full load ripple, 100µF C_{PRI}; No external C_{SEC}. Board-mounted module, scope setting: 20MHz analog BW*

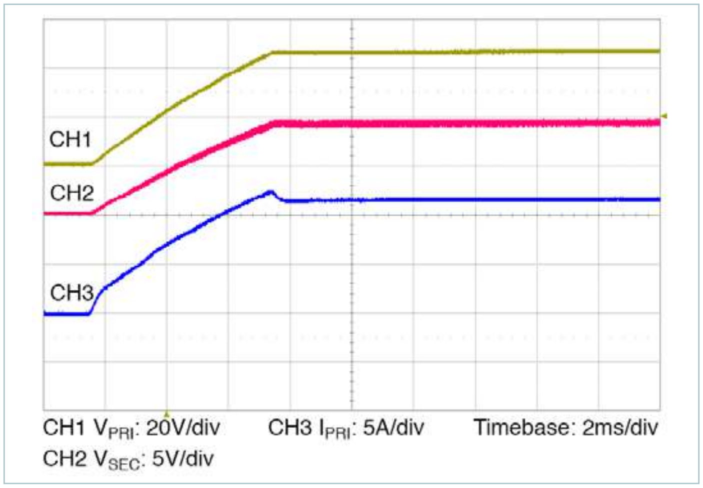


Figure 13 — *Start up from application of V_{PRI}; VC pre-applied C_{SEC} = 1000µF*

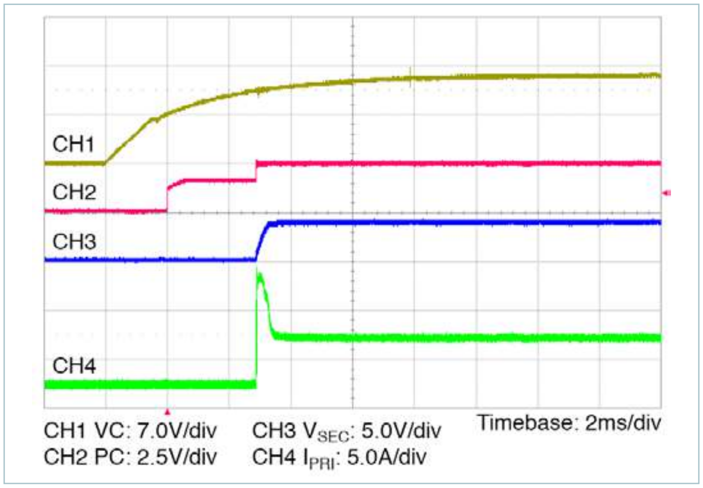


Figure 14 — *Start up from application of VC; V_{PRI} pre-applied C_{SEC} = 1000µF*

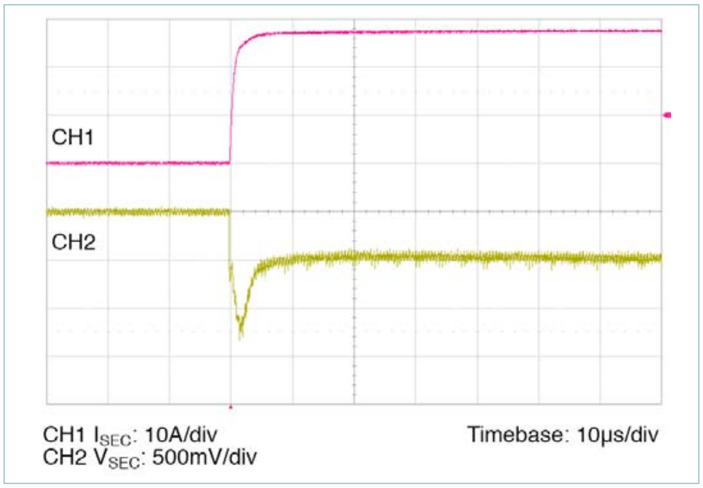


Figure 15 — *0A – Full load transient response: C_{PRI} = 100µF, no external C_{SEC}*

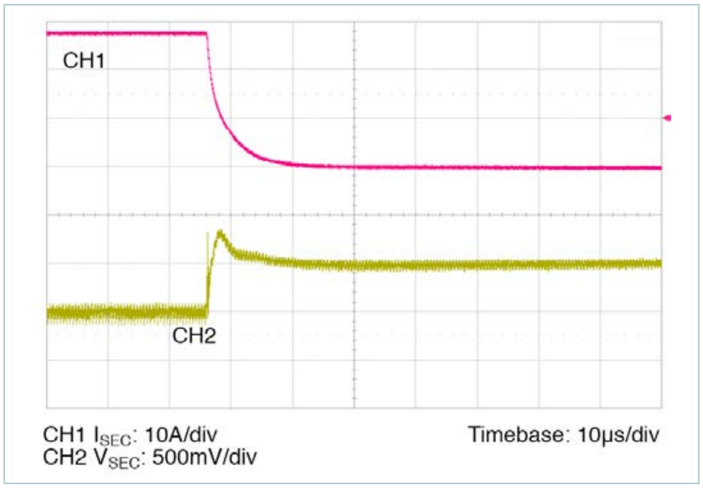


Figure 16 — *Full load – 0A transient response: C_{PRI} = 100µF, no external C_{SEC}*

General Characteristics

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C < T_J < 125 °C (T-Grade). All Other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		32.25 [1.270]	32.5 [1.280]	32.75 [1.289]	mm [in]
Width	W		21.75 [0.856]	22.0 [0.866]	22.25 [0.876]	mm [in]
Height	H		6.48 [0.255]	6.73 [0.265]	6.98 [0.275]	mm [in]
Volume	Vol	No heat sink		4.81 [0.294]		cm^3 [in^3]
Weight	W			15.0 [0.53]		g [oz]
Lead Finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
Thermal						
Operating Temperature	T_J	VTM48EF120T025A0R (T-Grade)	–40		125	°C
		VTM48EF120M025A0R (M-Grade)	–55		125	
		VTM48ET120T025A0R (T-Grade)	–40		125	
		VTM48ET120M025A0R (M-Grade)	–55		125	
Thermal Resistance	θ_{JC}	Isothermal heat sink and isothermal internal PCB		1		°C / W
Thermal Capacity				5		Ws / °C
Assembly						
Peak Compressive Force Applied to Case (Z-Axis)		Supported by J-Lead only			6	lbs
					5.41	lbs / in^2
Storage Temperature	T_{ST}	VTM48EF120T025A0R (T-Grade)	–40		125	°C
		VTM48EF120M025A0R (M-Grade)	–65		125	
		VTM48ET120T025A0R (T-Grade)	–40		125	
		VTM48ET120M025A0R (M-Grade)	–65		125	
ESD Withstand	ESD_{HBM}	Human Body Model, JEDEC JESD 22-A114-F	1000			V_{DC}
	ESD_{CDM}	Charge Device Model, JEDEC JESD 22-C101-D	400			
Soldering						
Peak Temperature During Reflow		MSL 4 (Datecode 1528 and later)			245	°C
Peak Time Above 217°C				60	90	s
Peak Heating Rate During Reflow				1.5	3	°C / s
Peak Cooling Rate Post Reflow				1.5	6	°C / s
Safety						
Isolation Voltage (Hipot)	V_{HIPOT}		**2250**			V_{DC}
Isolation Capacitance	C_{PRI_SEC}	Unpowered unit	**2500**	3200	**3800**	pF
Isolation Resistance	R_{PRI_SEC}		**10**			MΩ
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		6.03		MHrs
		Telcordia Issue 2 - Method I Case 1; Ground Benign, Controlled		7.94		MHrs
Agency Approvals / Standards		cTÜVus EN 60950-1				
		cURus UL 60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

Using the Control Signals VC, PC, TM

The VTM Control (VC) pin is a primary-referenced pin which powers the internal VCC circuitry when within the specified voltage range of 11.5 – 16.5V. This voltage is required for VTM current multiplier start up and must be applied as long as the primary is below 26V. In order to ensure a proper start, the slew rate of the applied voltage must be within the specified range.

Some additional notes on the using the VC pin:

- In most applications, the VTM module primary side will be powered by an upstream PRM™ regulator which provides a 10ms VC pulse during start up. In these applications the VC pins of the PRM regulator and VTM current multiplier should be tied together.
- In bidirectional applications, the primary of the VTM may also be providing power to a PRM input. In these applications, a proper VC voltage within the specified range must be applied any time the primary voltage of the VTM is below 26V.
- The VC voltage can be applied indefinitely allowing for continuous operation down to $0V_{PRI}$.
- The fault response of the VTM module is latching. A positive edge on VC is required in order to restart the unit. If VC is continuously applied the PC pin may be toggled to restart the VTM module.

Primary Control (PC) is a primary-referenced pin that can be used to accomplish the following functions:

- *Delayed start:* Upon the application of VC, the PC pin will source a constant 100µA current to the internal RC network. Adding an external capacitor will allow further delay in reaching the 2.5V threshold for module start.
- *Auxiliary voltage source:* Once enabled in regular operational conditions (no fault), each VTM PC provides a regulated 5V, 2mA voltage source.
- *Disable:* PC pin can be actively pulled down in order to disable the module. Pull-down impedance shall be lower than 400Ω.
- *Fault detection flag:* The PC 5V voltage source is internally turned off as soon as a fault is detected. It is important to notice that PC doesn't have current sink capability. Therefore, in an array, PC line will not be capable of disabling neighboring modules if a fault is detected.
- *Fault reset:* PC may be toggled to restart the unit if VC is continuously applied.

Temperature Monitor (TM) is a primary-referenced pin that provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- *Monitor the control IC temperature:* The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e., 3.0V = 300K = 27°C). If a heat sink is applied, TM can be used to thermally protect the system.
- *Fault detection flag:* The TM voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of TM signal.

Start-Up Behavior

Depending on the sequencing of the VC with respect to the same voltage, whether the source is on the primary or secondary, the behavior during start up will vary as follows:

- *Normal operation (VC applied prior to the source voltage):* In this case the controller is active prior to the source ramping. When the source voltage is applied, the VTM module load voltage will track the source (See Figure 13). The inrush current is determined by the source voltage rate of rise and load capacitance. If the VC voltage is removed prior to the primary voltage reaching 26V, the VTM may shut down.
- *Stand-alone operation (VC applied after V_{PRI}):* In this case the VTM secondary will begin to rise upon the application of the VC voltage (See Figure 14). The Adaptive Soft-Start Circuit may vary the secondary voltage rate of rise in order to limit the inrush current to its maximum level. When starting into high capacitance or a short, the secondary current will be limited for a maximum of 1200µs. After this period, the Adaptive Soft-Start Circuit will time out and the VTM module may shut down. No restart will be attempted until VC is re-applied or PC is toggled. The maximum secondary capacitance is limited to 1000µF in this mode of operation to ensure a successful start.

Thermal Considerations

VI Chip® products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the line/load conditions, thermal management and environmental conditions. Maintaining the top of the VTM48EF120T025A0R case to less than 100°C will keep all junctions within the VI Chip module below 125°C for most applications.

The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a VI Chip module for an extended period of time at full load without proper heat sinking.

Sine Amplitude Converter Point-of-Load Conversion

The Sine Amplitude Converter (SAC) uses a high-frequency resonant tank to move energy from primary to secondary. (The resonant tank is formed by Cr and leakage inductance Lr in the power transformer windings.) The resonant LC tank, operated at high frequency, is amplitude modulated as a function of primary voltage and secondary current. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving power density.

The VTM48EF120T025A0R SAC can be simplified into the following model:

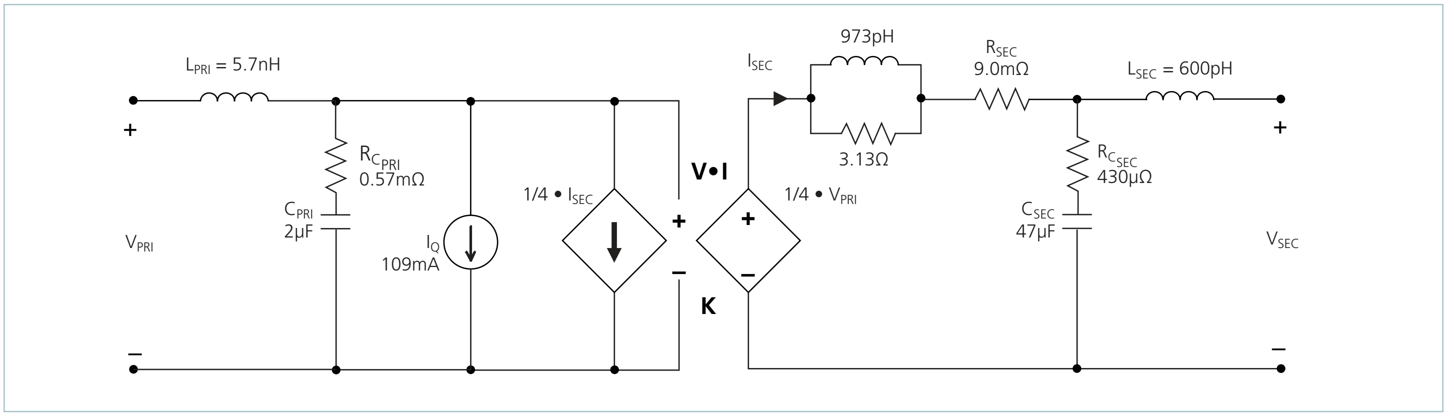


Figure 17 *— VI Chip® module AC model*

At no load:

$$V_{SEC} = V_{PRI} \bullet K \tag{1}$$

K represents the "turns ratio" of the SAC.
Rearranging Equation 1:

$$K = \frac{V_{SEC}}{V_{PRI}} \tag{2}$$

In the presence of load, V_{SEC} is represented by:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R_{SEC} \tag{3}$$

and I_{SEC} is represented by:

$$I_{SEC} = \frac{I_{PRI} - I_Q}{K} \tag{4}$$

R_{SEC} represents the impedance of the SAC, and is a function of the R_{DSON} of the primary and secondary MOSFETs and the winding resistance of the power transformer. I_Q represents the quiescent current of the SAC control and gate drive circuitry. For applications where the source is located on the secndary side, Equations 1 – 4 can be rearranged to represent V_{PRI} and I_{PRI} as a function of V_{SEC} and I_{SEC}.

The use of DC voltage transformation provides additional interesting attributes. Assuming that R_{SEC} = 0Ω and I_Q = 0A, Equation 3 now becomes Equation 1 and is essentially load independent, resistor R is now placed in series with V_{PRI} as shown in Figure 18.

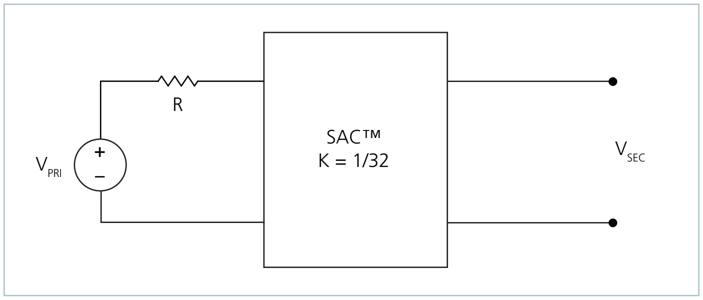


Figure 18 *— K = 1/32 Sine Amplitude Converter™ with series primary resistor*

The relationship between V_{PRI} and V_{SEC} becomes:

$$V_{SEC} = (V_{PRI} - I_{PRI} \bullet R) \bullet K \tag{5}$$

Substituting the simplified version of Equation 4 (I_Q is assumed = 0A) into Equation 5 yields:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R \bullet K^2 \tag{6}$$

This is similar in form to Equation 3, where R_{SEC} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the primary side of the SAC is effectively scaled by K^2 with respect to the secondary.

Assuming that R = 1Ω, the effective R as seen from the secondary side is 0.98mΩ, with K = 1/32 as shown in Figure 18.

A similar exercise should be performed with the additon of a capacitor or shunt impedance at the primary to the SAC. A switch in series with V_{PRI} is added to the circuit. This is depicted in Figure 19.

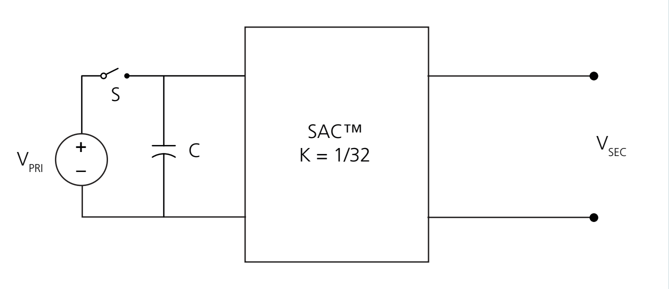


***Figure 19** — Sine Amplitude Converter™ with input capacitor*

A change in V_{PRI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\,\frac{dV_{PRI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{PRI}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{SEC} \bullet K \qquad (8)$$

Substituting Equations 1 and 8 into Equation 7 reveals:

$$I_{SEC} = \frac{C}{K^2} \bullet \frac{dV_{SEC}}{dt} \qquad (9)$$

The equation in terms of the secondary has yielded a K^2 scaling factor for C, specified in the denominator of the equation. A K factor less than unity results in an effectively larger capacitance on the secondary when expressed in terms of the primary. With a K = 1/32 as shown in Figure 19, C = 1µF would appear as C = 1024µF when viewed from the secondary. Note that in situations where the source voltage is located on the secondary side, the effect is reversed and effective valve of capacitance located on the secondary side is divided by a factor of $1/K^2$ when reflected to the primary.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point-of-load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low-loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the VTM module are:

- No load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss (R_{SEC}): refers to the power loss across the VTM modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{R_{SEC}} \qquad (10)$$

Therefore,

$$P_{SEC} = P_{PRI} - P_{DISSIPATED} = P_{PRI} - P_{NL} - P_{R_{SEC}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{SEC}}{P_{PRI}} = \frac{P_{PRI} - P_{NL} - P_{R_{SEC}}}{P_{PRI}} \qquad (12)$$

$$= \frac{V_{PRI} \bullet I_{PRI} - P_{NL} - (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}}$$

$$= 1 - \left(\frac{P_{NL} + (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}}\right)$$

Primary and Secondary Filter Design

A major advantage of a SAC system versus a conventional PWM converter is that the former does not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of primary voltage and secondary current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving high power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- *Guarantee low source impedance:*

  To take full advantage of the VTM module dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5MHz. Primary capacitance may be added to improve transient performance or compensate for high source impedance.

- *Further reduce primary and/or secondary voltage ripple without sacrificing dynamic response:*

  Given the wide bandwidth of the VTM module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the secondary of the VTM module multiplied by its K factor.

- *Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures:*

  The VI Chip® module primary/secondary voltage ranges must not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating primary or secondary range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Capacitive Filtering Considerations for a Sine Amplitude Converter™

It is important to consider the impact of adding capacitance to a Sine Amplitude Converter on the system as a whole. Both the capacitance value and the effective impedance of the capacitor must be considered.

A Sine Amplitude Converter has a DC R_{SEC} value which has already been discussed on Page 13. The AC R_{SEC} of the SAC contains several terms:

- Resonant tank impedance
- Primary lead inductance and internal capacitance
- Secondary lead inductance and internal capacitance

The values of these terms are shown in the behavioral model on Page 13. It is important to note on which side of the transformer these impedances appear and how they reflect across the transformer given the K factor.

The overall AC impedance varies from model to model. For most models it is dominated by DC R_{SEC} value from DC to beyond 500kHz. The behavioral model on Page 13 should be used to approximate the AC impedance of the specific model.

Any capacitors placed at the output of the VTM module reflect back to the primary of the module by the square of the K factor (Equation 9) with the impedance of the module appearing in series. It is very important to keep this in mind when using a PRM™ regulator to power the VTM module. Most PRM modules have a limit on the maximum amount of capacitance that can be applied to the secondary. This capacitance includes both the PRM output capacitance and the VTM module secondary capacitance reflected back to the primary. In PRM module remote-sense applications, it is important to consider the reflected value of VTM module secondary capacitance when designing and compensating the PRM module control loop.

Capacitance placed at the primary of the VTM module appear to the load reflected by the K factor with the impedance of the VTM module in series. In step-down ratios, the effective capacitance is increased by the K factor. The effective ESR of the capacitor is decreased by the square of the K factor, but the impedance of the module appears in series. Still, in most step-down VTM modules an electrolytic capacitor placed at the primary of the module will have a lower effective impedance compared to an electrolytic capacitor placed at the secondary. This is important to consider when placing capacitors at the secondary of the module. Even though the capacitor may be placed at the secondary, the majority of the AC current will be sourced from the lower impedance, which in most cases will be the module. This should be studied carefully in any system design using a module. In most cases, it should be clear that electrolytic secondary capacitors are not necessary to design a stable, well-bypassed system.

Current Sharing

The SAC™ topology bases its performance on efficient transfer of energy through a transformer without the need of closed-loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array with the same K factor, the VTM module will inherently share the load current (typically 5%) with parallel units according to the equivalent impedance divider that the system implements from the power source to the point-of-load.

Some general recommendations to achieve matched array impedances:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide the PCB layout as symmetric as possible.
- Apply same filtering to each unit.

For further details see:
AN:016 Using BCM® Bus Converters in High Power Arrays.

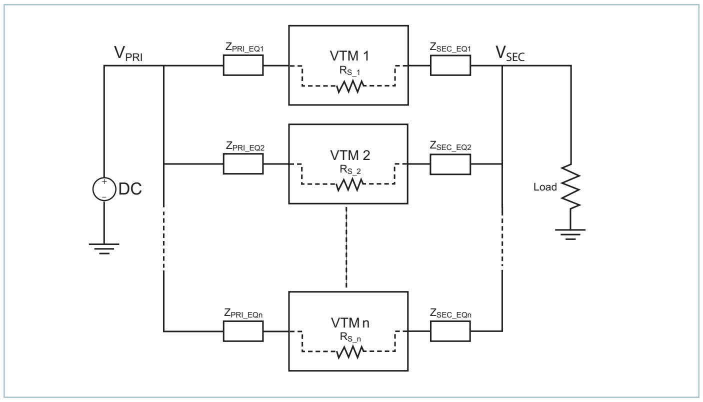


***Figure 20** — VTM module array*

Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® products are not internally fused. Line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

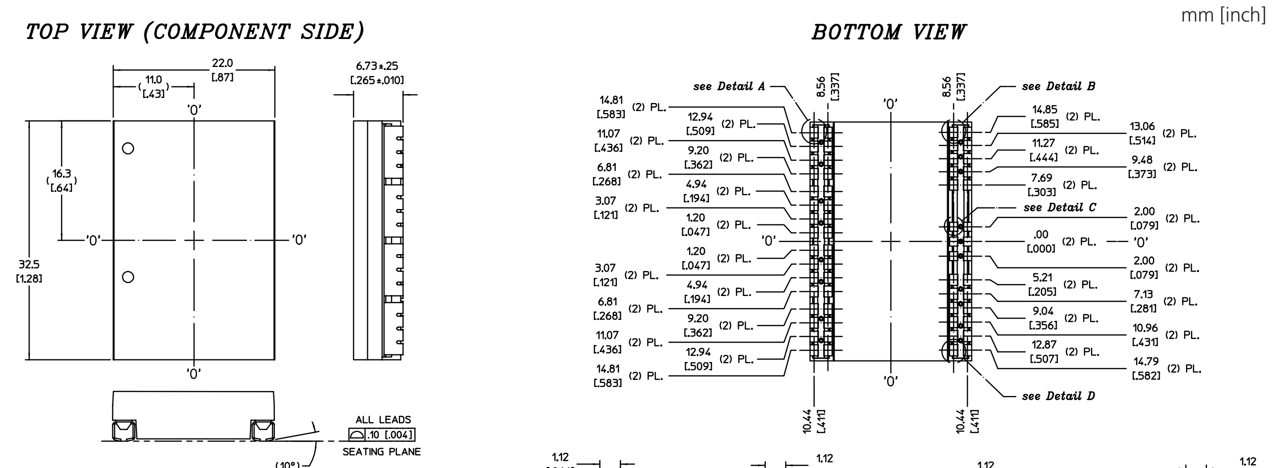
The fuse shall be selected by closely matching system requirements with the following characteristics:

- Direction of power flow: if a power source is located on the primary, there must be a fuse located in the series with the primary source; if a source is located on the secondary, there must also be a fuse located in series with the secondary source.
- Current rating (usually greater than maximum current of VTM module)
- Maximum voltage rating (usually greater than the maximum possible primary voltage)
- Ambient temperature
- Nominal melting I^2t

Bidirectional Operation

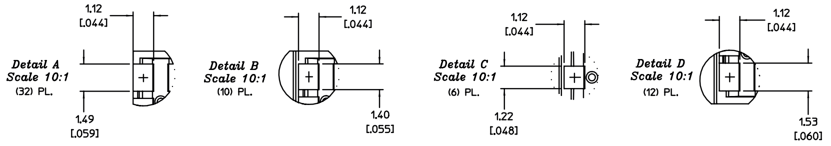
The VTM48EF120T025A0R is capable of bidirectional operation. If a voltage is present at the secondary which satisfies the condition $V_{SEC} > V_{PRI} \bullet K$ at the time the VC voltage is applied, or after the unit has started, then energy will be transferred from secondary to primary. The primary-to-secondary ratio will be maintained. The VTM48EF120T025A0R will continue to operate bidirectional as long as the primary and secondary are within the specified limits.

J-Lead Package Mechanical Drawing



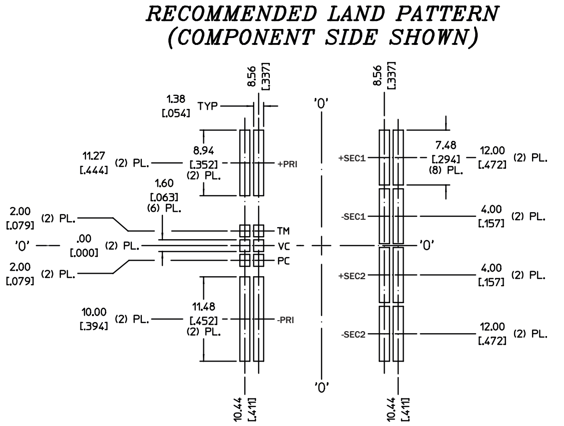
NOTES:

1. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2. DIMENSIONS ARE $\frac{\text{mm}}{\text{inch}}$.
   UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
3. .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
4. PRODUCT MARKING ON TOP SURFACE



DXF and PDF files are available on vicorpower.com

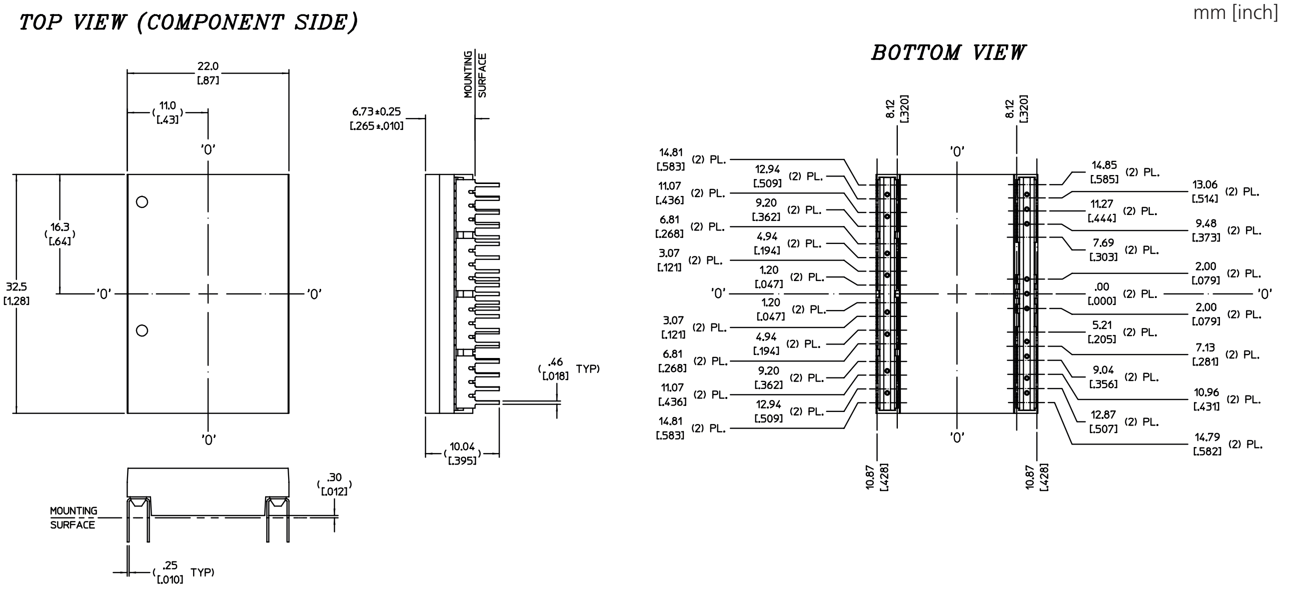
J-Lead Package Recommended Land Pattern



1. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2. DIMENSIONS ARE $\frac{\text{mm}}{\text{inch}}$.
   UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
3. .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
4. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

Through-Hole Package Mechanical Drawing

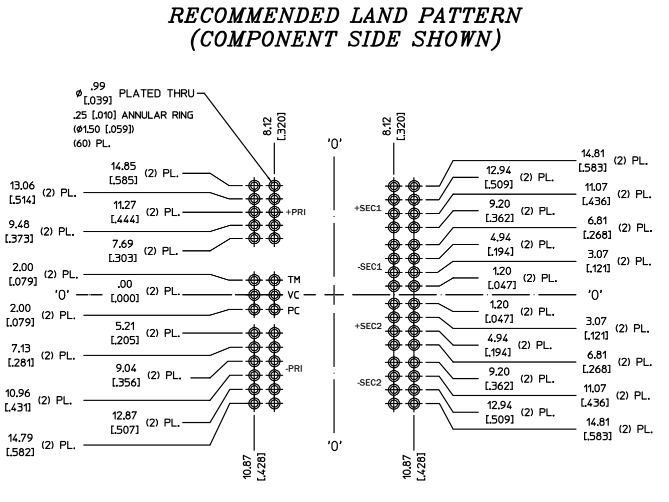


NOTES:

1. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2. DIMENSIONS ARE $\frac{\text{mm}}{\text{inch}}$.
   UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
3. .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
4. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

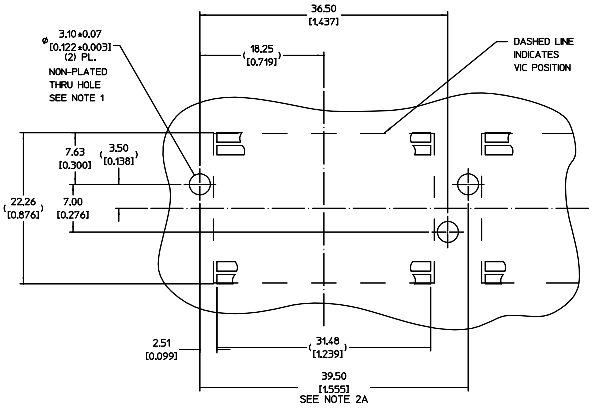
Through-Hole Package Recommended Land Pattern



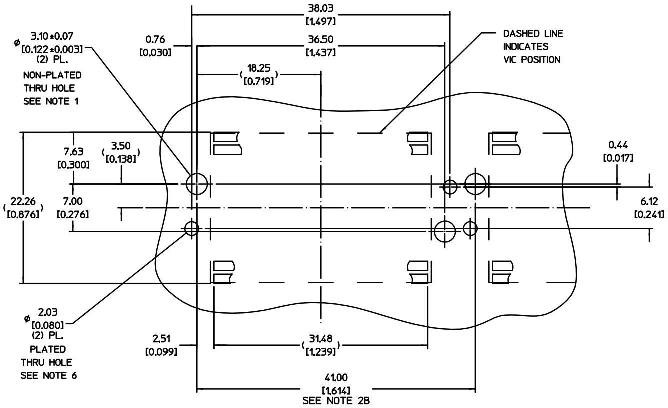
1. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2. DIMENSIONS ARE $\frac{\text{mm}}{\text{inch}}$.
   UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
3. .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
4. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

Recommended Heat Sink Push Pin Location



(NO GROUNDING CLIPS)

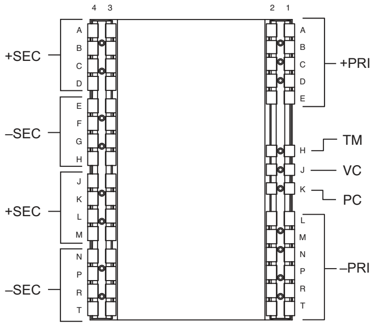


(WITH GROUNDING CLIPS)

Notes:

1. Maintain 3.50 (0.138) Dia. keep-out zone free of copper, all PCB layers.
2. (A) Minimum recommended pitch is 39.50 (1.555). This provides 7.00 (0.275) component edge-to-edge spacing, and 0.50 (0.020) clearance between Vicor heat sinks.
   (B) Minimum recommended pitch is 41.00 (1.614). This provides 8.50 (0.334) component edge-to-edge spacing, and 2.00 (0.079) clearance between Vicor heat sinks.
3. VI Chip® module land pattern shown for reference only; actual land pattern may differ. Dimensions from edges of land pattern to push–pin holes will be the same for all full-size VI Chip® products.
4. RoHS compliant per CST–0001 latest revision.
5. Unless otherwise specified:
   Dimensions are mm (inches)
   tolerances are:
   x.x (x.xx) = ±0.3 (0.01)
   x.xx (x.xxx) = ±0.13 (0.005)
6. Plated through holes for grounding clips (33855) shown for reference, heat sink orientation and device pitch will dictate final grounding solution.

VTM Module Pin Configuration



Bottom View

Signal Name	Pin Number
+PRI	A1 – E1, A2 – E2
–PRI	L1 – T1, L2 – T2
TM	H1, H2
VC	J1, J2
PC	K1, K2
+SEC	A3 – D3, A4 – D4, J3 – M3, J4 – M4
–SEC	E3 – H3, E4 – H4, N3 – T3, N4 – T4

Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

Visit http://www.vicorpower.com/dc-dc-converters-board-mount/vtm for the latest product information.

Vicor's Standard Terms and Conditions and Product Warranty

All sales are subject to Vicor's Standard Terms and Conditions of Sale, and Product Warranty which are available on Vicor's webpage (http://www.vicorpower.com/termsconditionswarranty) or upon request.

Life Support Policy

VICOR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF VICOR CORPORATION. As used herein, life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness. Per Vicor Terms and Conditions of Sale, the user of Vicor products and components in life support applications assumes all risks of such use and indemnifies Vicor against all liability and damages.

Intellectual Property Notice

Vicor and its subsidiaries own Intellectual Property (including issued U.S. and Foreign Patents and pending patent applications) relating to the products described in this data sheet. No license, whether express, implied, or arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Interested parties should contact Vicor's Intellectual Property Department.

The products described on this data sheet are protected by the following U.S. Patents Numbers:
5,945,130; 6,403,009; 6,710,257; 6,911,848; 6,930,893; 6,934,166; 6,940,013; 6,969,909; 7,038,917; 7,145,186; 7,166,898; 7,187,263; 7,202,646; 7,361,844; D496,906; D505,114; D506,438; D509,472; and for use under 6,975,098 and 6,984,965.

Contact Us: http://www.vicorpower.com/contact-us

Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715
www.vicorpower.com

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com