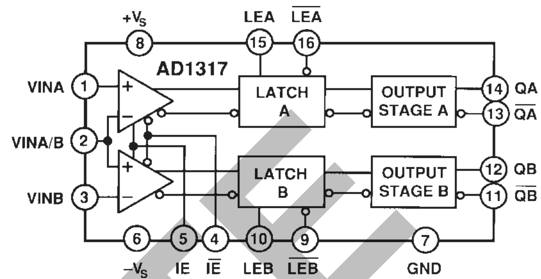
Ultrahigh Speed Window Comparator with Latch

AD1317

FEATURES
Full Window Comparator
2.0 pF max Input Capacitance
9 V max Differential Input Voltage
2.5 ns Propagation Delays
Low Dispersion
Low Input Bias Current
Independent Latch Function
Input Inhibit Mode
80 dB CMRR

APPLICATIONS
High Speed Pin Electronic Receiver
High Speed Triggers
Threshold Detectors
Peak Detectors

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1317 is an ultrahigh speed window comparator with a latch. It uses a high speed monolithic process to provide high dc accuracy without sacrificing input voltage range. The AD1317 guarantees a 2.8 ns maximum propagation delay.

On-chip connection of the common input eliminates the contributions of a second bonding pad and package pin to the input capacitance, resulting in a maximum input capacitance of 2 pF.

The dispersion, or variation in propagation delay with input overdrive levels and slew rates, is typically 350 ps for 5 V signals and 200 ps for 1 V inputs.

The AD1317 employs a high precision differential input stage with a common-mode range of 9 V. Its complementary digital outputs are ECL compatible. The output stage is capable of driving a 50 Ω line terminated to –2 V. The AD1317 also provides a latch function, allowing operation in a sample-hold mode. The latch inputs can also be used to generate hysteresis.

The comparator input can be switched into a high impedance state through the inhibit mode feature, electrically removing the comparator from the circuit. The bias current in inhibit mode is typically 50 pA.

The AD1317 is available in a small 16-lead, hermetically sealed "gull-wing" surface mount package and operates over the commercial temperature range, 0°C to +70°C.

REV. A

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AD1317–SPECIFICATIONS (All specifications at +25°C, free air. Outputs terminated into 50 Ω to –2 V, with + V_S = +10 V, –V_S = 5.2 V unless otherwise noted)

Parameter	Symbol	AD1317KZ			Units	Comments
		Min	Typ	Max		
DC INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	–10		10	mV	CMV = 0 V
Offset Drift	dV_{OS}/dT		20		μV/°C	
VINA/B Bias Currents						–2 V to +7 V
Active	Ibca		10	33	μA	
Inhibit	Ibci		50		pA	
VINA, VINB Bias Currents						–2 V to +7 V
Active	Ibsa		5	16.5	μA	
Inhibit	Ibsi		50		pA	
VINA/B Resistance	Rinc		4		MΩ	
VINA, VINB Resistance	Rins		8		MΩ	
Capacitance VINA/B, VINA, VINB	C_{IN}		1.5	2.0	pF	
Voltage Range	V_{CM}	–2		7	Volts	See Note 5
Differential Voltage	V_{DIFF}			9	Volts	
Common-Mode Rejection Ratio	CMRR	70	80		dB	–2 V to +7 V
LATCH ENABLE INPUTS						
Input Voltage, Any Input		–2.0		5.0	Volts	
Differential Voltage		0.4		4	Volts	
Logic "1" Current	I_{IH}			10	μA	
Logic "0" Current	I_{IL}	–200			μA	
Capacitance				4	pF	
INPUT ENABLE CURRENTS						
Input Voltage, Any Input		–2.0		5.0	Volts	
Differential Voltage		0.4		4	Volts	
Logic "1" Current	I_{IH}			20	μA	
Logic "0" Current	I_{IL}	–200			μA	
Capacitance				4	pF	
DIGITAL OUTPUTS						
Logic "l" Voltage	V_{OH}	–0.98			Volts	
Logic "0" Voltage	V_{OL}			–1.50	Volts	
SWITCHING PERFORMANCE						See Figure 3
Propagation Delays						
Input to Output	t_{PDR}, t_{PDF}		1.8	2.8	ns	See Note 1
Latch Enable to Output	t_{LO}		2.0	2.5	ns	See Note 1
Active to Inhibit	t_{IN}		2.5		ns	See Note 2
Inhibit to Active	t_{IE}		15		ns	See Note 3
Propagation Delay T.C.			5		ps/°C	
Dispersion						See Note 4
5 V Signal						See Figure 1
All Edges			450	600	ps	
Rising Edge			350		ps	
Falling Edge			350		ps	
1 V Signal						See Figure 2
All Edges			250	400	ps	
Rising Edge			200		ps	
Falling Edge			200		ps	
LATCH TIMING						
Input Pulse Width	t_{PW}	2.5	1.0		ns	
Setup Time	t_S	1.5	0.4		ns	
Hold Time	t_H	0			ns	
POWER SUPPLIES						
$-V_S$ to $+V_S$ Range			15.2	15.6		See Note 5
Positive Supply	$+V_S$	8.0	10.0	11.0	Volts	
Negative Supply	$-V_S$	–7.2	–5.2	–4.2	Volts	
Positive Supply Current	I+		50	70	mA	
Negative Supply Current	I–	–100	–70		mA	
PSRR		65	75		dB	Measured at ±2.5% of $+V_S$ and $-V_S$

NOTES

[1]Propagation Delay is measured from the input threshold crossing at the 50% point of a 0 V to 5 V input to the output Q and $\overline{Q}$ crossing.

[2]Propagation Delay is measured from the input crossing of IE and $\overline{IE}$ to when the input bias currents drop to 10% of their nominal value.

[3]Propagation Delay is measured from the input crossing of IE and $\overline{IE}$ to when the input bias currents rise to 90% of their nominal value.

[4]Dispersion is measured with input slew rates of 0.5 V/ns and 2.5 V/ns for 5 V swings, 0.5 V/ns and 1 V/ns for 1 V swings.

[5]The comparator input voltage range is specified for –2 V to +7 V for typical power supply values of -5.2 V and +10.0 V but can be offset for different input ranges such as –1 V to +8 V with power supplies of –4.2 V and +11 V, as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $+V_S$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage
- $+V_S$ to GND . . . . +12 V
- $-V_S$ to GND . . . . –9 V
- Difference from $+V_S$ to $-V_S$ . . . . +16 V

Inputs
- VINA/B, VINA, VINB . . . . $+V_S$ – 13.5 V, $-V_S$ + 13.7 V
- LEA, LEA, LEB, LEB . . . . $+V_S$ – 14 V, $-V_S$ + 12 V
- IE, $\overline{IE}$ . . . . $+V_S$ – 14 V, $-V_S$ + 10.3 V

Outputs[2]
- QA, $\overline{QA}$, QB, $\overline{QB}$ . . . . GND – 0.5 V, GND + 3.5 V

Operating Temperature Range . . . . 0°C to +70°C

Storage Temperature Range
- After Soldering . . . . –65°C to + 125°C

Lead Temperature Range (Soldering 20 sec)[3] . . . . +300°C

NOTES

[1]Stresses above those limits under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Limits apply for shorted output.

[3]To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in an environment at 24°C ±5°C (75°F ±10°F) with relative humidity not to exceed 65%.

WINDOW COMPARATOR PIN ASSIGNMENT

Pin No.	Description	
1	VINA	Noninverting Comparator A Input
2	VINA/B	Window Comparator Common Input
3	VINB	Inverting Comparator B Input
4	$\overline{IE}$	$\overline{\text{Input Enable}}$
5	IE	Input Enable
6	$-V_S$	Negative Supply, –5.2V
7	GND	Ground
8	$+V_S$	Positive Supply, +10 V
9	$\overline{LEB}$	$\overline{\text{Latch Enable B}}$
10	LEB	Latch Enable B
11	$\overline{QB}$	$\overline{\text{Comparator B Output}}$
12	QB	Comparator B Output
13	$\overline{QA}$	$\overline{\text{Comparator A Output}}$
14	QA	Comparator A Output
15	LEA	Latch Enable A
16	$\overline{LEA}$	$\overline{\text{Latch Enable A}}$

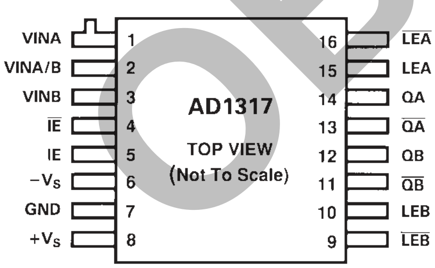
ORDERING GUIDE

Model	Temperature Range	Description	Package Option*	Quantity
AD1317KZ	0°C to +70°C	16-Lead Gull Wing	Z-16A	1-24 25–99 100+

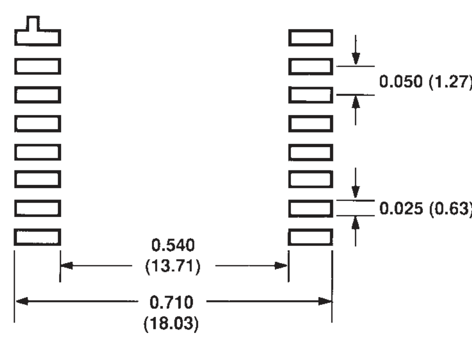
*Z = Ceramic Leaded Chip Carrier.

CONNECTION DIAGRAMS

Dimensions shown in inches and (mm).



SUGGESTED LANDING PADS LOCATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1317 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

DEFINITION OF TERMS

Vos INPUT OFFSET VOLTAGE—The voltage that must be applied between either VINA and VINA/B or VINB and VINA/B to obtain zero voltage between outputs QA and $\overline{QA}$, or QB and $\overline{QB}$, respectively.

dV_{OS}/dT OFFSET DRIFT—The ratio of the change in input offset voltages, over the operating temperature range, to the change in temperature.

Ibca INPUT BIAS CURRENT (VINA/B, ACTIVE)—The bias current of the window comparator's common input with inputs enabled.

Ibci INPUT BIAS CURRENT (VINA/B, INHIBIT)—The bias current of the window comparator's common input with inputs inhibited.

Ibsa INPUT BIAS CURRENT (VINA or VINB, ACTIVE)—The bias current of either single input with inputs active.

Ibsi INPUT BIAS CURRENT (VINA or VINB, INHIBIT)—The bias current of either single input with inputs inhibited.

Rinc INPUT RESISTANCE (VINA/B)—The input resistance looking into the window comparator's common input.

Rins INPUT RESISTANCE (VINA or VINB)—The input resistance looking into either single input.

C_{IN} INPUT CAPACITANCE (VINA/B)—The capacitance looking into the window comparator's common input.

V_{CM} INPUT COMMON-MODE VOLTAGE RANGE—The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

V_{DIFF} INPUT DIFFERENTIAL VOLTAGE RANGE—The maximum difference between any input terminal voltages.

CMRR COMMON-MODE REJECTION RATIO—The ratio of common-mode input voltage range to the peak-to-peak change in input offset voltage over this range.

I_{IH} LOGIC "1" INPUT CURRENT—The logic high current flowing into (+) or out of (–) a logic input.

I_{IL} LOGIC "0" INPUT CURRENT—The logic low current flowing into (+) or out of (–) a logic input.

V_{OH} LOGIC "1" OUTPUT VOLTAGE—The logic high output voltage with a specified load.

V_{OL} LOGIC "0" OUTPUT VOLTAGE—The logic low output voltage with a specified load.

I_{OH} LOGIC "1" OUTPUT CURRENT—The logic high output source current.

I_{OL} LOGIC "0" OUTPUT CURRENT—The logic low output source current.

I+ POSITIVE SUPPLY CURRENT—The current required from the $+V_S$ supply.

I– NEGATIVE SUPPLY CURRENT—The current required from the $–V_S$ supply.

PSRR POWER SUPPLY REJECTION RATIO—The ratio of power supply voltage change to the peak-to-peak change in input offset voltage.

AD1317 SWITCHING TERMS (See Figure 3)

t_{PDR} INPUT TO OUTPUT RISING EDGE DELAY—The propagation delay measured from the time VINA/B crosses either VINA or VINB, in a low to high transition, to the time QA and $\overline{QA}$ or QB and $\overline{QB}$ cross, respectively.

t_{PDF} INPUT TO OUTPUT FALLING EDGE DELAY—The propagation delay measured from the time VINA/B crosses either VINA or VINB, in a high to low transition, to the time QA and $\overline{QA}$ or QB and $\overline{QB}$ cross, respectively.

t_S MINIMUM LATCH SET-UP TIME—The minium time before LE goes high with respect to $\overline{LE}$ that an input signal change must be present in order to be acquired and held at the outputs.

t_H MINIMUM LATCH HOLD TIME—The minium time after LE goes high with respect to $\overline{LE}$ that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{PW} MINIMUM LATCH ENABLE PULSE WIDTH—The minimum time that LE must be held high with respect to $\overline{LE}$ in order to acquire and hold an input change.

t_{LO} LATCH ENABLE TO OUTPUT DELAY—The time between when LE goes high with respect to $\overline{LE}$ that QA and $\overline{QA}$ or QB and $\overline{QB}$ cross.

t_{ID} INPUT STAGE DISABLE TIME—The time between when $\overline{IE}$ goes high with respect to IE that the input bias currents drop to 10% of their nominal value.

t_{IE} INPUT STAGE ENABLE TIME—The time between when IE goes high with respect to $\overline{IE}$ that the input bias currents rise to 90% of their nominal values.

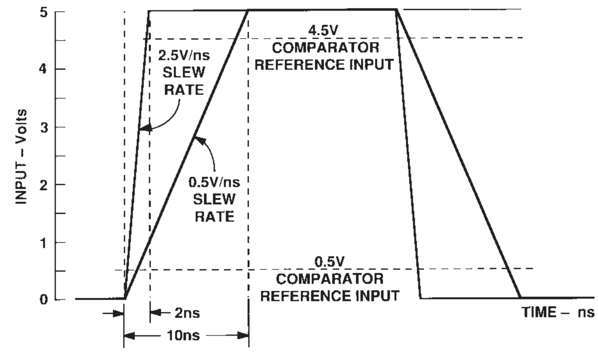


Figure 1. Dispersion Test Input Conditions—5 V Signal

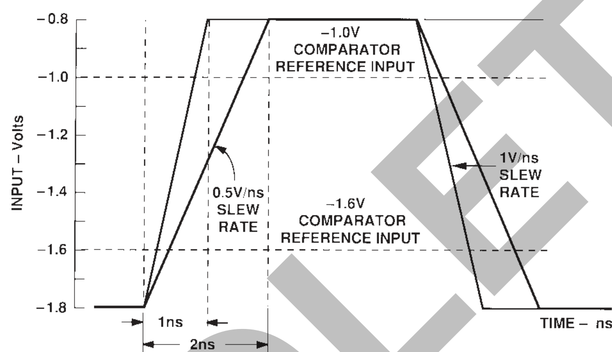


Figure 2. Dispersion Test Input Conditions—1 V Signal

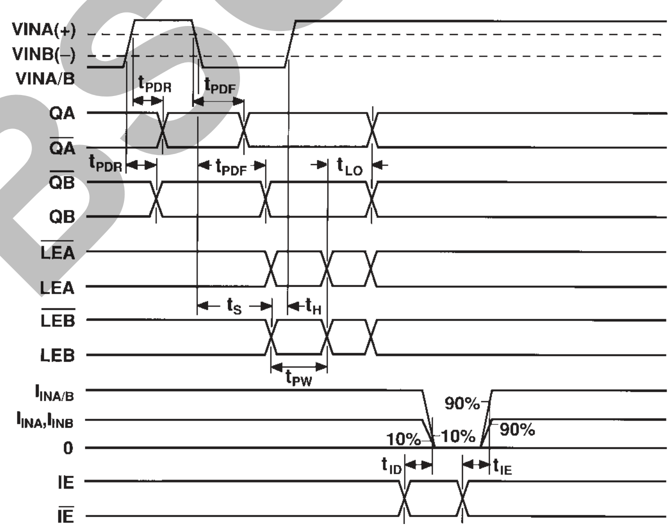


Figure 3. Timing Diagram

AD1317—Typical Performance Characteristics

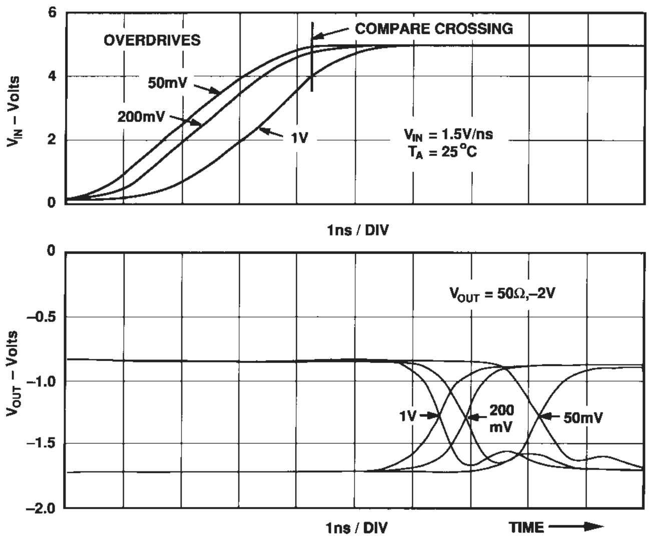


Figure 4. Response to Overdrive Variation—Rising Edge

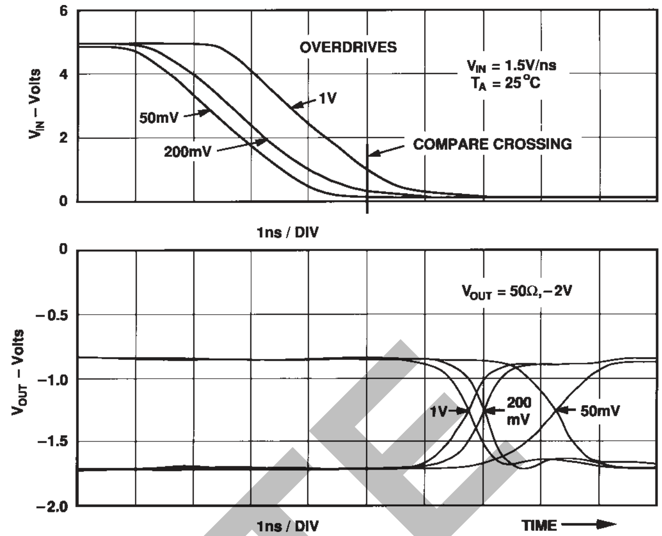


Figure 7. Response to Overdrive Variation—Falling Edge

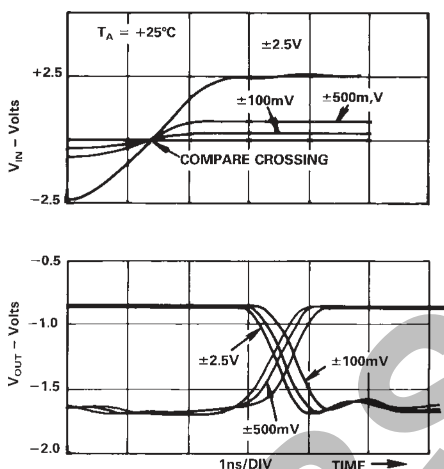


Figure 5. Response to Various Signal Levels—Rising Edge

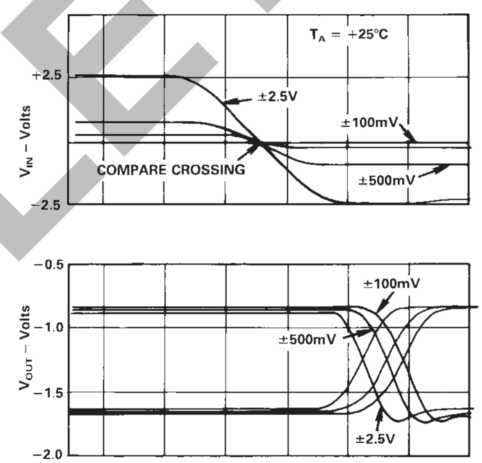


Figure 8. Response to Various Signal Levels—Falling Edge

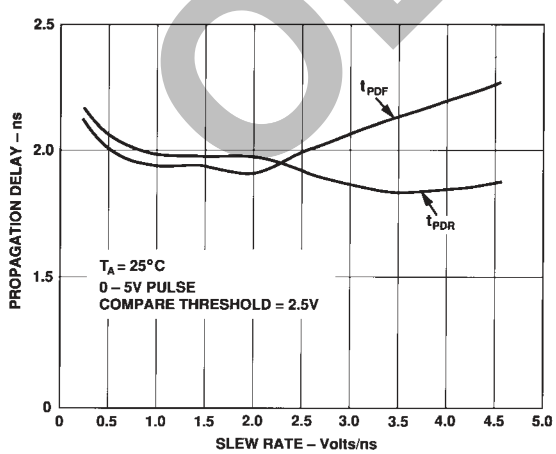


Figure 6. Propagation Delay vs. Slew Rate

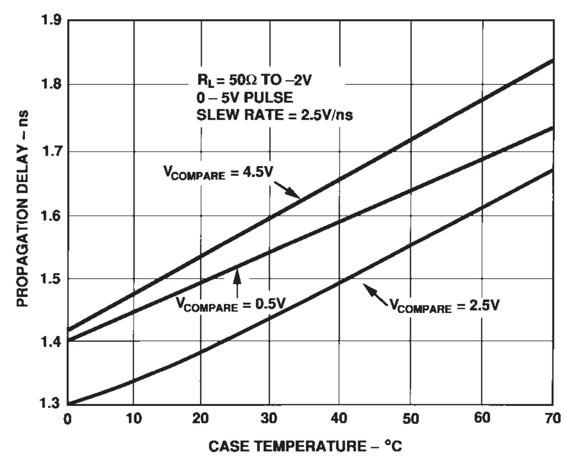


Figure 9. Propagation Delay vs. Temperature—Rising Edge

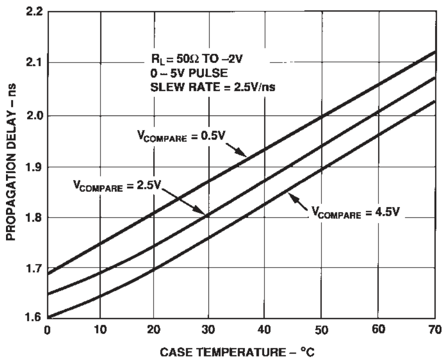


Figure 10. Propagation Delay vs. Temperature—Falling Edge

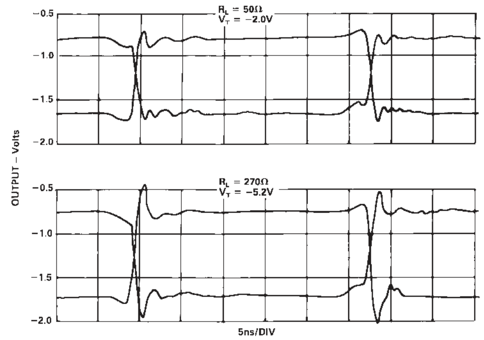


Figure 11. Output Waveform vs. Load

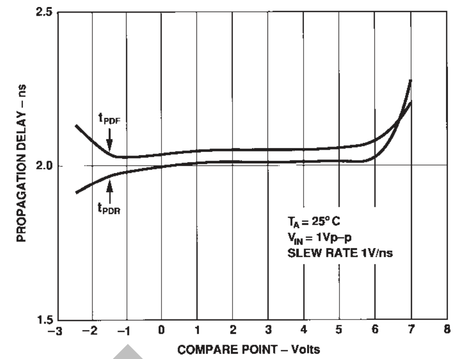


Figure 12. Propagation Delay vs. Common-Mode Voltage

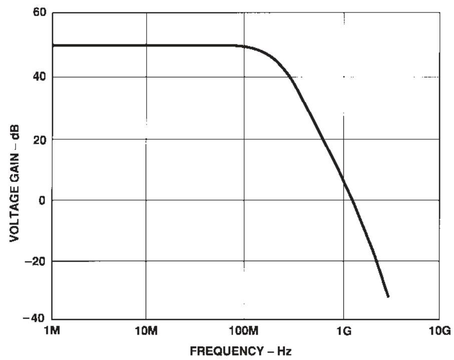


Figure 13. Voltage Gain vs. Frequency

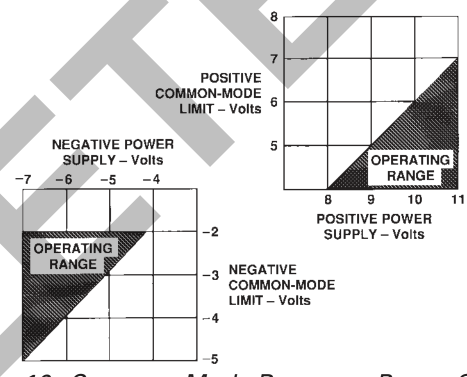


Figure 16. Common-Mode Range vs. Power Supply

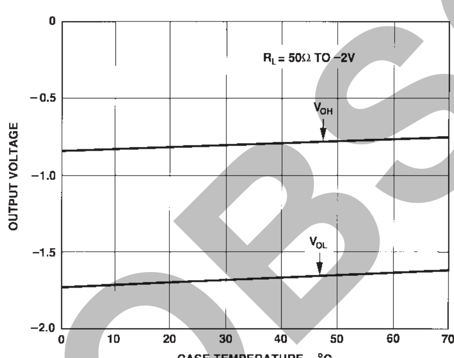


Figure 14. Output Levels vs. Temperature

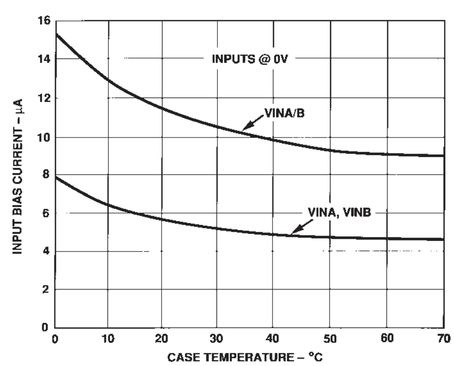


Figure 17. Input Bias Current vs. Temperature

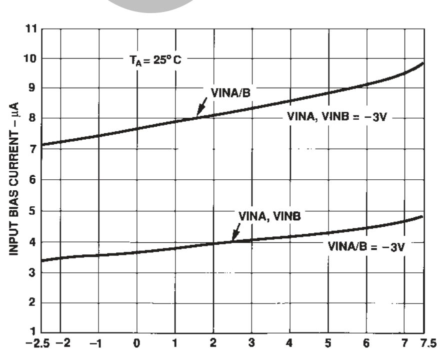


Figure 15. Input Bias Current vs. Input Voltage

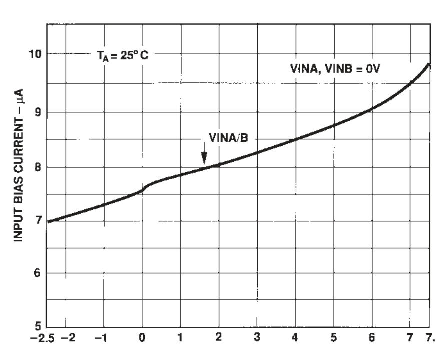


Figure 18. Input Bias Current vs. Input Voltage

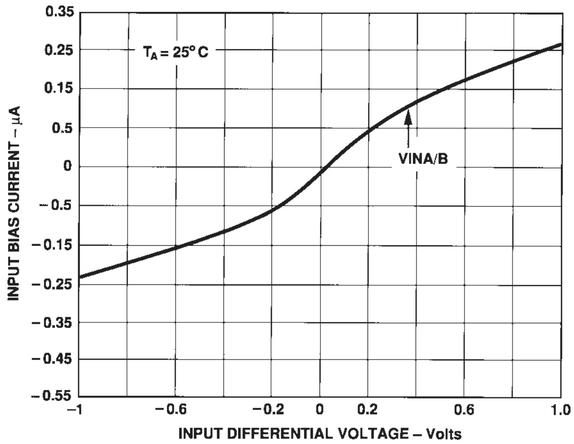


Figure 19. Change in Bias Current vs. Input Differential Voltage (VINA/B – VINA, VINB)

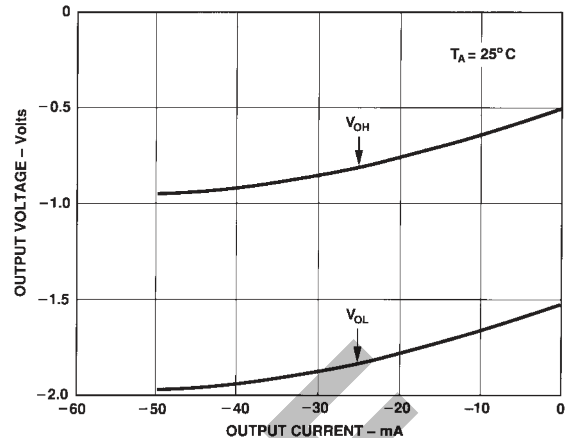


Figure 22. Output Voltage vs. Source Current

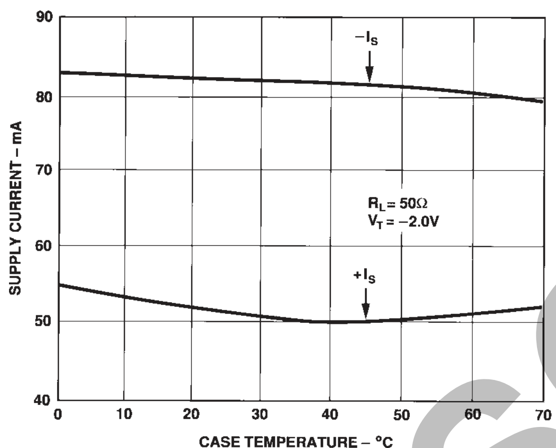


Figure 20. Power Supply Currents vs. Temperature

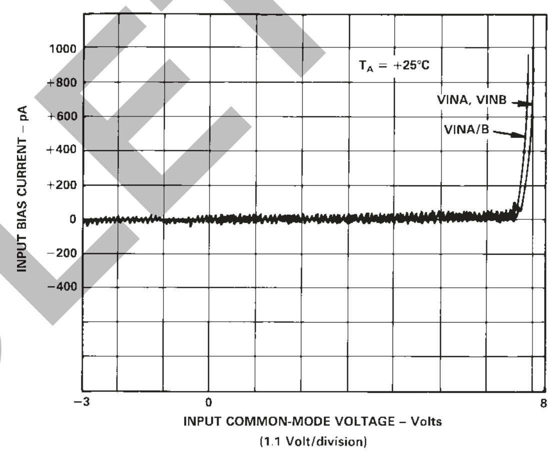


Figure 23. Inhibit Input Bias Current vs. Common-Mode Voltage

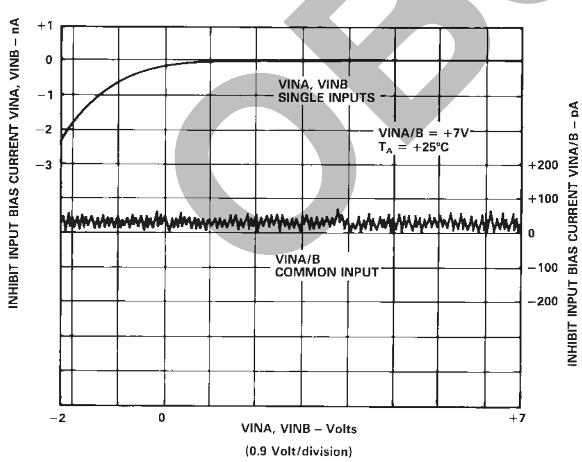


Figure 21. Inhibit Input Bias Current vs. Input Voltage (VINA/B = 7 V)

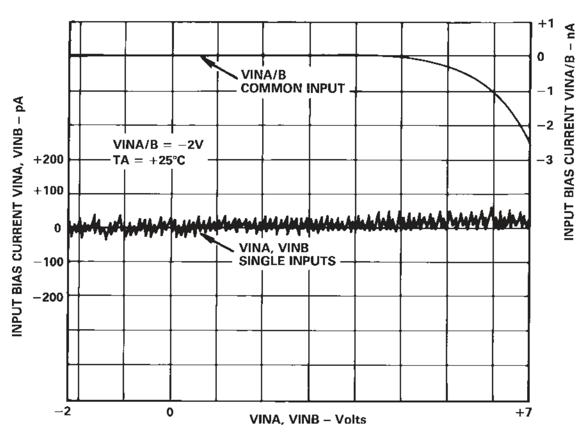


Figure 24. Inhibit Input Bias Current vs. Input Voltage (VINA/B = –2 V)

FUNCTIONAL DESCRIPTION

The AD1317 is an ultrahigh speed window comparator designed for use in general purpose instrumentation and automatic test equipment. The internal connections for windowing operation keep the capacitance at the critical common input (VINA/B) well below what could normally be obtained using separate input pins.

Another key feature is that the front end circuitry may be disabled, decreasing input bias currents to 50 pA (typical). This enables sensitive dc current testing without having to physically disconnect the AD1317's input from the circuit. The comparator's outputs would normally be latched to maintain absolute logic levels prior to inhibiting the input.

High speed comparators using bipolar process technology usually have input bias currents in the 1 µA to 20 µA range, and the AD1317 is no exception in this regard. This occurs because the input devices usually have low current gain but must be operated at high currents to obtain the widest possible bandwidth. Careful design minimizes variations in the AD1317's bias current with respect to both differential and common-mode input variations. This translates directly to a high equivalent input resistance, the minimum of which occurs with zero differential input. The typical input resistance of the AD1317's common input under this condition is on the order of 4 megohms.

Many ATE applications have required input dividers/buffers to reduce standard logic voltages to levels which can be processed by "687" type comparators. These dividers have also reduced the slew rates at which the comparators must properly function. The AD1317's 9 volt differential and common-mode input ranges and 2.5 V/ns slew rate capability make these buffer circuits unnecessary in most applications.

Separate, complementary latch inputs are provided for each comparator. These may be driven by differential or single-ended sources ranging from ECL to HCMOS logic. When using the comparator's transparent mode, the latch inputs may be tied anywhere within their common-mode range with a maximum differential of 4 V. Symmetrical hysteresis may also be generated by applying a small differential voltage to the latch inputs (see HYSTERESIS).

The AD1317's outputs are standard emitter followers with ECL-compatible voltage swings. The recommended output termination is 50 Ω to –2 V. Larger value termination resistors connected to $-V_S$ may be used, but will reduce edge fidelity. Typical output rise and fall times (20%–80%) are 1 ns with a 50 Ω, 10 pF load. The maximum output source current is 40 mA.

THERMAL CONSIDERATIONS

The AD1317 is provided in a 0.450" × 0.450", 16-lead (bottom brazed) gull wing, surface mount package with a typical θ_{JC} (junction-to-case thermal resistance) of 17.5°C/W. Thermal resistance θ_{CA} (case to ambient) vs. air flow for the AD1317 in this package is shown in Figure 25. The improvement in thermal resistance vs. air flow begins to flatten out just above 400 lfm[1, 2].

NOTES
[1]lfm is airflow in linear feet/minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

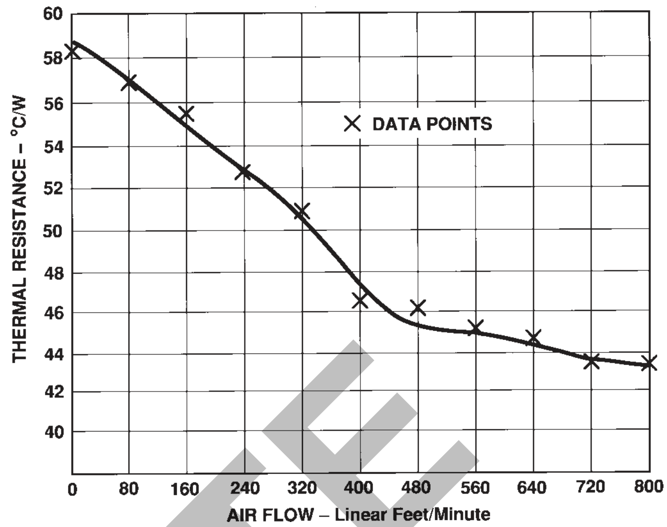


Figure 25. Case-to-Ambient Thermal Resistance vs. Air Flow

DISPERSION

Propagation delay dispersion is the change in device propagation delay which results from changes in the input signal conditions. Dispersion is an indicator of how well the comparator's frontend design balances the conflicting requirements of high gain and wide bandwidth. High gain is needed to ensure that small overdrives will produce valid logic outputs without an increase in propagation delay, while wide bandwidth enables the comparator to handle fast input slew rates. The input signal criteria used to determine the AD1317's dispersion performance are amplitude, overdrive and slew rate for both standard CMOS and ECL signal levels.

HYSTERESIS

The customary technique for introducing hysteresis into a comparator uses positive feedback as shown in Figure 27. The major problems with this approach are that the amount of hysteresis varies with the output logic levels and that the hysteresis is not symmetrical around zero.

The AD1317 does not use this technique. Instead, hysteresis is generated by introducing a differential voltage between LE and $\overline{LE}$ as shown in Figure 28. Hysteresis generated in this manner is independent of output swing and is symmetrical around zero. The variation of hysteresis with input voltage is shown in Figure 29; the useful hysteresis range is about 20 mV.

LAYOUT CONSIDERATIONS

Like any high speed device, the AD1317 requires careful layout and bypassing to obtain optimum performance. Oscillations are generally caused by coupling from an output to the high impedance inputs. All drive impedances should be as low as possible, and lead lengths should be minimized. A ground plane should be used to provide low impedance return paths. Care should be taken in selecting sockets for incoming or other testing to minimize lead inductance, and sockets are not recommended for production use.

Output wire lengths should be kept below one inch. Longer connections require the use of transmission line techniques to prevent ringing and reflections. Lines should be terminated with their characteristic impedance to –2 V. Thevenin-equivalent termination to $-V_S$ is also possible.

High quality RF capacitors should be used for power supply bypassing. These should be located as closely as possible to the AD1317's power pins and connections to the ground plane should have the minimum possible length. Both $+V_S$ and $-V_S$ must be bypassed with 470 pF capacitors located within 0.25 inches of the device's supply pins. In addition, each supply should be bypassed with 0.1 μF ceramic and 10 μF tantalum capacitors. Low impedance power distribution techniques will make the locations of these components less critical. Adding 470 pF capacitors at the VINA and VINB inputs, as close as possible to the package, will improve circuit performance and noise immunity in dc-compare applications.

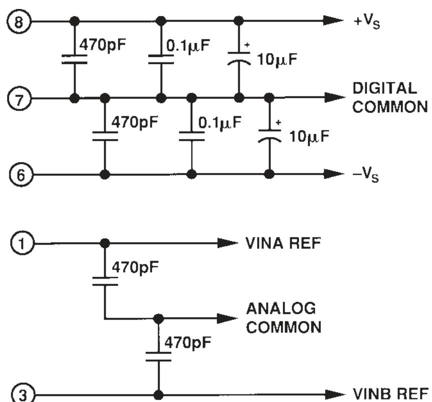


Figure 26. Basic Circuit Decoupling

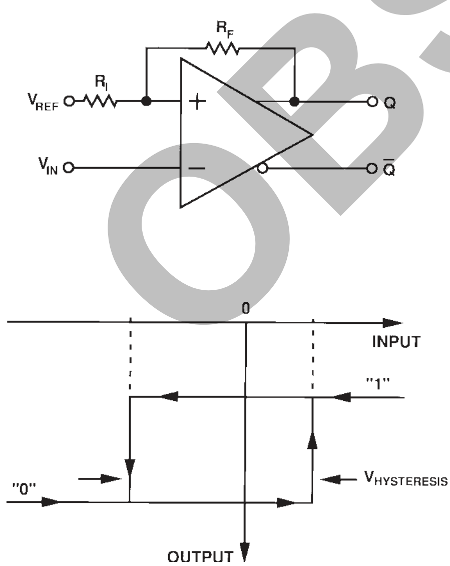


Figure 27. Typical Comparator Hysteresis

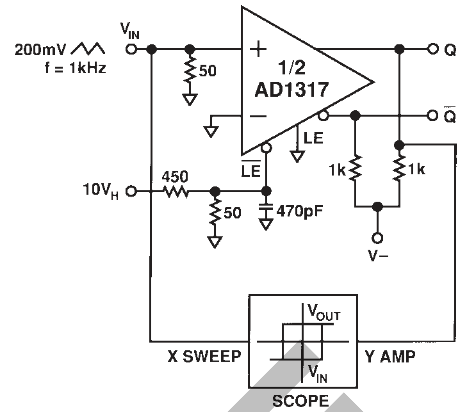


Figure 28. Comparator Hysteresis Test Setup

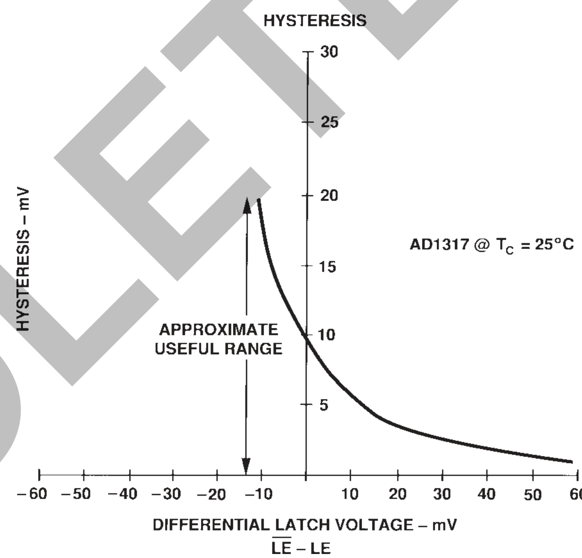


Figure 29. Typical Hysteresis Curve

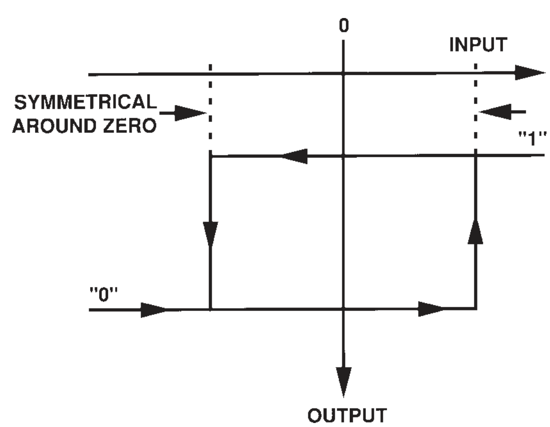


Figure 30. Hysteresis

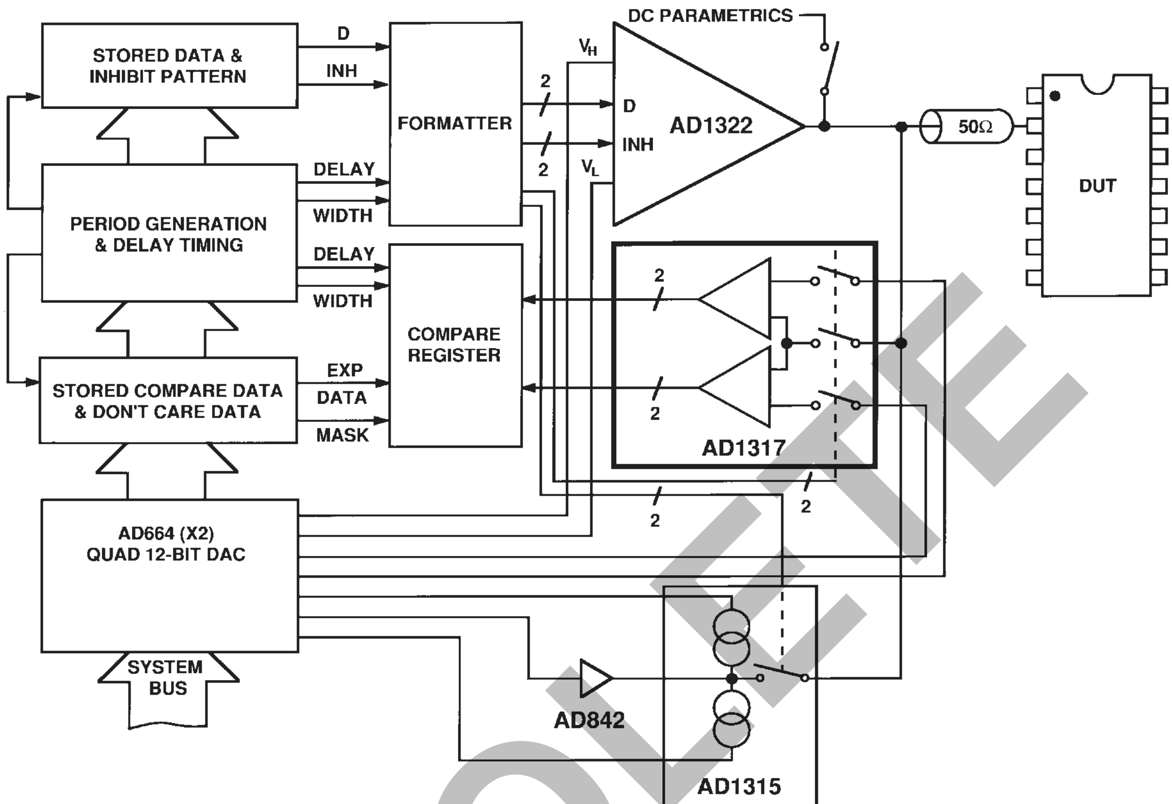
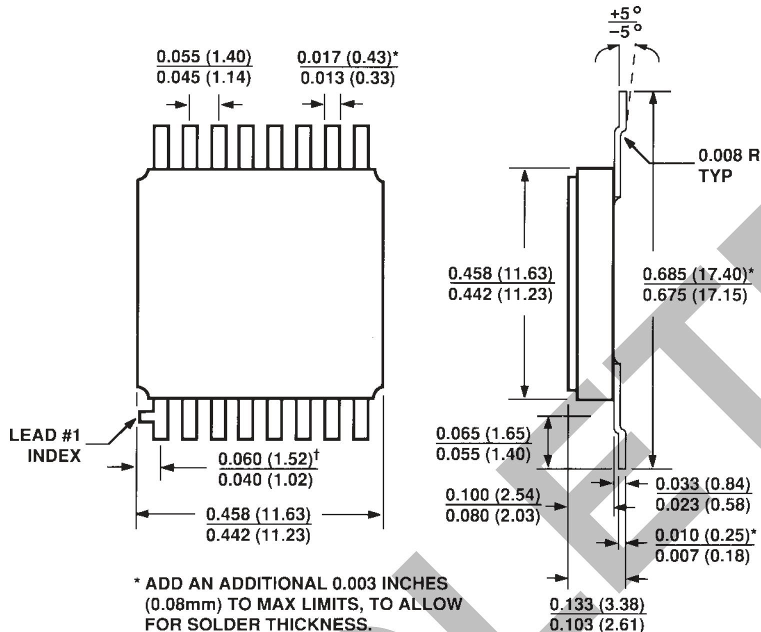


Figure 31. High Speed Digital Test System Block Diagram

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Ceramic Leaded Chip Carrier (Z-16A)



* ADD AN ADDITIONAL 0.003 INCHES (0.08mm) TO MAX LIMITS, TO ALLOW FOR SOLDER THICKNESS.

† APPLIES TO ALL FOUR CORNERS

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