

# CLC5602

## Dual, High Output, Video Amplifier

### General Description

The National CLC5602 has a new output stage that delivers high output drive current (130mA), but consumes minimal quiescent supply current (1.5mA/ch) from a single 5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3dB frequency.

The CLC5602 offers 0.1dB gain flatness to 22MHz and differential gain and phase errors of 0.06% and 0.02°. These features are ideal for professional and consumer video applications.

The CLC5602 offers superior dynamic performance with a 135MHz small-signal bandwidth, 300V/μs slew rate and 5.7ns rise/fall times ( $2V_{step}$ ). The combination of low quiescent power, high output current drive, and high-speed performance make the CLC5602 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC5602 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC5602 will drive a 100Ω load with only -86/-85dBc second/third harmonic distortion ( $A_V = +2$ ,  $V_{out} = 2V_{pp}$ ,  $f = 1\text{MHz}$ ). With a 25Ω load, and the same conditions, it produces only -86/-72dBc second/third harmonic distortion.

The CLC5602 can also be used for driving differential-input step-up transformers for applications such as Asynchronous Digital Subscriber Lines (ADSL) or High-Bit-Rate Digital Subscriber Lines (HDSL).

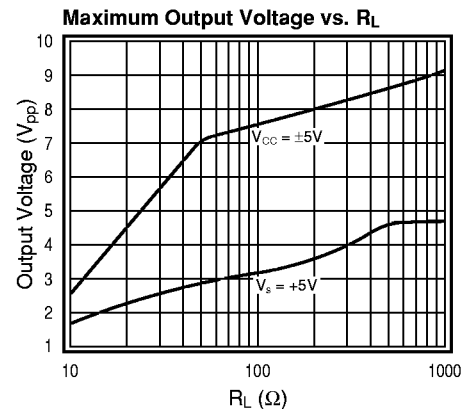
When driving the input of high-resolution A/D converters, the CLC5602 provides excellent -87/-95dBc second/third harmonic distortion ( $A_V = +2$ ,  $V_{out} = 2V_{pp}$ ,  $f = 1\text{MHz}$ ,  $R_L = 1\text{k}\Omega$ ) and fast settling time.

### Features

- 130mA output current
- 0.06%, 0.02° differential gain, phase
- 1.5mA/ch supply current
- 135MHz bandwidth ( $A_V = +2$ )
- -87/-95dBc HD2/HD3 (1MHz)
- 15ns settling to 0.05%
- 300V/μs slew rate
- Stable for capacitive loads up to 1000pf
- Single 5V or ±5V supplies

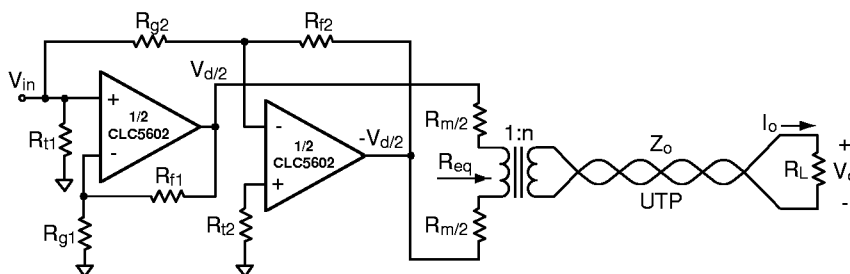
### Applications

- Video line driver
- ADSL/HDSL driver
- Coaxial cable driver
- UTP differential line driver
- Transformer/coil driver
- High capacitive load driver
- Portable/battery-powered applications
- Differential A/D driver



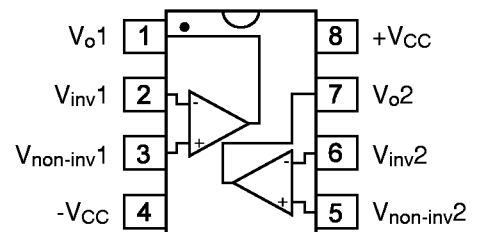
### Typical Application

#### Differential Line Driver with Load Impedance Conversion



### Pinout

#### DIP & SOIC



## +5V Electrical Characteristics (A<sub>v</sub> = +2, R<sub>f</sub> = 750Ω, R<sub>L</sub> = 100Ω, V<sub>s</sub> = +5V<sup>1</sup>, V<sub>cm</sub> = V<sub>EE</sub> + (V<sub>s</sub>/2), R<sub>L</sub> tied to V<sub>cm</sub>, unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
			+25°C	0 to 70°C	-40 to 85°C		
Ambient Temperature	CLC5602IN/IM	+25°C	+25°C	0 to 70°C	-40 to 85°C		
<b>FREQUENCY DOMAIN RESPONSE</b>							
-3dB bandwidth	V <sub>o</sub> = 0.5V <sub>pp</sub>	100	85	75	70	MHz	
	V <sub>o</sub> = 2.0V <sub>pp</sub>	65	60	55	50	MHz	
-0.1dB bandwidth	V <sub>o</sub> = 0.5V <sub>pp</sub>	22	20	17	15	MHz	
gain peaking	<200MHz, V <sub>o</sub> = 0.5V <sub>pp</sub>	0	0.5	0.9	1.0	dB	
gain rolloff	<30MHz, V <sub>o</sub> = 0.5V <sub>pp</sub>	0.1	0.3	0.4	0.5	dB	
linear phase deviation	<30MHz, V <sub>o</sub> = 0.5V <sub>pp</sub>	0.3	0.5	0.6	0.6	deg	
differential gain	NTSC, R <sub>L</sub> = 150Ω to -1V	0.04	–	–	–	%	
differential phase	NTSC, R <sub>L</sub> = 150Ω to -1V	0.09	–	–	–	deg	
<b>TIME DOMAIN RESPONSE</b>							
rise and fall time	2V step	6.1	8.5	9.2	10.0	ns	
settling time to 0.05%	1V step	25	35	50	80	ns	
overshoot	2V step	10	20	22	22	%	
slew rate	2V step	220	190	165	150	V/μs	
<b>DISTORTION AND NOISE RESPONSE</b>							
2 <sup>nd</sup> harmonic distortion	2V <sub>pp</sub> , 1MHz	-77	-74	-71	-71	dBc	
	2V <sub>pp</sub> , 1MHz; R <sub>L</sub> = 1kΩ	-80	-77	-75	-70	dBc	
	2V <sub>pp</sub> , 5MHz	-63	-59	-57	-57	dBc	
3 <sup>rd</sup> harmonic distortion	2V <sub>pp</sub> , 1MHz	-85	-81	-78	-78	dBc	
	2V <sub>pp</sub> , 1MHz; R <sub>L</sub> = 1kΩ	-82	-79	-76	-76	dBc	
	2V <sub>pp</sub> , 5MHz	-62	-57	-54	-54	dBc	
equivalent input noise							
voltage (e <sub>ni</sub> )	>1MHz	3.4	4.4	4.9	4.9	nV/√Hz	
non-inverting current (i <sub>bn</sub> )	>1MHz	6.3	8.2	9.0	9.0	pA/√Hz	
inverting current (i <sub>bi</sub> )	>1MHz	8.7	11.3	12.4	12.4	pA/√Hz	
crosstalk (input referred)	10MHz, 1V <sub>pp</sub>	-72	–	–	–	dB	
<b>STATIC DC PERFORMANCE</b>							
input offset voltage		1	4	5	6	mV	A
average drift		7	–	15	15	μV/°C	
input bias current (non-inverting)		5	12	15	16	μA	A
average drift		25	–	60	60	nA/°C	
input bias current (inverting)		3	10	12	13	μA	A
average drift		10	–	20	20	nA/°C	
power supply rejection ratio	DC	48	45	43	43	dB	
common-mode rejection ratio	DC	49	47	45	45	dB	
supply current per channel	R <sub>L</sub> = ∞	1.5	1.7	1.8	1.8	mA	A
<b>MISCELLANEOUS PERFORMANCE</b>							
input resistance (non-inverting)		0.46	0.36	0.32	0.32	MΩ	
input capacitance (non-inverting)		1.8	2.75	2.75	2.75	pF	
input voltage range, High		4.2	4.1	4.1	4.0	V	
input voltage range, Low		0.8	0.9	0.9	1.0	V	
output voltage range, High	R <sub>L</sub> = 100Ω	4.0	3.9	3.9	3.8	V	
output voltage range, Low	R <sub>L</sub> = 100Ω	1.0	1.1	1.1	1.2	V	
output voltage range, High	R <sub>L</sub> = ∞	4.1	4.0	4.0	3.9	V	
output voltage range, Low	R <sub>L</sub> = ∞	0.9	1.0	1.0	1.1	V	
output current		100	80	65	40	mA	B
output resistance, closed loop	DC	55	90	90	120	mΩ	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

### Notes

- A) J-level: spec is 100% tested at +25°C.  
 B) The short circuit current can exceed the maximum safe output current.  
 1) V<sub>s</sub> = V<sub>CC</sub> - V<sub>EE</sub>

### Absolute Maximum Ratings

supply voltage (V <sub>CC</sub> - V <sub>EE</sub> )	+14V
output current (see note C)	140mA
common-mode input voltage	V <sub>EE</sub> to V <sub>CC</sub>
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD rating (human body model)	1000V

### Reliability Information

Transistor Count	98
MTBF (based on limited test data)	290Mhr

## ±5V Electrical Characteristics (A<sub>v</sub> = +2, R<sub>i</sub> = 750Ω, R<sub>L</sub> = 100Ω, V<sub>CC</sub> = ±5V, unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
			+25°C	+25°C	0 to 70°C		
Ambient Temperature	CLC5602IN/IM	+25°C	+25°C	0 to 70°C	-40 to 85°C		
<b>FREQUENCY DOMAIN RESPONSE</b>							
-3dB bandwidth	V <sub>o</sub> = 1.0V <sub>pp</sub>	135	115	105	100	MHz	
	V <sub>o</sub> = 4.0V <sub>pp</sub>	48	45	42	40	MHz	
-0.1dB bandwidth	V <sub>o</sub> = 1.0V <sub>pp</sub>	20	18	15	12	MHz	
gain peaking	<200MHz, V <sub>o</sub> = 1.0V <sub>pp</sub>	0	0.5	0.9	1.0	dB	
gain rolloff	<30MHz, V <sub>o</sub> = 1.0V <sub>pp</sub>	0.1	0.3	0.4	0.5	dB	
linear phase deviation	<30MHz, V <sub>o</sub> = 1.0V <sub>pp</sub>	0.15	0.3	0.4	0.4	deg	
differential gain	NTSC, R <sub>L</sub> = 150Ω	0.06	0.18	–	–	%	
differential phase	NTSC, R <sub>L</sub> = 150Ω	0.02	0.04	–	–	deg	
<b>TIME DOMAIN RESPONSE</b>							
rise and fall time	2V step	5.7	6.2	6.8	7.3	ns	
settling time to 0.05%	2V step	15	25	40	60	ns	
overshoot	2V step	18	20	22	22	%	
slew rate	2V step	300	225	190	175	V/μs	
<b>DISTORTION AND NOISE RESPONSE</b>							
2 <sup>nd</sup> harmonic distortion	2V <sub>pp</sub> , 1MHz	-86	-82	-79	-79	dBc	
	2V <sub>pp</sub> , 1MHz; R <sub>L</sub> = 1kΩ	-87	-83	-80	-80	dBc	
	2V <sub>pp</sub> , 5MHz	-70	-64	-61	-60	dBc	
3 <sup>rd</sup> harmonic distortion	2V <sub>pp</sub> , 1MHz	-85	-81	-78	-78	dBc	
	2V <sub>pp</sub> , 1MHz; R <sub>L</sub> = 1kΩ	-95	-90	-87	-87	dBc	
	2V <sub>pp</sub> , 5MHz	-66	-64	-61	-60	dBc	
equivalent input noise voltage (e <sub>ni</sub> )	>1MHz	3.4	4.4	4.9	4.9	nV/√Hz	
non-inverting current (i <sub>bn</sub> )	>1MHz	6.3	8.2	9.0	9.0	pA/√Hz	
inverting current (i <sub>bi</sub> )	>1MHz	8.7	11.3	12.4	12.4	pA/√Hz	
crosstalk (input referred)	10MHz, 1V <sub>pp</sub>	-72	–	–	–	dB	
<b>STATIC DC PERFORMANCE</b>							
input offset voltage		2	6	7	8	mV	
average drift		8	–	–	–	μV/°C	
input bias current (non-inverting)		5	12	16	17	μA	
average drift		40	–	–	–	nA/°C	
input bias current (inverting)		8	24	28	28	μA	
average drift		20	–	45	45	nA/°C	
power supply rejection ratio	DC	48	45	43	43	dB	
common-mode rejection ratio	DC	51	49	47	47	dB	
supply current (per channel)	R <sub>L</sub> = ∞	1.6	1.9	2.0	2.0	mA	
<b>MISCELLANEOUS PERFORMANCE</b>							
input resistance (non-inverting)		0.59	0.47	0.43	0.43	MΩ	
input capacitance (non-inverting)		1.45	2.15	2.15	2.15	pF	
common-mode input range		±4.2	±4.1	±4.1	±4.0	V	
output voltage range	R <sub>L</sub> = 100Ω	±3.8	±3.6	±3.6	±3.5	V	
output voltage range	R <sub>L</sub> = ∞	±4.0	±3.8	±3.8	±3.7	V	
output current		130	100	80	50	mA	B
output resistance, closed loop	DC	40	70	70	90	mΩ	

### Notes

B) The short circuit current can exceed the maximum safe output current.

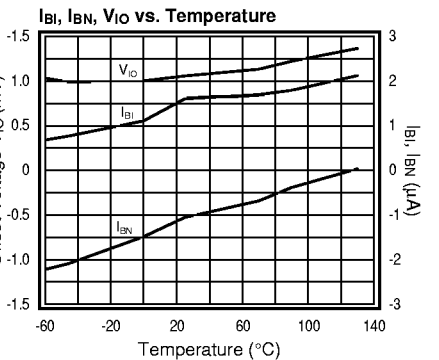
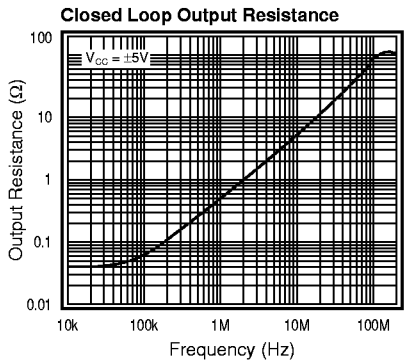
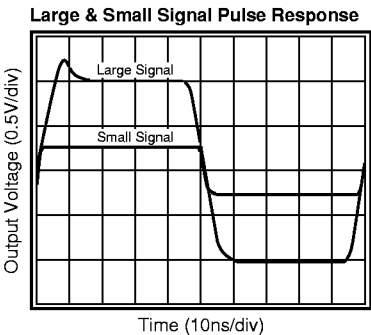
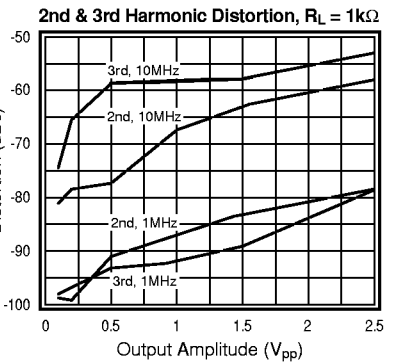
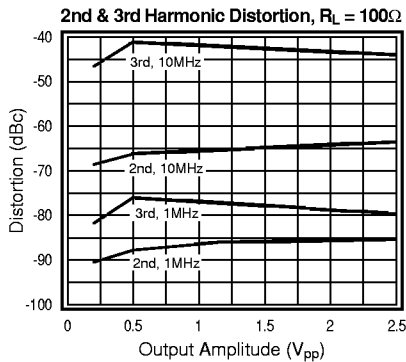
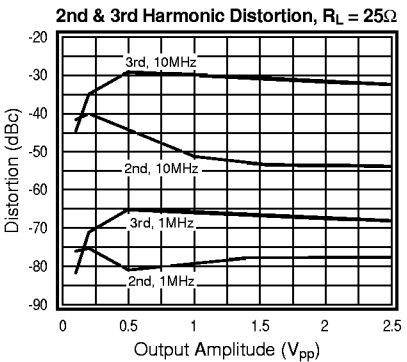
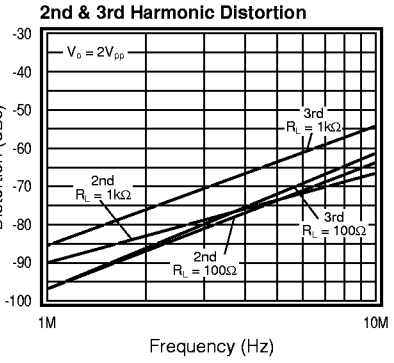
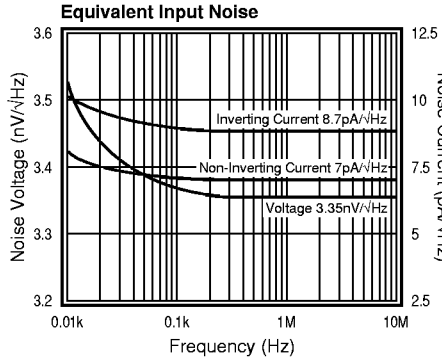
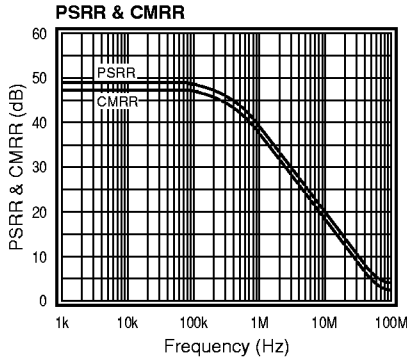
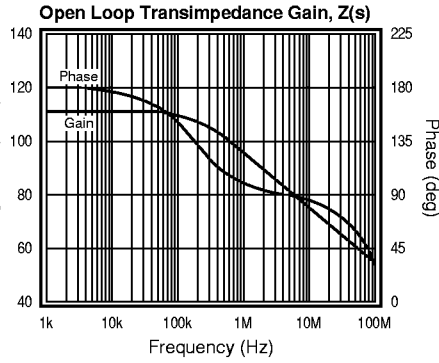
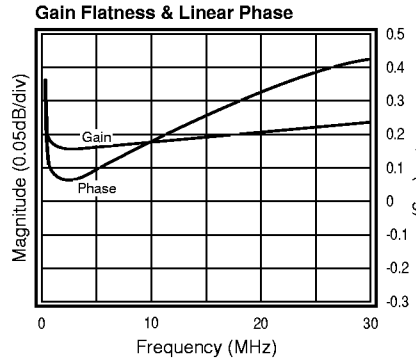
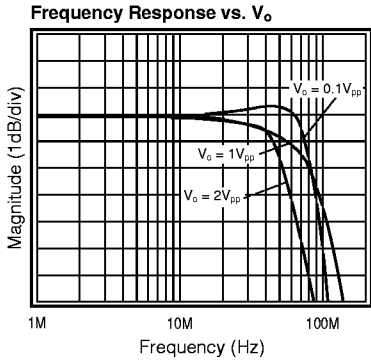
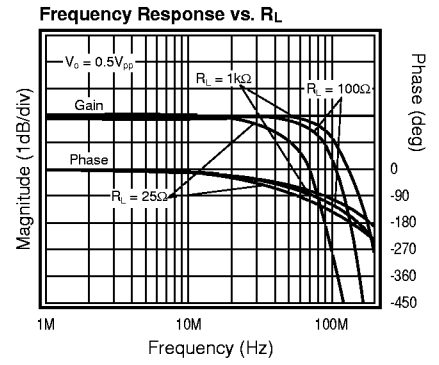
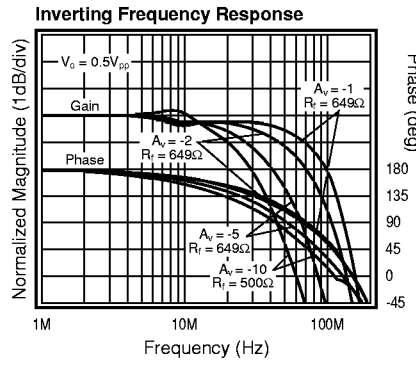
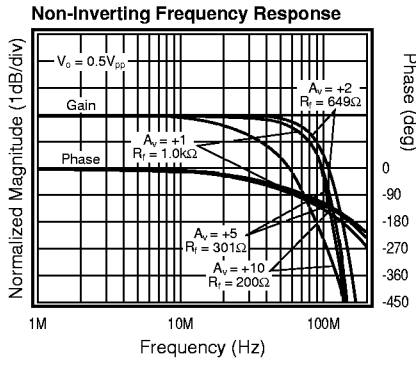
### Package Thermal Resistance

Package	θ <sub>JC</sub>	θ <sub>JA</sub>
Plastic (IN)	65°C/W	130°C/W
Surface Mount (IM)	50°C/W	145°C/W

### Ordering Information

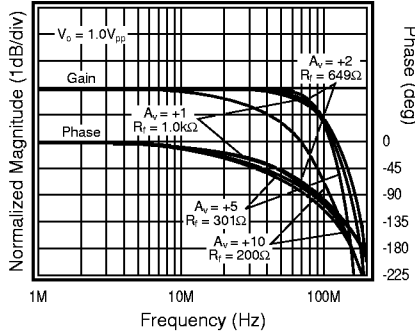
Model	Temperature Range	Description
CLC5602IN	-40°C to +85°C	8-pin PDIP
CLC5602IM	-40°C to +85°C	8-pin SOIC
CLC5602IMX	-40°C to +85°C	8-pin SOIC tape & reel

**+5V Typical Performance** ( $A_v = +2$ ,  $R_f = 750\Omega$ ,  $R_L = 100\Omega$ ,  $V_s = +5V^1$ ,  $V_{cm} = V_{EE} + (V_s/2)$ ,  $R_L$  tied to  $V_{cm}$ , unless specified)

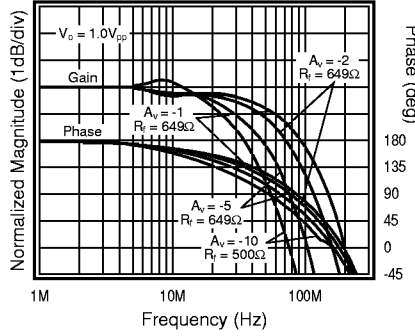


# ±5V Typical Performance ( $A_v = +2$ , $R_f = 750\Omega$ , $R_L = 100\Omega$ , $V_{CC} = \pm 5V$ , unless specified)

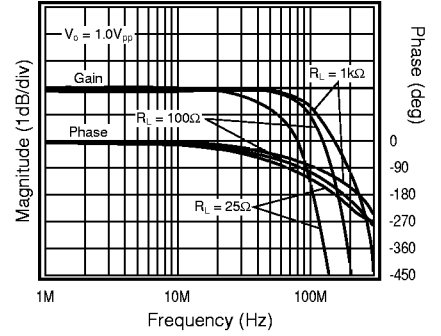
**Frequency Response**



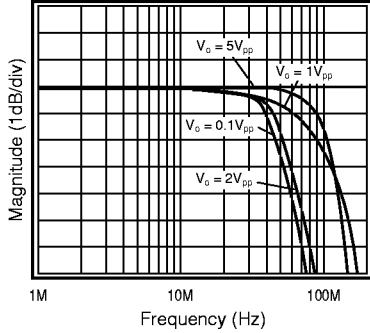
**Inverting Frequency Response**



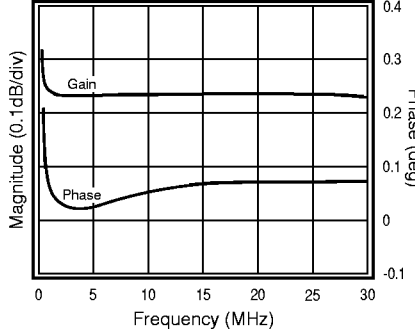
**Frequency Response vs.  $R_L$**



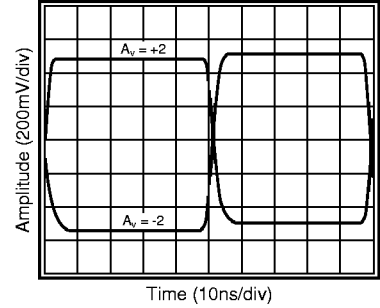
**Frequency Response vs.  $V_o$**



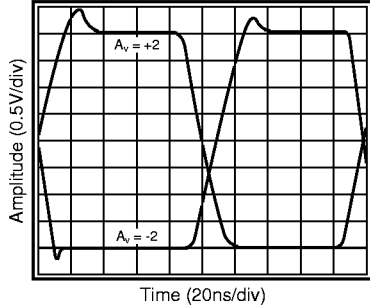
**Gain Flatness & Linear Phase**



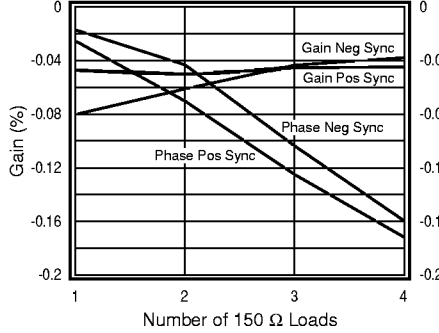
**Small Signal Pulse Response**



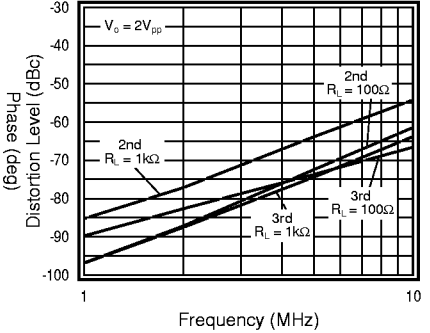
**Large Signal Pulse Response**



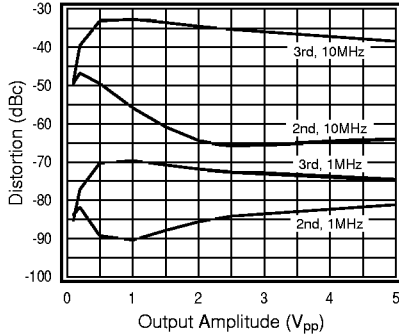
**Differential Gain & Phase**



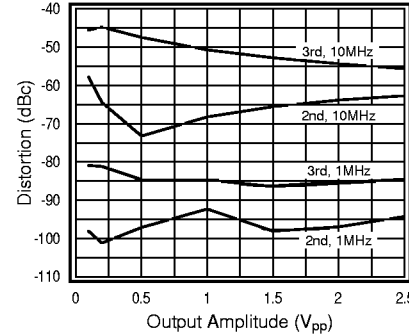
**2nd & 3rd Harmonic Distortion vs. Frequency**



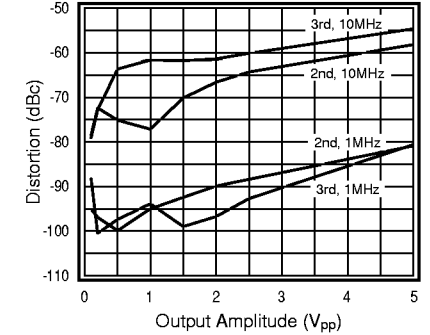
**2nd & 3rd Harmonic Distortion,  $R_L = 25\Omega$**



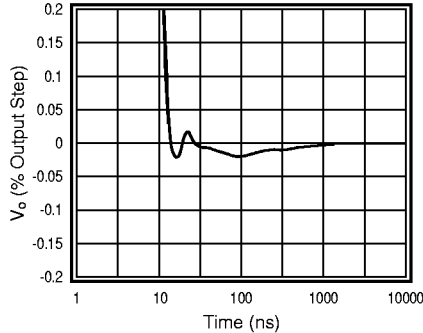
**2nd & 3rd Harmonic Distortion,  $R_L = 100\Omega$**



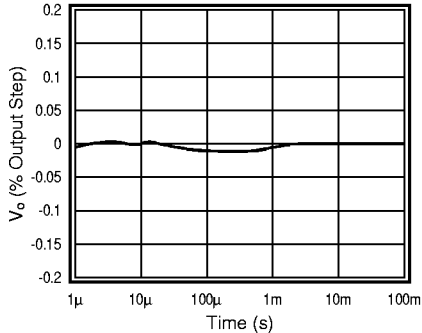
**2nd & 3rd Harmonic Distortion,  $R_L = 1k\Omega$**



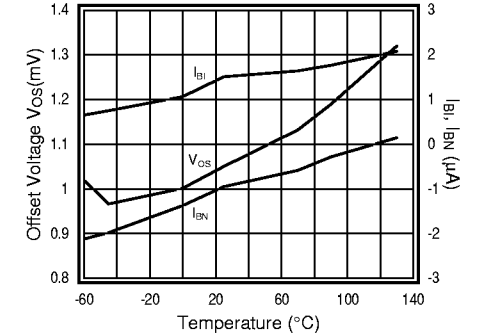
**Short Term Settling Time**



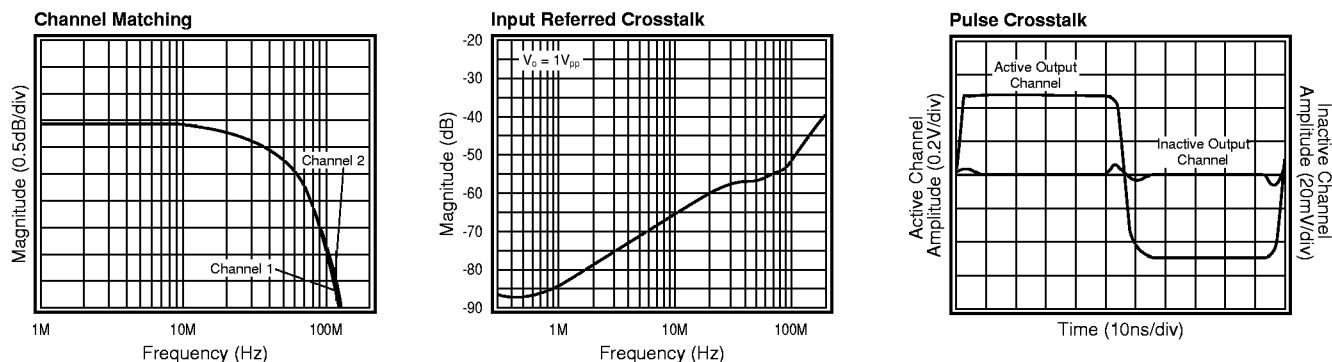
**Long Term Settling Time**



**$I_{BI}$ ,  $I_{BN}$ ,  $V_{OS}$  vs. Temperature**



## ±5V Typical Channel Matching Performance ( $A_v = +2$ , $R_f = 750\Omega$ , $R_L = 100\Omega$ , $V_{CC} = \pm 5V$ , unless specified)



## CLC5602 OPERATION

The CLC5602 is a current feedback amplifier built in an advanced complementary bipolar process. The CLC5602 operates from a single 5V supply or dual ±5V supplies. Operating from a single supply, the CLC5602 has the following features:

- Provides 100mA of output current while consuming 7.5mW of power
- Offers low -80/-82dB 2nd and 3rd harmonic distortion
- Provides BW > 60MHz and 1MHz distortion < -65dBc at  $V_o = 2.0V_{pp}$

The CLC5602 performance is further enhanced in ±5V supply applications as indicated in the **±5V Electrical Characteristics** table and **±5V Typical Performance** plots.

### Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \quad \text{Equation 1}$$

where:

- $A_v$  is the closed loop DC voltage gain
- $R_f$  is the feedback resistor
- $Z(j\omega)$  is the CLC5602's open loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$  is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between  $R_f$  and  $Z(j\omega)$  dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing  $R_f$  has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

Refer to the **Feedback Resistor Selection** section for more details on selecting a feedback resistor value.

## CLC5602 DESIGN INFORMATION

### Single Supply Operation ( $V_{CC} = +5V$ , $V_{EE} = GND$ )

The specifications given in the **±5V Electrical Characteristics** table for single supply operation are measured with a common mode voltage ( $V_{cm}$ ) of 2.5V.  $V_{cm}$  is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5V supply, the Common Mode Input Range (CMIR) of the CLC5602 is typically +0.8V to

+4.2V. The typical output range with  $R_L=100\Omega$  is +1.0V to +4.0V.

For single supply DC coupled operation, keep input signal levels above 0.8V DC. For input signals that drop below 0.8V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

### DC Coupled Single Supply Operation

Figures 1 and 2 show the recommended non-inverting and inverting configurations for input signals that remain above 0.8V DC.

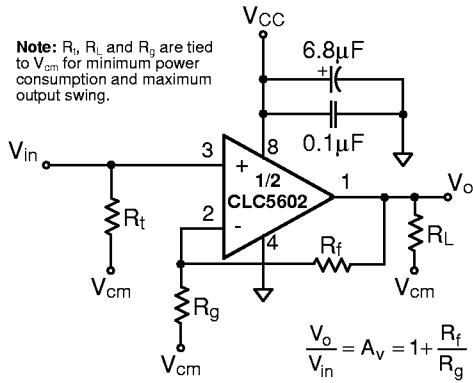


Figure 1: Non-Inverting Configuration

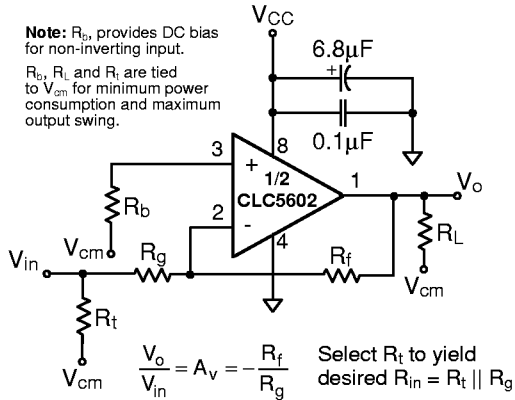


Figure 2: Inverting Configuration

### AC Coupled Single Supply Operation

Figures 3 and 4 show possible non-inverting and inverting configurations for input signals that go below 0.8V DC. The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to  $V_{CC} \div 2 = 2.5V$  (For  $V_{CC} = +5V$ ).

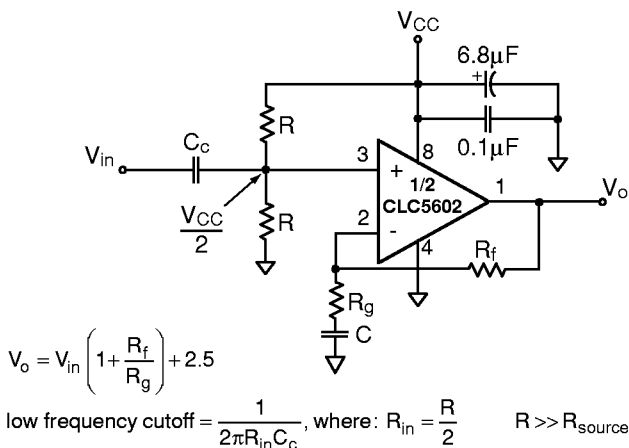


Figure 3: AC Coupled Non-Inverting Configuration

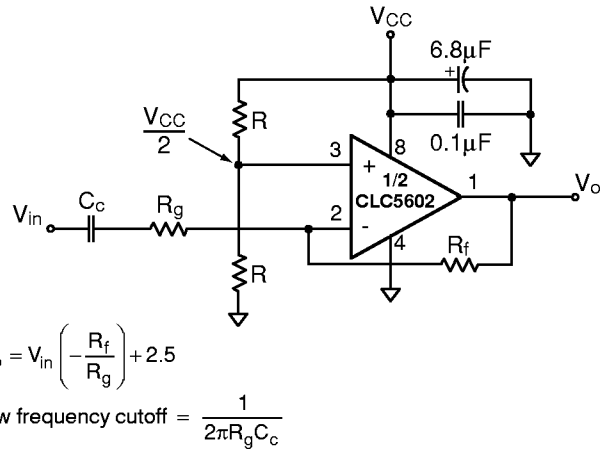


Figure 4: AC Coupled Inverting Configuration

### Dual Supply Operation

The CLC5602 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in Figures 5 and 6.

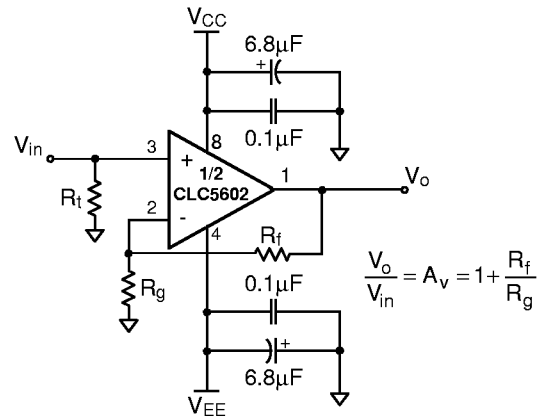


Figure 5: Dual Supply Non-Inverting Configuration

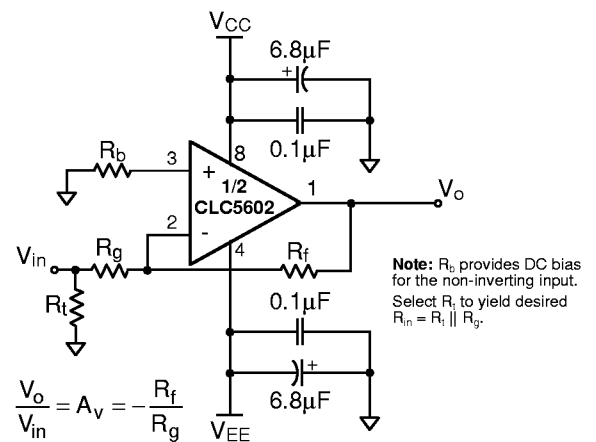


Figure 6: Dual Supply Inverting Configuration

## Feedback Resistor Selection

The feedback resistor,  $R_f$ , affects the loop gain and frequency response of a current feedback amplifier. Optimum performance of the CLC5602, at a gain of +2V/V, is achieved with  $R_f$  equal to 750Ω. The frequency response plots in the **Typical Performance** sections illustrate the recommended  $R_f$  for several gains. These recommended values of  $R_f$  provide the maximum bandwidth with minimal peaking. Within limits,  $R_f$  can be adjusted to optimize the frequency response.

- Decrease  $R_f$  to peak frequency response and extend bandwidth
- Increase  $R_f$  to roll off frequency response and compress bandwidth

As a rule of thumb, if the recommended  $R_f$  is doubled, then the bandwidth will be cut in half.

## Unity Gain Operation

The recommended  $R_f$  for unity gain (+1V/V) operation is 1kΩ.  $R_g$  is left open. Parasitic capacitance at the inverting node may require a slight increase in  $R_f$  to maintain a flat frequency response.

## Load Termination

The CLC5602 can source and sink near equal amounts of current. For optimum performance, the load should be tied to  $V_{cm}$ .

## Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC5602 will improve stability and settling performance. The **Frequency Response vs.  $C_L$**  plot, shown below in Figure 7, gives the recommended series resistance value for optimum flatness at various capacitive loads.

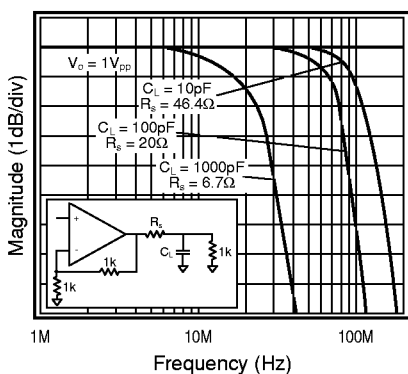


Figure 7: Frequency Response vs.  $C_L$

## Transmission Line Matching

One method for matching the characteristic impedance ( $Z_0$ ) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier.

Figure 8 shows typical inverting and non-inverting circuit configurations for matching transmission lines.

Non-inverting gain applications:

- Connect  $R_g$  directly to ground.
- Make  $R_1$ ,  $R_2$ ,  $R_6$ , and  $R_7$  equal to  $Z_0$ .
- Use  $R_3$  to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

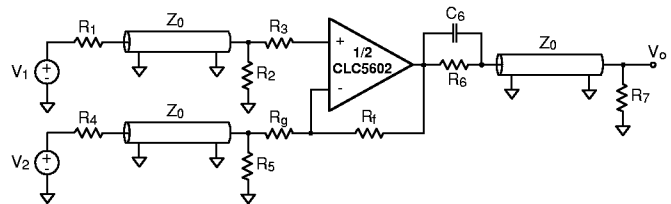


Figure 8: Transmission Line Matching

Inverting gain applications:

- Connect  $R_3$  directly to ground.
- Make the resistors  $R_4$ ,  $R_6$ , and  $R_7$  equal to  $Z_0$ .
- Make  $R_5 \parallel R_g = Z_0$ .

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use  $C_6$  to match the output transmission line over a greater frequency range.  $C_6$  compensates for the increase of the amplifier's output impedance with frequency.

## Power Dissipation

Follow these steps to determine the power consumption of the CLC5602:

1. Calculate the quiescent (no-load) power:  
 $P_{amp} = I_{CC} (V_{CC} - V_{EE})$
2. Calculate the RMS power at the output stage:  
 $P_o = (V_{CC} - V_{load}) (I_{load})$ , where  $V_{load}$  and  $I_{load}$  are the RMS voltage and current across the external load.
3. Calculate the total RMS power:  
 $P_t = P_{amp} + P_o$

The maximum power that the DIP and SOIC packages can dissipate at a given temperature is illustrated in Figure 9. The power derating curve for any CLC5602 package can be derived by utilizing the following equation:

$$\frac{(175^\circ - T_{amb})}{\theta_{JA}}$$

where

$T_{amb}$  = Ambient temperature ( $^\circ\text{C}$ )

$\theta_{JA}$  = Thermal resistance, from junction to ambient, for a given package ( $^\circ\text{C/W}$ )



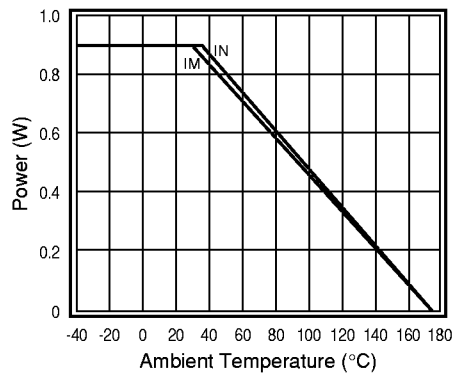


Figure 9: Power Derating Curves

### Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC5602 (CLC730038-DIP, CLC730036-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8 $\mu$ F tantalum and 0.1 $\mu$ F ceramic capacitors on both supplies.
- Place the 6.8 $\mu$ F capacitors within 0.75 inches of the power pins.
- Place the 0.1 $\mu$ F capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

### Evaluation Board Information

A data sheet is available for the CLC730038/ CLC730036 evaluation boards. The evaluation board data sheet provides:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

### SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The *readme* file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the readme file.

## Application Circuits

### Single Supply Cable Driver

The typical application shown below shows one of the CLC5602 amplifiers driving 10m of 75 $\Omega$  coaxial cable. The CLC5602 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at  $V_o$ .

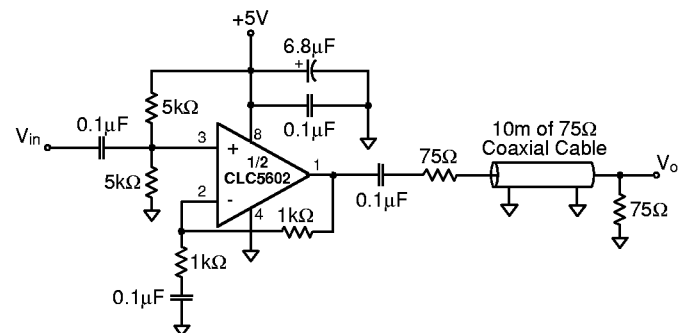


Figure 10: Single Supply Cable Driver

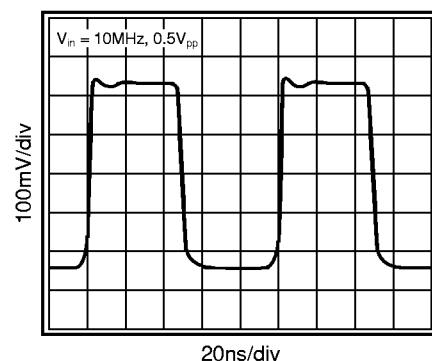
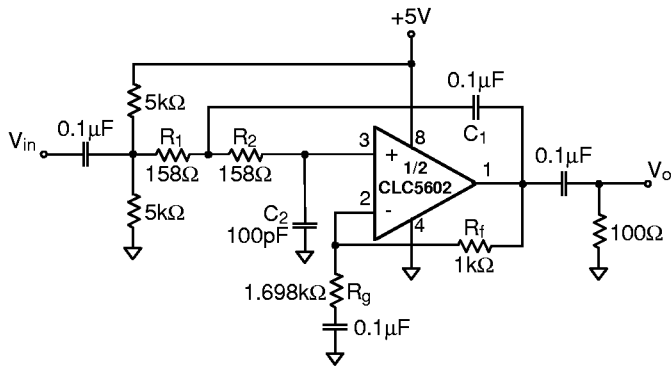


Figure 11: Response After 10m of Cable

### Single Supply Lowpass Filter

Figures 12 and 13 illustrate a lowpass filter and design equations. The circuit operates from a single supply of +5V. The voltage divider biases the non-inverting input to 2.5V. And the input is AC coupled to prevent the need for level shifting the input signal at the source. Use the design equations to determine  $R_1$ ,  $R_2$ ,  $C_1$ , and  $C_2$  based on the desired Q and corner frequency.



**Figure 12: Lowpass Filter Topology**

$$\text{Gain} = K = 1 + \frac{R_f}{R_g}$$

$$\text{Corner frequency} = \omega_c = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{1}{\sqrt{\frac{R_2 C_2}{R_1 C_1} + \frac{R_1 C_2}{R_2 C_1} + (1-K) \sqrt{\frac{R_1 C_1}{R_2 C_2}}}}$$

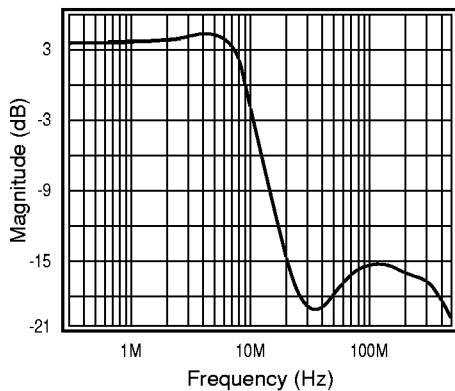
For  $R_1 = R_2 = R$  and  $C_1 = C_2 = C$

$$\omega_c = \frac{1}{RC}$$

$$Q = \frac{1}{(3-K)}$$

**Figure 13: Design Equations**

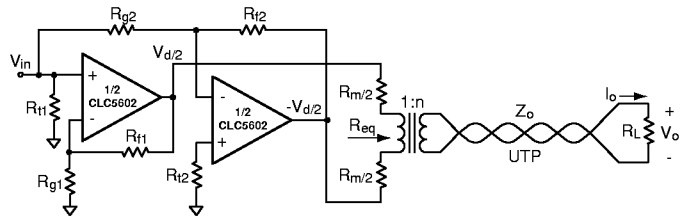
This example illustrates a lowpass filter with  $Q = 0.707$  and corner frequency  $f_c = 10\text{MHz}$ . A  $Q$  of 0.707 was chosen to achieve a maximally flat, Butterworth response. Figure 14 indicates the filter response.



**Figure 14: Lowpass Response**

## Differential Line Driver With Load Impedance Conversion

The circuit shown in the **Typical Application** schematic on the front page and in Figure 15, operates as a differential line driver. The transformer converts the load impedance to a value that best matches the CLC5602's output capabilities. The single-ended input signal is converted to a differential signal by the CLC5602. The line's characteristic impedance is matched at both the input and the output. The schematic shows Unshielded Twisted Pair for the transmission line; other types of lines can also be driven.



**Figure 15: Differential Line Driver with Load Impedance Conversion**

Set up the CLC5602 as a difference amplifier:

$$\frac{V_d}{V_{in}} = 2 \cdot \left( 1 + \frac{R_{f1}}{R_{g1}} \right) = 2 \cdot \frac{R_{f2}}{R_{g2}}$$

Make the best use of the CLC5602's output drive capability as follows:

$$R_m + R_{eq} = \frac{2 \cdot V_{max}}{I_{max}}$$

where  $R_{eq}$  is the transformed value of the load impedance,  $V_{max}$  is the Output Voltage Range, and  $I_{max}$  is the maximum Output Current.

Match the line's characteristic impedance:

$$R_L = Z_o$$

$$R_m = R_{eq}$$

$$n = \sqrt{\frac{R_L}{R_{eq}}}$$

Select the transformer so that it loads the line with a value very near  $Z_o$  over frequency range. The output impedance of the CLC5602 also affects the match. With an ideal transformer we obtain:

$$\text{Return Loss} = -20 \cdot \log_{10} \left| \frac{n^2 \cdot Z_{o(5602)}(j\omega)}{Z_o} \right|, \text{dB}$$

where  $Z_{o(5602)}(j\omega)$  is the output impedance of the CLC5602 and  $|Z_{o(5602)}(j\omega)| \ll R_{m1}$ .

The load voltage and current will fall in the ranges:

$$|V_o| \leq n \cdot V_{max}$$

$$|I_o| \leq \frac{I_{max}}{n}$$

The CLC5602's high output drive current and low distortion make it a good choice for this application.

### Full Duplex Cable Driver

The circuit shown in Figure 16 below, operates as a full duplex cable driver which allows simultaneous transmission and reception of signals on one transmission line. The circuit on either side of the transmission line uses are CLC5602 as a cable driver, and the second CLC5602 as a receiver.  $V_{oA}$  is an attenuated version of  $V_{inA}$ , while  $V_{oB}$  is an attenuated version of  $V_{inB}$ .

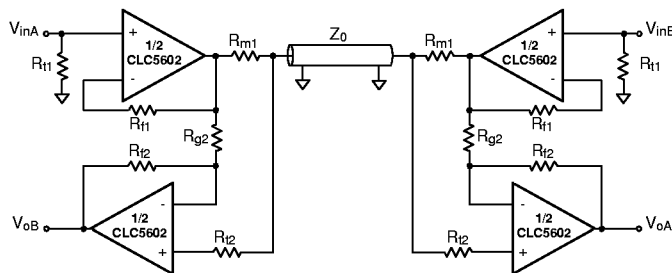


Figure 16: Full Duplex Cable Driver

$R_{m1}$  is used to match the transmission line.  $R_{f2}$  and  $R_{g2}$  set the DC gain of the CLC5602, which is used in a difference mode.  $R_{f2}$  provides good CMRR and DC offset. The transmitting CLC5602's are shown in a unity gain configuration because they consume the least power of any gain, for a given load. For proper operation we need  $R_{f2} = R_{g2}$ .

The receiver output voltages are:

$$V_{outA(B)} \approx V_{inA(B)} \cdot A + \frac{V_{inB(A)}}{2} \cdot \left( 1 - \frac{R_{f2}}{R_{g2}} + \frac{Z_{o(5602)}(j\omega)}{R_{m1}} \right)$$

where A is the attenuation of the cable,  $Z_{o(5602)}(j\omega)$  is the output impedance of the CLC5602 (see the **Closed-Loop Output Resistance** plot), and  $|Z_{o(5602)}(j\omega)| \ll R_{m1}$ .

We selected the component values as follows:

- $R_{f1} = 1.0k\Omega$ , the recommended value for the CLC5602 at unity gain
- $R_{m1} = Z_o = 50\Omega$ , the characteristic impedance of the transmission line
- $R_{f2} = R_{g2} = 750\Omega \geq R_{m1}$ , the recommended value for the CLC5602 at  $A_v = 2$
- $R_{t2} = (R_{f2} || R_{g2}) - \frac{R_{m1}}{2} = 25\Omega$

These values give excellent isolation from the other input:

$$\frac{V_{oA(B)}}{V_{inB(A)}} \approx -38dB, f = 5.0MHz$$

The CLC5602 provides large output current drive, while consuming little supply current, at the nominal bias point. It also produces low distortion with large signal swings and heavy loads. These features make the CLC5602 an excellent choice for driving transmission lines.

---

### Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

#### Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



#### National Semiconductor Corporation

1111 West Bardin Road  
Arlington, TX 76017  
Tel: 1(800) 272-9959  
Fax: 1(800) 737-7018

#### National Semiconductor Europe

Fax: (+49) 0-180-530 85 86  
E-mail: europe.support.nsc.com  
Deutsch Tel: (+49) 0-180-530 85 85  
English Tel: (+49) 0-180-532 78 32  
Francais Tel: (+49) 0-180-532 93 58  
Italiano Tel: (+49) 0-180-534 16 80

#### National Semiconductor Hong Kong Ltd.

13th Floor, Straight Block  
Ocean Centre, 5 Canton Road  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

#### National Semiconductor Japan Ltd.

Tel: 81-043-299-2309  
Fax: 81-043-299-2408

---

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.