## Single and Dual Ultra-Low Noise, Ultra-Low Distortion, Low Power Op Amp

The ISL55190 and ISL55290 are single and dual high speed operational amplifiers featuring low noise, low distortion, and rail-to-rail output drive capability. They are designed to operate with single and dual supplies from +5VDC (±2.5VDC) down to +3VDC (±1.5VDC). These amplifiers draw 16mA of quiescent supply current per amplifier. For power conservation, this family offers a low-power shutdown mode that reduces supply current to 21μA and places the amplifiers' output into a high impedance state. The ISL55190 ENABLE logic places the device in the shutdown mode with EN = 0 and the ISL55290 is placed in the shutdown mode with $\overline{EN}$ = 1.

These amplifiers have excellent input and output overload recovery times and outputs that swing rail-to-rail. Their input common mode voltage range includes ground. The ISL55190 and ISL55290 are stable at gains as low as 5 with an input referred noise voltage of 1.2nV/√Hz and harmonic distortion products -95dBc (2nd) and -92dBc (3rd) below a 4MHz 2V$_{P-P}$ signal.

The ISL55190 is available in space-saving 8 Ld DFN and 8 Ld SOIC packages. The ISL55290 is available in a 10 Ld MSOP package.

## Ordering Information

| PART NUMBER (Note) | PART MARKING | TAPE AND REEL | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL55190IBZ | 55190 IBZ | - | 8 Ld SOIC | MDP0027 |
| ISL55190IBZ-T13 | 55190 IBZ | 13" (2,500 pcs) | 8 Ld SOIC Tape and Reel | MDP0027 |
| ISL55190IRZ | 190Z | - | 8 Ld DFN | L8.3x3D |
| ISL55190IRZ-T13 | 190Z | 13" (2,500 pcs) | 8 Ld DFN Tape and Reel | L8.3x3D |
| ISL55290IUZ | 5290Z | - | 10 Ld MSOP | MDP0043 |
| ISL55290IUZ-T13 | 5290Z | 13" (2500 pcs) | 10 Ld MSOP Tape and Reel | MDP0043 |
| *Coming Soon* ISL55190EVAL1Z | Evaluation Board | | | |
| *Coming Soon* ISL55290EVAL1Z | Evaluation Board | | | |

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

- 1.2nV/√Hz input voltage noise, f$_O$ = 1kHz

- Harmonic Distortion -95dBc, -92dBc, f$_O$ = 4MHz

- Stable at gains as low as 5

- 800MHz gain bandwidth product (A$_V$ = 5)

- 268V/μs typical slew rate

- 16mA typical supply current (21μA in disable mode)

- 300μV typical offset voltage

- 25μA typical input bias current

- 3V to 5V single supply voltage range

- Rail-to-rail output

- Enable pin

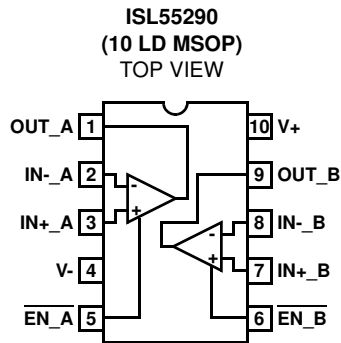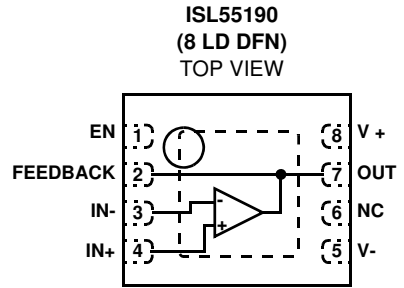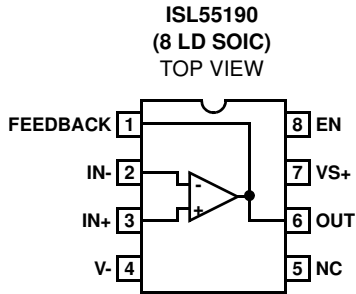- Pb-free plus anneal available (RoHS compliant)

## Applications

- High speed pulse applications

- Low noise signal processing

- ADC buffers

- DAC output amplifiers

- Radio systems

- Portable equipment

TABLE 1. ENABLE LOGIC

| | ENABLE | DISABLE |
|---|---|---|
| ISL55190 | EN = 1 | EN = 0 |
| ISL55290 | $\overline{EN}$ = 0 | $\overline{EN}$ = 1 |

## *Pinouts*

**ISL55190**
**(8 LD SOIC)**
TOP VIEW

```
FEEDBACK  1        8  EN
     IN-  2        7  VS+
     IN+  3        6  OUT
      V-  4        5  NC
```

**ISL55190**
**(8 LD DFN)**
TOP VIEW

```
      EN  1        8  V +
FEEDBACK  2        7  OUT
     IN-  3        6  NC
     IN+  4        5  V-
```

**ISL55290**
**(10 LD MSOP)**
TOP VIEW

```
 OUT_A  1        10  V+
 IN-_A  2         9  OUT_B
 IN+_A  3         8  IN-_B
    V-  4         7  IN+_B
  EN_A  5         6  EN_B
```

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## ISL55190, ISL55290

### Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5V
Supply Turn On Voltage Slew Rate . . . . . . . . . . . . . . . . . . . . . 1V/μs
Differential Input Current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5mA
Differential Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.5V
Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . V- - 0.5V to V+ + 0.5V
ESD Rating
   Human Body Model (Per MIL-STD-883 Method 3015.7) . . . . .3kV
   Machine Model (Per EIAJ ED-4701 Method C-111) . . . . . . . .300V

### Thermal Information

Thermal Resistance                              $\theta_{JA}$ (°C/W)
   8 Ld DFN Package . . . . . . . . . . . . . . . . . . . . . . . . .   65.75
   8 Ld SO Package . . . . . . . . . . . . . . . . . . . . . . . . . .   110
   10 Ld MSOP Package . . . . . . . . . . . . . . . . . . . . . . .   115
Ambient Operating Temperature Range . . . . . . . . . . .-40°C to +85°C
Storage Temperature Range . . . . . . . . . . . . . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . . . . . . . . . . . . . . . . . .+125°C
Pb-free reflow profile . . . . . . . . . . . . . . . . . . . . . . . . . .see link below
   http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

### Electrical Specifications

V+ = 5V, V -= GND, $R_L$ = 1kΩ, $R_G$ = 30Ω, $R_F$ = 120Ω. unless otherwise specified. Parameters are per amplifier. All values are at V+ = 5V, $T_A$ = +25°C

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC SPECIFICATIONS** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | | -1100 | -300 | 500 | μV |
| $\dfrac{\Delta V_{OS}}{\Delta T}$ | Input Offset Drift vs Temperature | -40°C to +85°C | | 0.43 | | μV/°C |
| $I_{OS}$ | Input Offset Current | | -1.3 | -0.3 | 0.7 | μA |
| $I_B$ | Input Bias Current | | | -25 | -40 | μA |
| $V_{CM}$ | Common-Mode Voltage Range | | 0 | | 3.8 | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = 0V to 3.8V | 80 | 95 | | dB |
| PSRR | Power Supply Rejection Ratio | V+ = 3V to 5V | 80 | 100 | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = 0.5V to 4V, $R_L$ = 1kΩ | 85 | 115 | | dB |
| $V_{OUT}$ | Maximum Output Voltage Swing | Output low, $R_L$ = 1kΩ | | 39 | 100 | mV |
| | | Output high, $R_L$ = 1kΩ, V+= 5V | 4.960 | 4.978 | | V |
| $I_{S,ON}$ | Supply Current, Enabled | ISL55190 | | 16 | 20 | mA |
| | | ISL55290 | | 30 | 38 | mA |
| $I_{S,OFF}$ | Supply Current, Disabled | | | 21 | 49 | μA |
| $I_{O+}$ | Short-Circuit Output Current | $R_L$ = 10Ω | 110 | 130 | | mA |
| $I_{O-}$ | Short-Circuit Output Current | $R_L$ = 10Ω | 110 | 130 | | mA |
| $V_{SUPPLY}$ | Supply Operating Range | V+ to V- | 3 | | 5 | V |
| $V_{INH}$ | ENABLE High Level | Referred to -V | 2 | | | V |
| $V_{INL}$ | ENABLE Low Level | Referred to -V | | | 0.8 | V |
| $I_{ENH}$ | ENABLE Input High Current $V_{EN}$ = V+ | ISL55190 (EN) | | 20 | 80 | nA |
| | | ISL55290 ($\overline{EN}$) | | 0.8 | 1.5 | μA |
| $I_{ENL}$ | ENABLE Input Low Current $V_{EN}$ = V- | ISL55190 (EN) | | 5 | 6.2 | μA |
| | | ISL55290 ($\overline{EN}$) | | 20 | 80 | nA |

# ISL55190, ISL55290

**Electrical Specifications**   $V+ = 5V$, $V- = GND$, $R_L = 1k\Omega$, $R_G = 30\Omega$, $R_F = 120\Omega$. unless otherwise specified. Parameters are per amplifier. All values are at $V+ = 5V$, $T_A = +25°C$

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AC SPECIFICATIONS** | | | | | | |
| GBW | Gain Bandwidth Product | $A_V = +5$; $V_{OUT} = 100mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ | | 800 | | MHz |
| HD (4 MHz) | 2nd Harmonic Distortion | $A_V = 5$; $V_{OUT} = 2V_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ | | -95 | | dBc |
| | 3rd Harmonic Distortion | | | -92 | | dBc |
| ISO | Off-state Isolation; $\overline{EN} = 1$ ISL55290; EN = 0 ISL55190 | $f_O = 10MHz$; $A_V = 5$; $V_{IN} = 640mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$; $C_L = 1.2pF$ | | -65 | | dB |
| X-TALK ISL55290 | Channel-to-Channel Crosstalk | $f_O = 10MHz$; $A_V = 5$; $V_{OUT}$ (Driven Channel) = $640mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$; $C_L = 1.2pF$ | | -75 | | dB |
| PSRR | Power Supply Rejection Ratio $f_O = 10MHz$; | $V_S = \pm2.5V$; $A_V = 5$; $V_{SOURCE} = 640mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$; $C_L = 1.2pF$ | | -45 | | dB |
| CMRR | Input Common Mode Rejection Ratio; $f_O = 10MHz$; | $V_S = \pm2.5V$; $A_V = 5$; $V_{CM} = 640mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$; $C_L = 1.2pF$ | | -38 | | dB |
| $V_N$ | Input Referred Voltage Noise | $f_O = 1kHz$ | | 1.2 | | nV/√Hz |
| IN | Input Referred Current Noise | $f_O = 10kHz$ | | 6 | | pA/√Hz |
| **TRANSIENT RESPONSE** | | | | | | |
| SR | Slew Rate | | 163 | 268 | | V/uS |
| $t_r$, $t_f$ Large Signal | Rise Time, $t_r$ 10% to 90% | $A_V = 5$; $V_{OUT} = 3.5V_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ $C_L = 1.2pF$ | | 11.2 | | ns |
| | Fall Time, $t_f$ 10% to 90% | | | 9.8 | | ns |
| | Rise Time, $t_r$ 10% to 90% | $A_V = 5$; $V_{OUT} = 1V_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ $C_L = 1.2pF$ | | 4.4 | | ns |
| | Fall Time, $t_f$ 10% to 90% | | | 4.0 | | ns |
| $t_r$, $t_f$, Small Signal | Rise Time, $t_r$ 10% to 90% | $A_V = 5$; $V_{OUT} = 1V_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ $C_L = 1.2pF$ | | 2.2 | | ns |
| | Fall Time, $t_f$ 10% to 90% | | | 2.0 | | ns |
| $t_{pd}$ | Propagation Delay 10% $V_{IN}$ to 10% $V_{OUT}$ | $A_V = 5$; $V_{OUT} = 100mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ $C_L = 1.2pF$ | | 1.6 | | ns |
| $t_{IOL}$ | Positive Input Overload Recovery Time, $t_{IOL+}$; 10% $V_{IN}$ to 10% $V_{OUT}$ | $V_S = \pm2.5V$; $A_V = 5$; $V_{IN} = +V_{CM} +0.1V$; $R_f/R_g = 402\Omega/100\Omega$; $C_L = 1.2pF$ | | 15 | | ns |
| | Negative Input Overload Recovery Time, $t_{IOL-}$; 10% $V_{IN}$ to 10% $V_{OUT}$ | $V_S = \pm2.5V$; $A_V = 5$; $V_{IN} = -V -0.5V$; $R_f/R_g = 402\Omega/100\Omega$; $C_L = 1.2pF$ | | 18 | | ns |
| $t_{OOL}$ | Positive Output Overload Recovery Time, $t_{OOL+}$; 10% $V_{IN}$ to 10% $V_{OUT}$ | $V_S = \pm2.5V$; $A_V = 5$; $V_{IN} = 1.1V_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$; $C_L = 1.2pF$ | | 17 | | ns |
| | Negative Output Overload Recovery Time, $t_{OOL-}$; 10% $V_{IN}$ to 10% $V_{OUT}$ | $V_S = \pm2.5V$; $A_V = 5$; $V_{IN} = 1.1V_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$; $C_L = 1.2pF$ | | 17 | | ns |
| $t_{EN}$ ISL55190 | ENABLE to Output Turn-on Delay Time; 10% EN to 10% $V_{OUT}$ | $A_V = 5$; $V_{IN} = 500mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ $C_L = 1.2pF$ | | 420 | | ns |
| | ENABLE to Output Turn-off Delay Time; 10% EN to 10% $V_{OUT}$ | $A_V = 5$; $V_{IN} = 500mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ $C_L = 1.2pF$ | | 240 | | ns |
| $t\overline{EN}$ ISL55290 | ENABLE to Output Turn-on Delay Time; 10% $\overline{EN}$ to 10% $V_{OUT}$ | $A_V = 5$; $V_{IN} = 500mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ $C_L = 1.2pF$ | | 160 | | ns |
| | ENABLE to Output Turn-off Delay Time;10% $\overline{EN}$ to 10% $V_{OUT}$ | $A_V = 5$; $V_{IN} = 500mV_{P-P}$; $R_f/R_g = 402\Omega/100\Omega$ $C_L = 1.2pF$ | | 32 | | ns |

## Typical Performance Curves
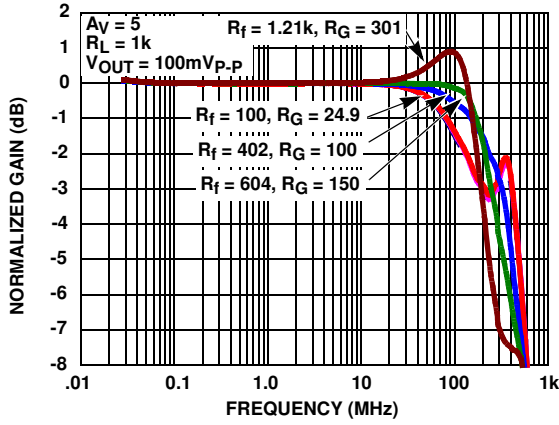


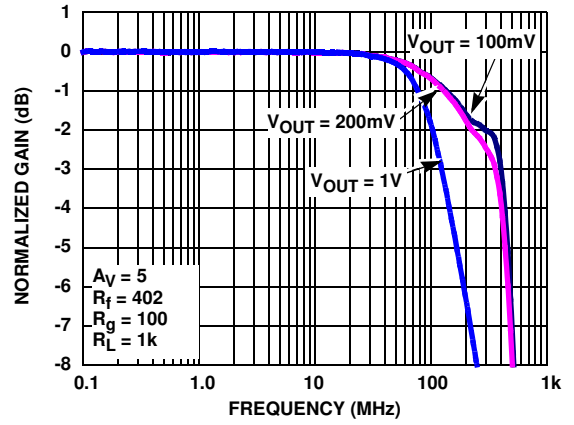FIGURE 1. GAIN vs FREQUENCY vs $R_f$ AND $R_g$
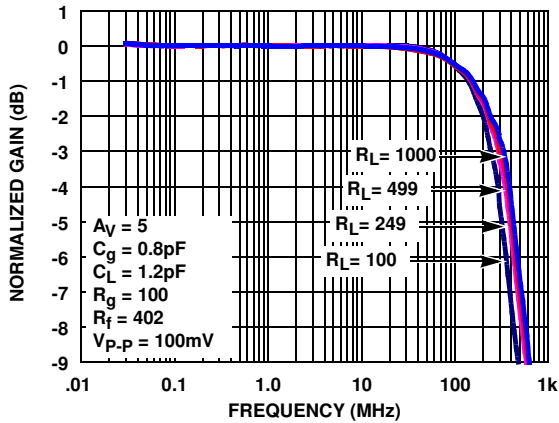


FIGURE 2. GAIN vs FREQUENCY vs $V_{OUT}$
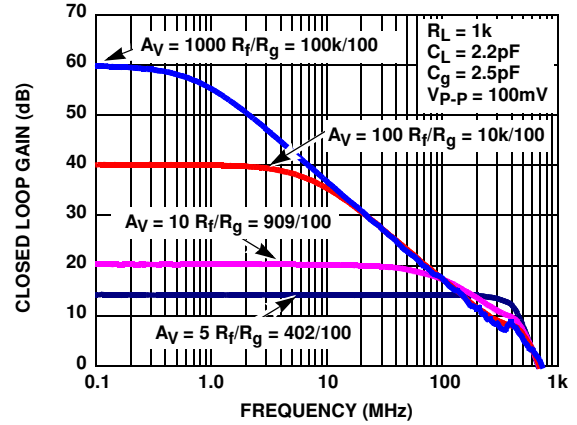


FIGURE 3. ISL55290 GAIN vs FREQUENCY vs $R_L$



FIGURE 4. CLOSED LOOP GAIN vs FREQUENCY



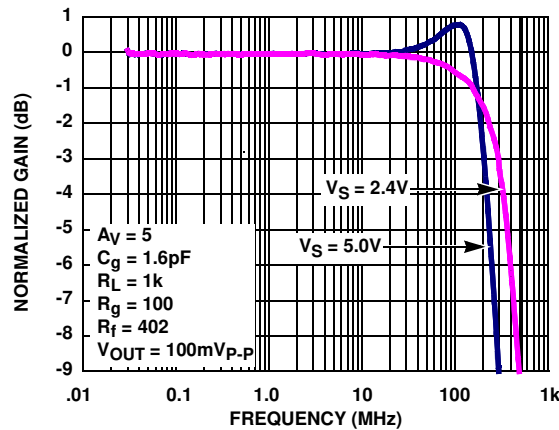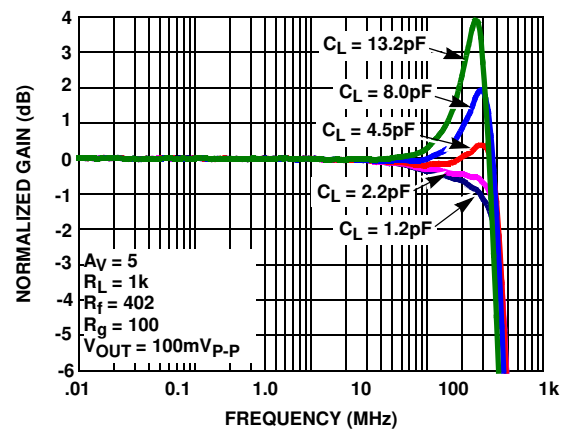FIGURE 5. GAIN vs FREQUENCY vs VS



FIGURE 6. ISL55190 GAIN vs FREQUENCY vs $C_L$
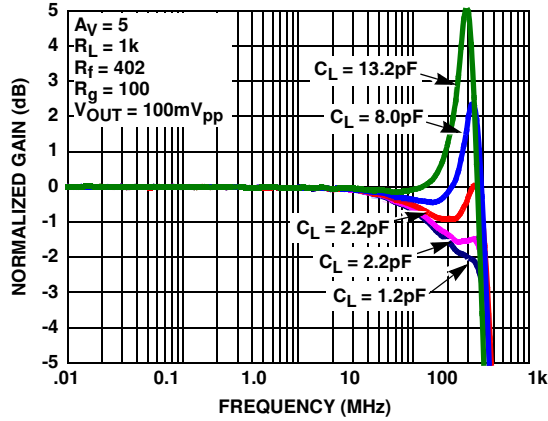
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## *Typical Performance Curves* (Continued)
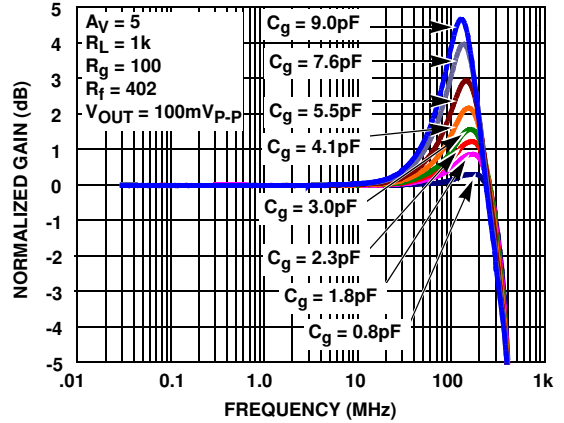


FIGURE 7. ISL55290 GAIN vs FREQUENCY vs C$_L$
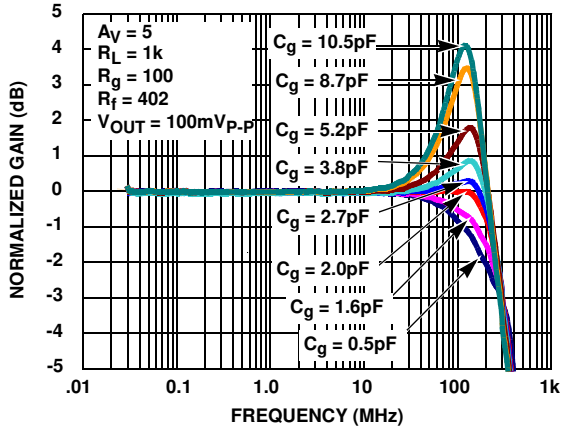


FIGURE 8. ISL55190 GAIN vs FREQUENCY vs C$_g$



FIGURE 9. ISL55290 GAIN vs FREQUENCY vs C$_g$
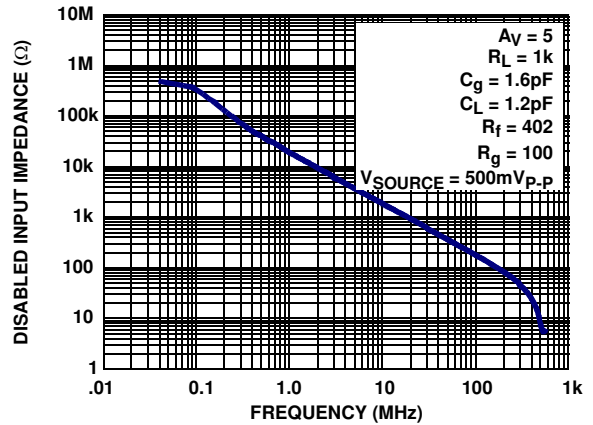


FIGURE 10. DISABLED INPUT IMPEDANCE vs FREQUENCY
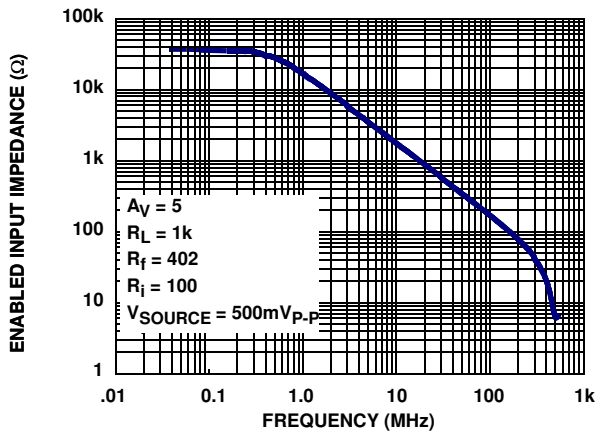


FIGURE 11. ENABLED INPUT IMPEDANCE vs FREQUENCY
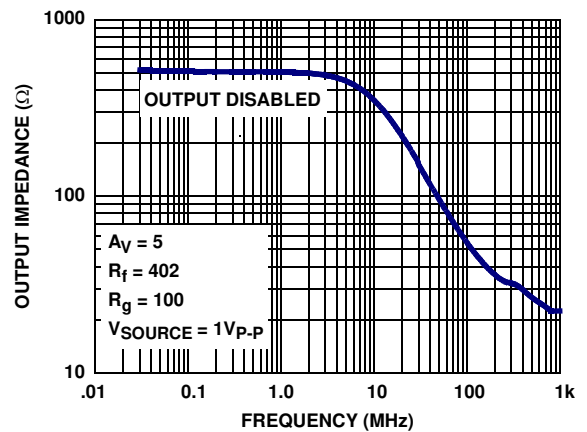


FIGURE 12. DISABLED OUTPUT IMPEDANCE vs FREQUENCY

## *Typical Performance Curves* (Continued)
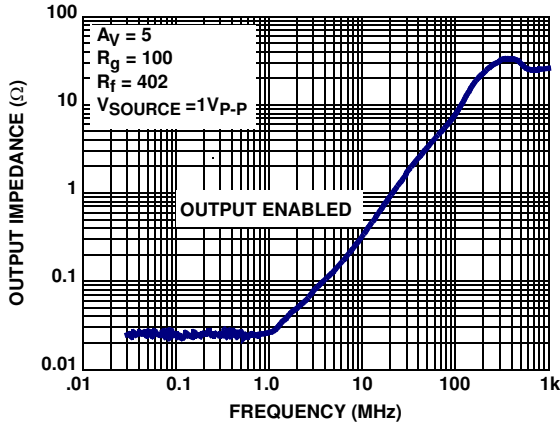


FIGURE 13.  ENABLED OUTPUT IMPEDANCE vs FREQUENCY
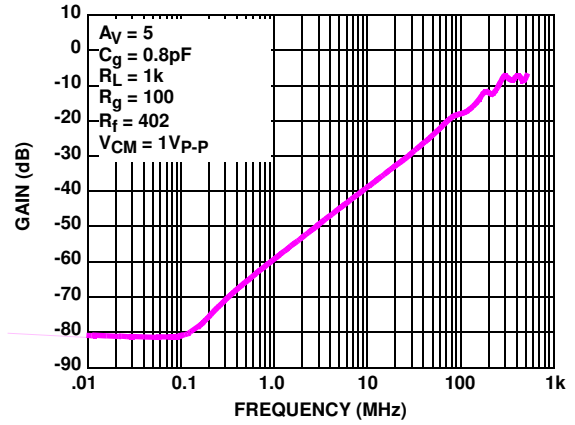


FIGURE 14.  CMRR vs FREQUENCY
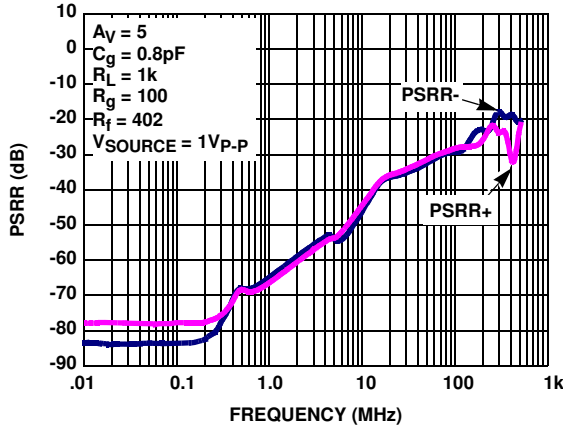


FIGURE 15.  PSRR vs FREQUENCY
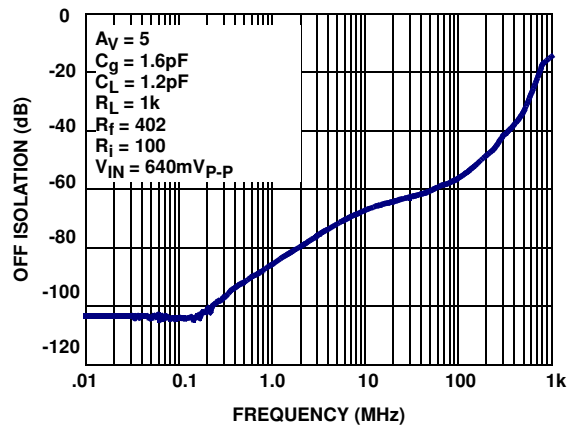


FIGURE 16.  OFF ISOLATION vs FREQUENCY
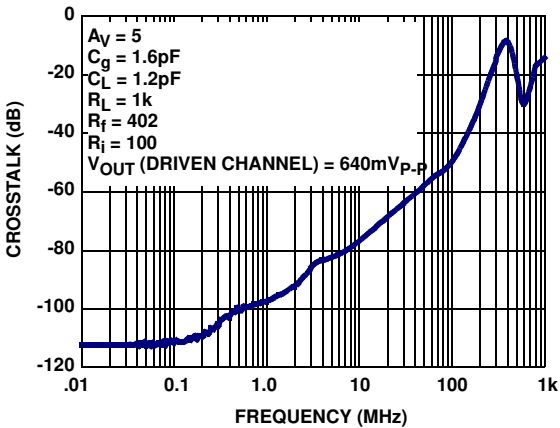


FIGURE 17.  ISL55290 CHANNEL TO CHANNEL CROSSTALK vs FREQUENCY
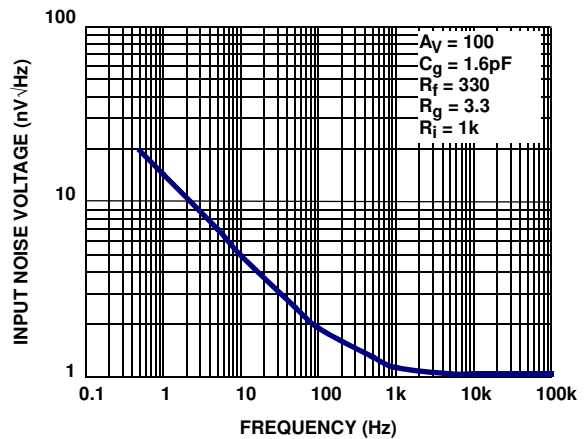


FIGURE 18.  INPUT VOLTAGE NOISE vs FREQUENCY

## *Typical Performance Curves* (Continued)
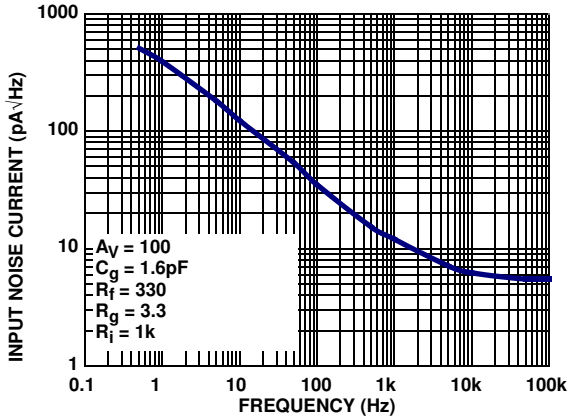


FIGURE 19. INPUT NOISE CURRENT vs FREQUENCY
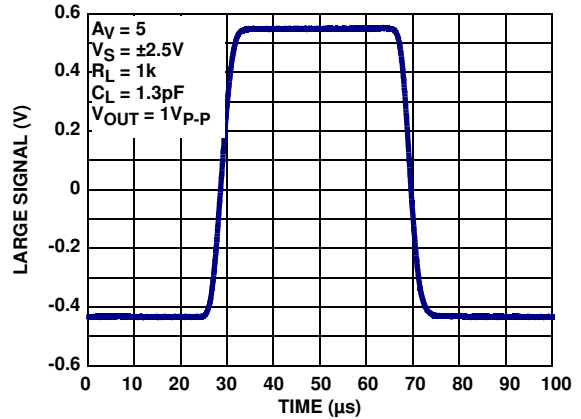


FIGURE 20. LARGE SIGNAL STEP RESPONSE
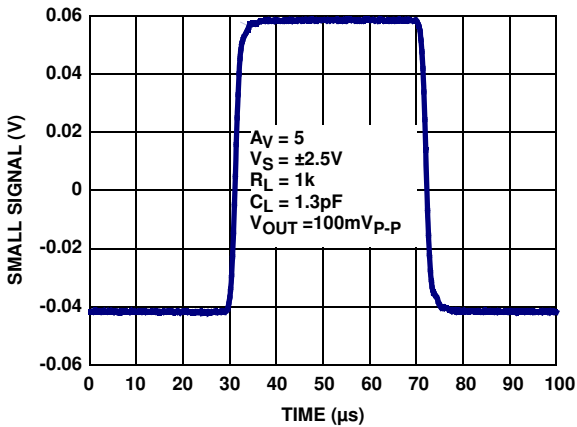


FIGURE 21. SMALL SIGNAL STEP RESPONSE
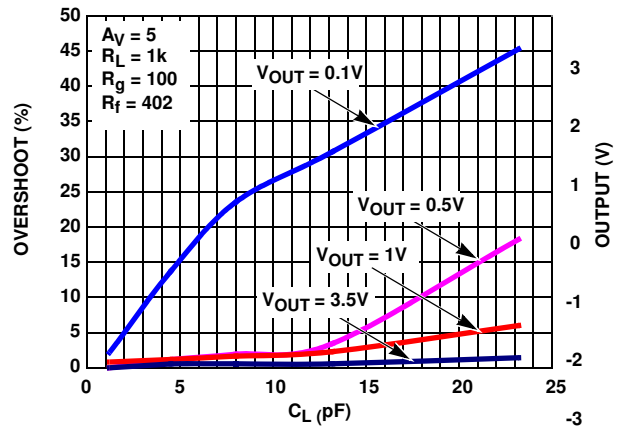


FIGURE 22. ISL55290 PERCENT OVERSHOOT vs V$_{OUT}$, C$_L$
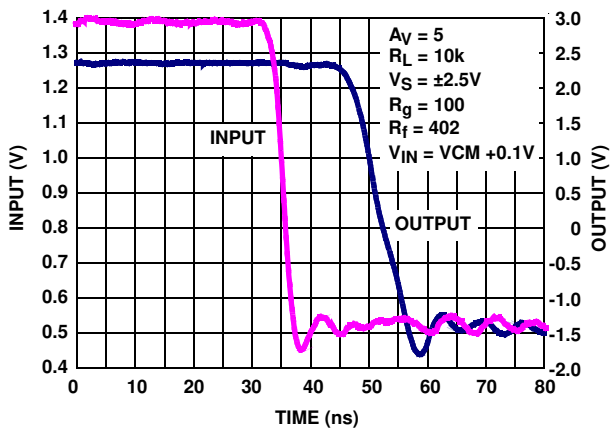


FIGURE 23. POSITIVE INPUT OVERLOAD RECOVERY TIME
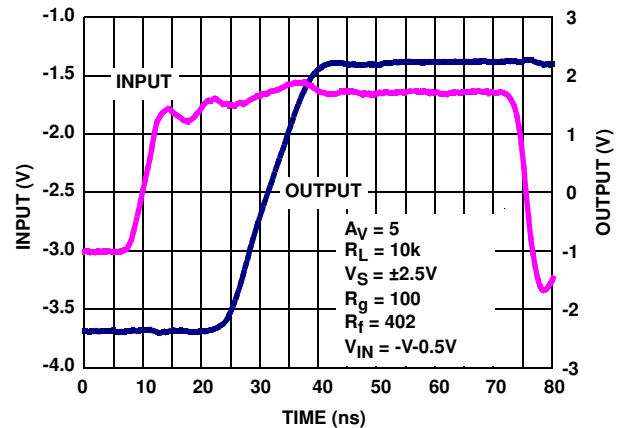


FIGURE 24. NEGATIVE INPUT OVERLOAD RECOVERY TIME

## *Typical Performance Curves* (Continued)
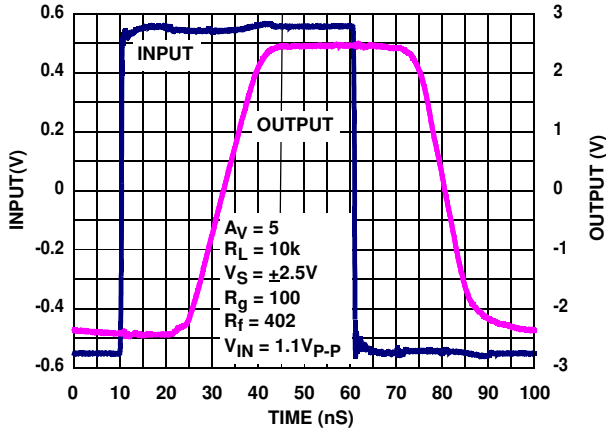


FIGURE 25. OUTPUT OVERLOAD RECOVERY TIME
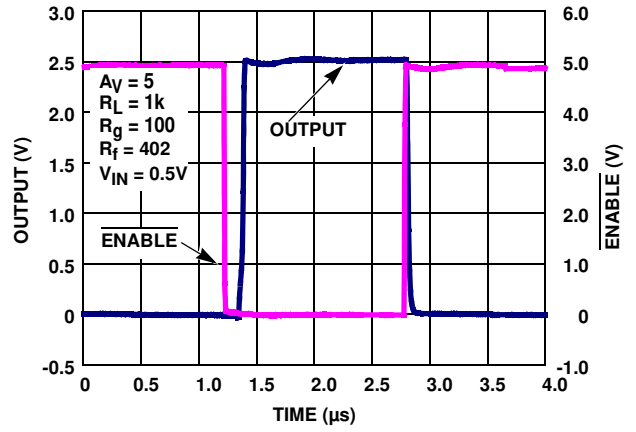


FIGURE 26. ISL55290 ENABLE TO OUTPUT DELAY
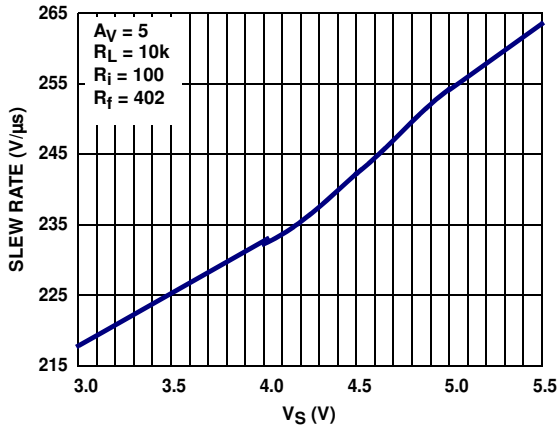


FIGURE 27. ISL55290 POSITIVE SLEW RATE vs VS
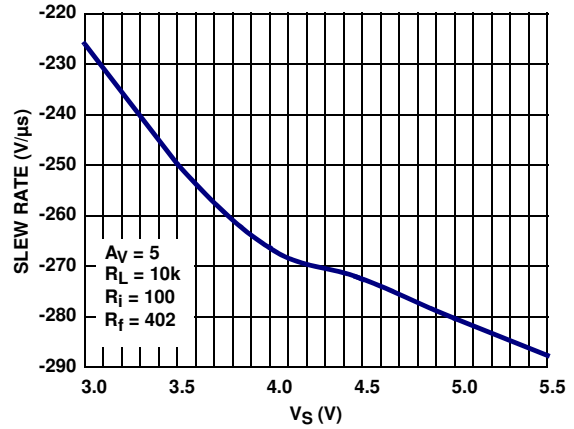


FIGURE 28. ISL55290 NEGATIVE SLEW RATE vs VS
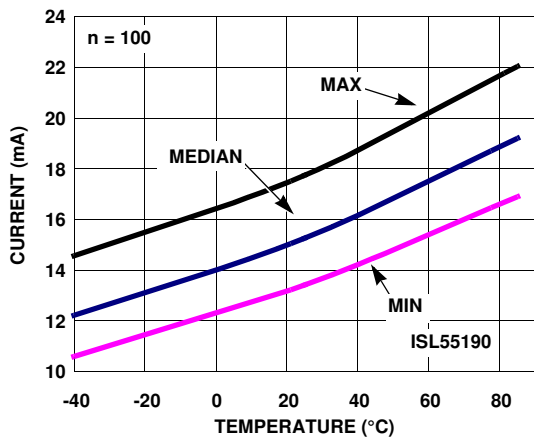


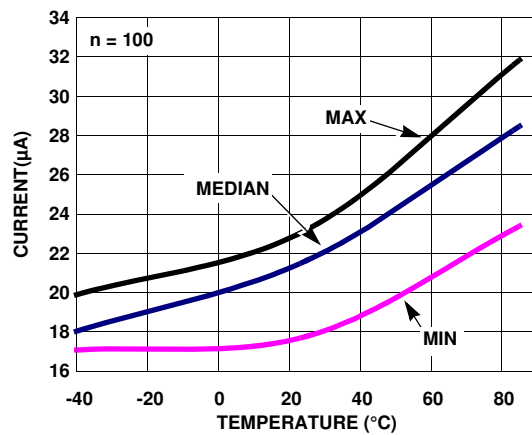FIGURE 29. SUPPLY CURRENT ENABLED vs TEMPERATURE
$V_S$ = ±2.5V



FIGURE 30. SUPPLY CURRENT DISABLED vs TEMPERATURE
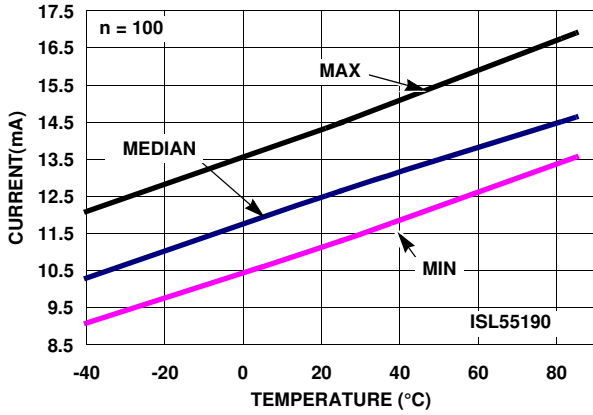$V_S$ = ±2.5V

## *Typical Performance Curves* (Continued)



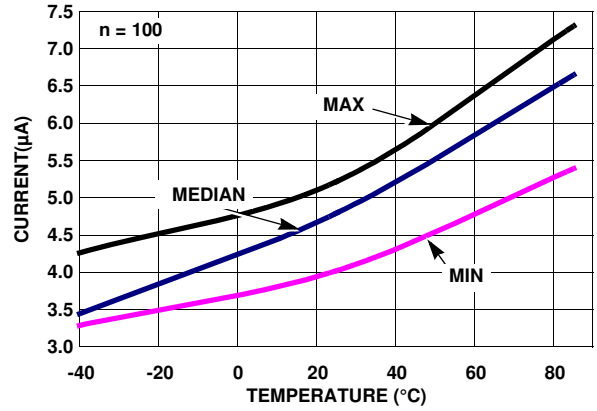FIGURE 31. SUPPLY CURRENT ENABLED vs TEMPERATURE $V_S = \pm 1.5V$



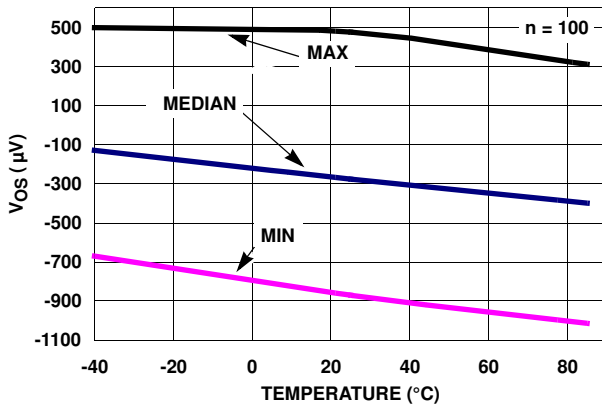FIGURE 32. SUPPLY CURRENT DISABLED vs TEMPERATURE $V_S = \pm 1.5V$



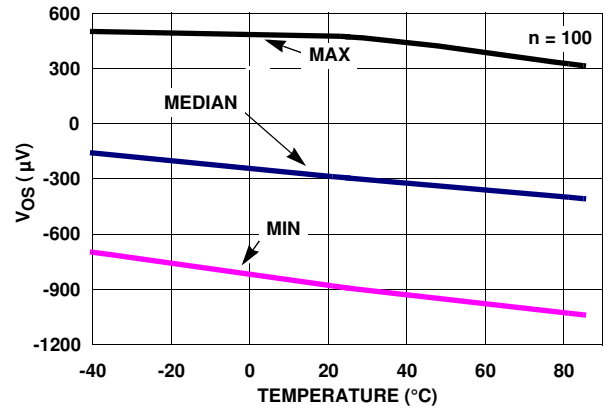FIGURE 33. $V_{IO}$ vs TEMPERATURE $V_S = \pm 2.5V$
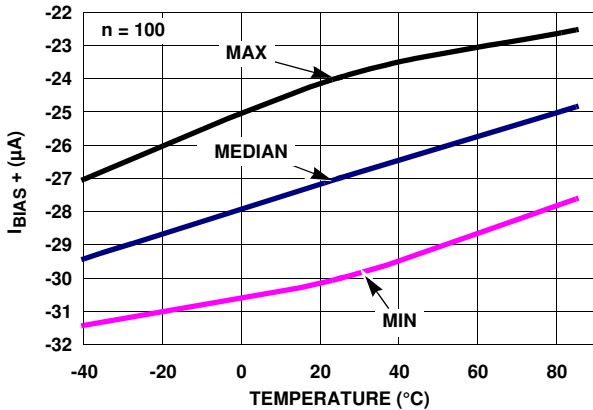


FIGURE 34. $V_{IO}$ vs TEMPERATURE $V_S = \pm 1.5V$



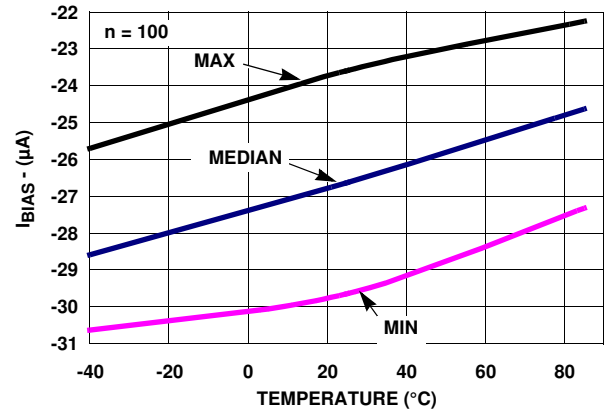FIGURE 35. $I_{BIAS+}$ vs TEMPERATURE $V_S = \pm 2.5V$



FIGURE 36. $I_{BIAS-}$ vs TEMPERATURE $V_S = \pm 2.5V$
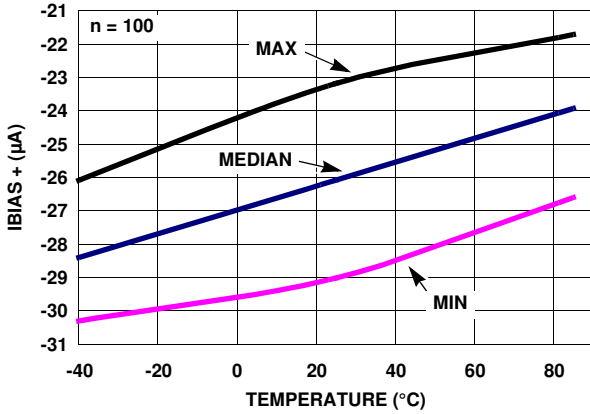
## *Typical Performance Curves* (Continued)



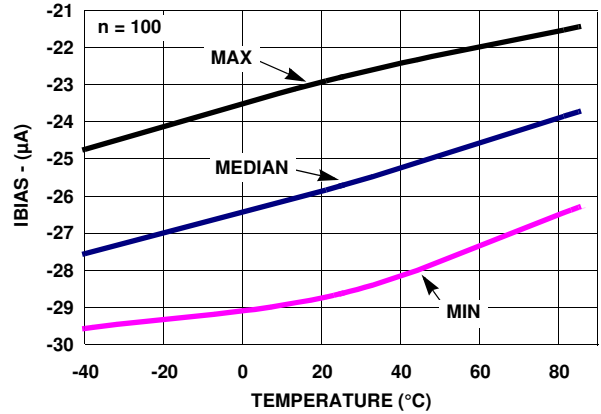**FIGURE 37.** $I_{BIAS+}$ vs TEMPERATURE $V_S = \pm1.5V$



**FIGURE 38.** $I_{BIAS-}$ vs TEMPERATURE $V_S = \pm1.5V$



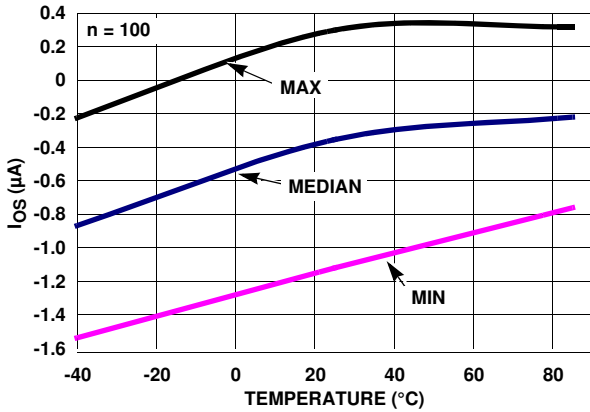**FIGURE 39.** $I_{OS}$ vs TEMPERATURE $V_S = \pm2.5V$
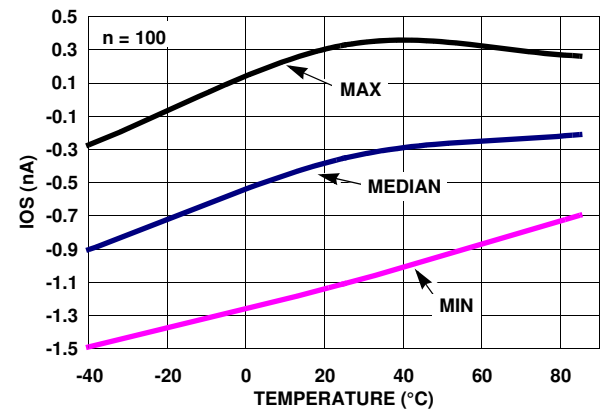


**FIGURE 40.** $I_{OS}$ vs TEMPERATURE $V_S = \pm1.5V$
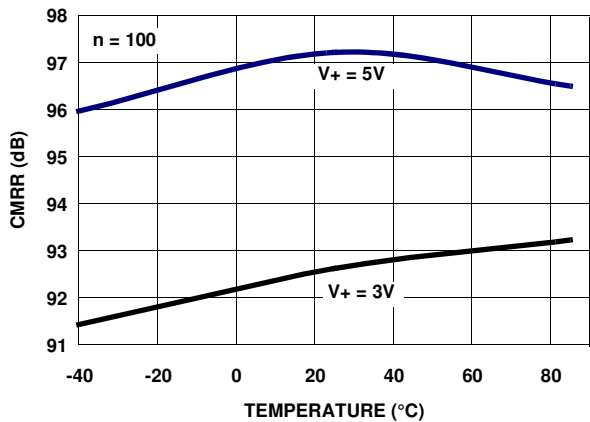


**FIGURE 41.** CMRR vs TEMPERATURE. V+ = ±2.5V, ±1.5V



**FIGURE 42.** PSRR vs TEMPERATURE ±1.5V to ±2.5V,
$V_S = \pm2.5V$

_intersil_

## *Typical Performance Curves* (Continued)



FIGURE 43.  $V_{OUT}$ HIGH vs TEMPERATURE $V_S$ = ±2.5V, $R_L$ = 1k



FIGURE 44.  $V_{OUT}$ LOW vs TEMPERATURE $V_S$ = ±2.5V, $R_L$ = 1k
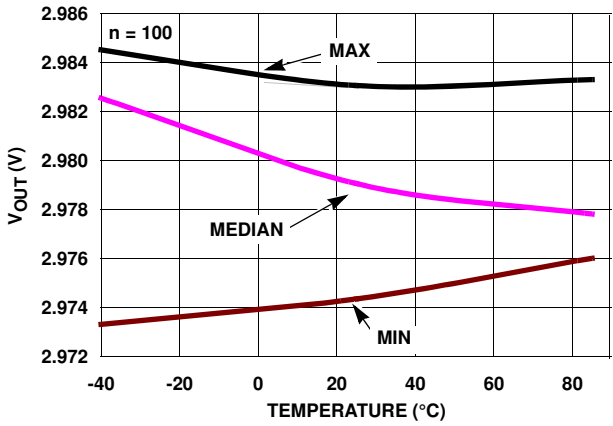


FIGURE 45.  $V_{OUT}$ HIGH vs TEMPERATURE $V_S$ = ±1.5V, $R_L$ = 1k
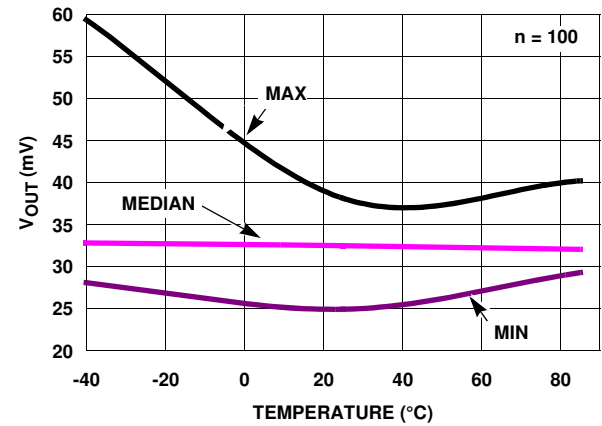


FIGURE 46.  $V_{OUT}$ LOW vs TEMPERATURE $V_S$ = ±1.5V, $R_L$ = 1k

## *Pin Descriptions*

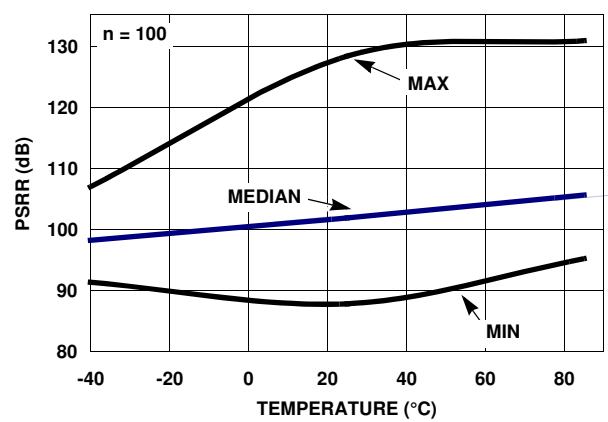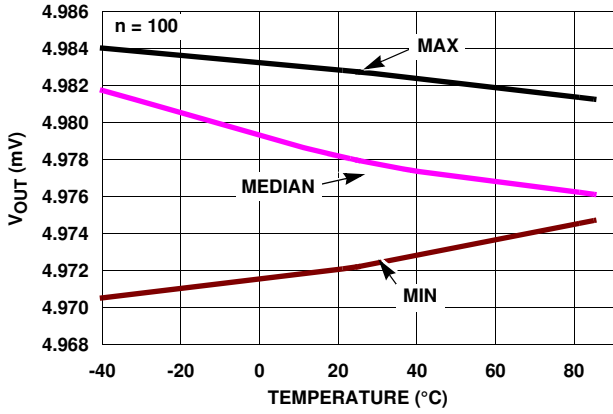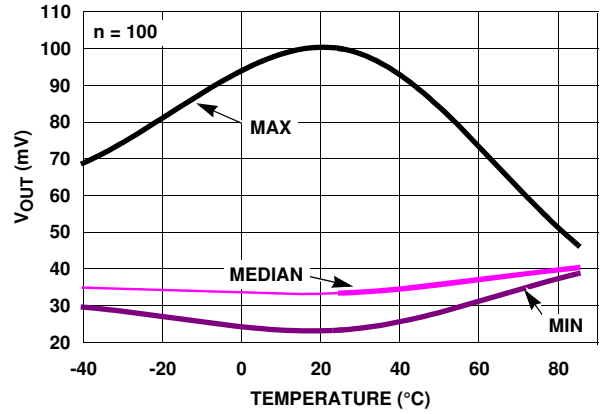| ISL55190 (8 Ld SOIC) | ISL55190 (8 Ld DFN) | ISL55290 (10 Ld MSOP) | PIN NAME | FUNCTION | EQUIVALENT CIRCUIT |
|---|---|---|---|---|---|
| 5 | 6 | | NC | Not connected | |
| 2 | 3 | 2 (A) 8 (B) | IN- | Inverting input | Circuit 1 |
| 3 | 4 | 3 (A) 7 (B) | IN+ | Non-inverting input | (See circuit 1) |
| 4 | 5 | 4 | V- | Negative supply | |
| 6 | 7 | 1 (A) 9 (B) | OUT | Output | Circuit 2 |
| 7 | 8 | 10 | V+ | Positive supply | |
| | | 5 (A) 6 (B) | $\overline{EN}$ | Enable pin with internal pull-down referenced to the -V pin; Logic "1" selects the disabled state; Logic "0" selects the enabled state. | Circuit 3a |
| 8 | 1 | | EN | Enable pin with internal pull-down referenced to the -V pin; Logic "0" (-V) selects the disabled state; Logic "1" (+V) selects the enabled state. | Circuit 3b |
| 1 | 2 | | FEEDBACK | Feedback pin to reduce IN- capacitance | Circuit 4 |

## *Applications Information*

### *Product Description*

The ISL55190 and ISL55290 are single and dual high speed, voltage feedback amplifiers designed for fast pulse applications, as well as communication and imaging systems that require very low voltage and current noise. Both devices are stable at a minimum gain of 5 and feature low distortion while drawing moderately low supply current. The ISL55190 and ISL55290 use a classical voltage-feedback topology, which allows them to be used in a variety of high speed applications where current-feedback amplifiers are not appropriate due to restrictions placed upon the feedback element used with the amplifier.

### *Enable/Power-Down*

Both devices can be operated from a single supply with a voltage range of +3V to +5V, or from split ±1.5V to ±2.5V. The logic level input to the ENABLE pins are TTL compatible and are referenced to the -V terminal in both single and split supply applications. The following discussion assumes single supply operation.

The ISL55190 uses a logic "0" (<0.8V) to disable the amplifier and the ISL55290 uses a logic "1" (>2V) to disable its amplifiers. In this condition, the output(s) will be in a high impedance state and the amplifier(s) current will be reduced to 21µA. The ISL55190 has an internal pull-up on the EN pin and is enabled by either floating or tying the EN pin to a voltage >2V. The ISL55290 has internal pull-downs on the $\overline{\text{EN}}$ pins and are enabled by either floating or tying the $\overline{\text{EN}}$ pins to a voltage <0.8V. The enable pins should be tied directly to their respective supply pins when not being used ($\overline{\text{EN}}$ tied to -V for the ISL55290 and EN tied to +V for the ISL55190).

### *Current Limiting*

The ISL55190 and ISL55290 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

### *Power Dissipation*

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature ($T_{JMAX}$) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times PD_{MAXTOTAL})$$

(EQ. 1)

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package ($PD_{MAX}$)

- $PD_{MAX}$ for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = 2^* V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L}$$

(EQ. 2)

where:

- $T_{MAX}$ = Maximum ambient temperature

- $\theta_{JA}$ = Thermal resistance of the package

- $PD_{MAX}$ = Maximum power dissipation of 1 amplifier

- $V_S$ = Supply voltage

- $I_{MAX}$ = Maximum supply current of 1 amplifier

- $V_{OUTMAX}$ = Maximum output voltage swing of the application

- $R_L$ = Load resistance

### *Power Supply Bypassing and Printed Circuit Board Layout*

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Low impedance ground plane construction is essential. Surface mount components are recommended, but if leaded components are used, lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with a 0.01µF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum, especially at the inverting input. When ground plane construction is used, it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of additional series inductance. Use of sockets (particularly for the SOIC package) should be avoided if possible. Sockets add parasitic inductance and capacitance which, will result in additional peaking and overshoot.

For inverting gains, this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains, this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large-value feedback and gain resistors exacerbates the problem by further lowering the pole frequency (increasing the possibility of oscillation).
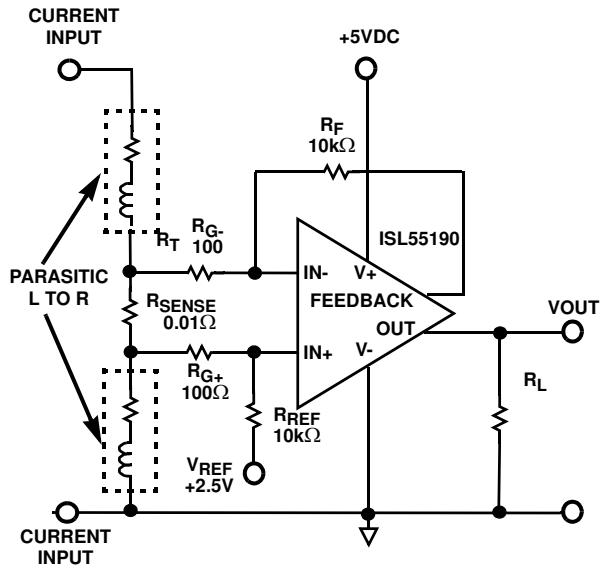
*intersil*

**FIGURE 47. GROUND SIDE CURRENT SENSE AMPLIFIER**

The ISL55190 single has a dedicated feedback pin which is internally connected to the amplifier output and located next to the inverting input pin. This additional output connection enables the PC board trace capacitance at the inverting pin to be minimized.

### *Current Sense Application Circuit*

The schematic in Figure 47 provides an example of utilizing the ISL55190 high speed performance with the ground sensing input capability to implement a single-supply, G =1 0 differential low side current sense amplifier. This circuit can be used to sense currents of either polarity. The reference voltage applied to $V_{REF}$ (+2.5V) defines the amplifier output 0A current sense reference voltage at one half the supply voltage level ($V_S$ = +5VDC), and $R_{SENSE}$ sets the current sense gain and full scale values. In this example the current gain is 10A/V over a maximum current range of slightly less than ±25A with $R_{SENSE}$ = 0.01Ω. The amplifier $V_{IO}$ error (-1.1mV max) and input bias offset current ($I_{IO}$) error (1.3μA) together contribute less than 15mV (150mA) at the output for better than 0.3% full scale accuracy.

The amplifier's high slew rate and fast pulse response make this circuit suitable for low-side current sensing in PWM and motor control applications. The excellent input overload recovery response enables the circuit to maintain performance in the presence of parasitic inductance that can cause fast rise and falling edge spikes that can momentarily overload the input stage of the amplifier.

## *Small Outline Package Family (SO)*
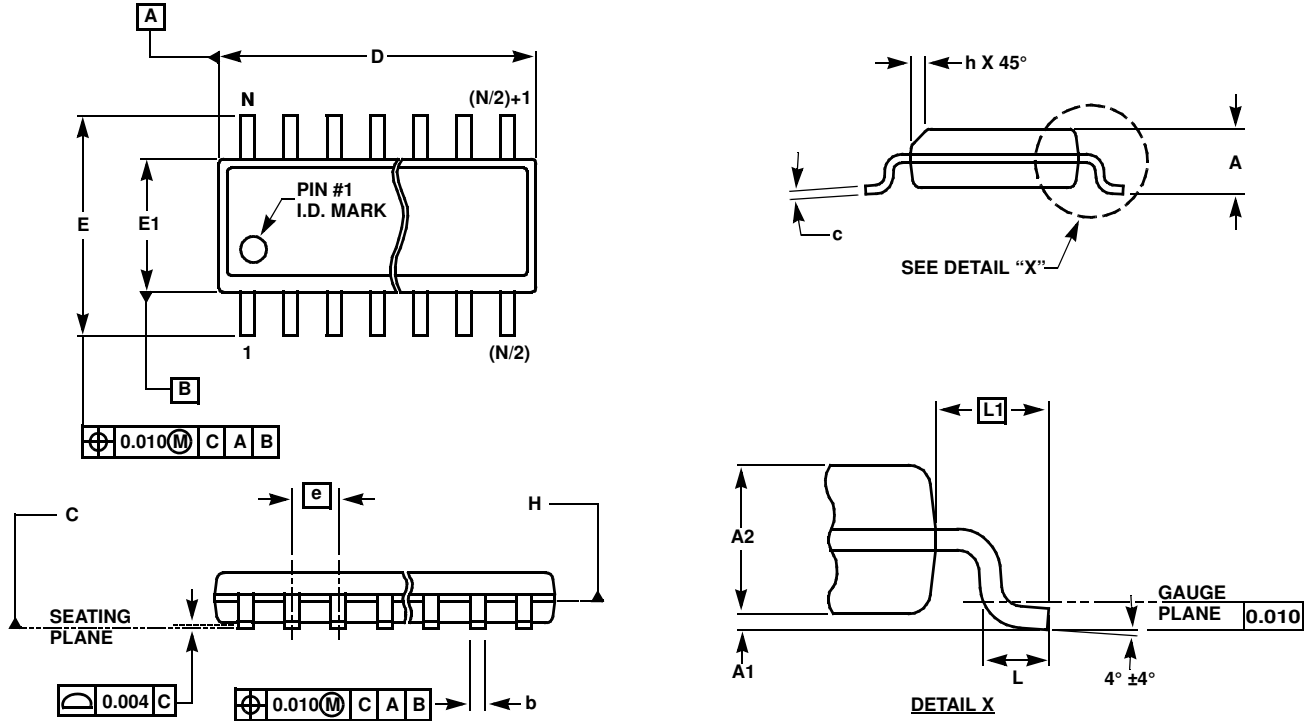


### MDP0027

**SMALL OUTLINE PACKAGE FAMILY (SO)**

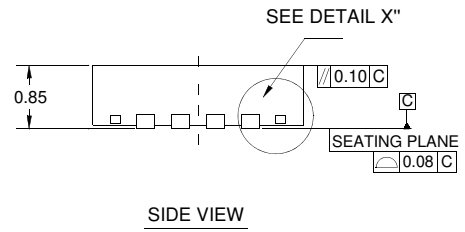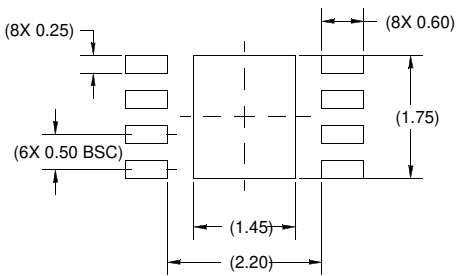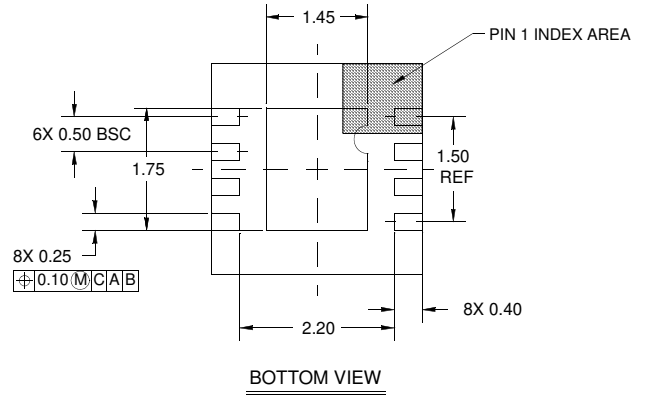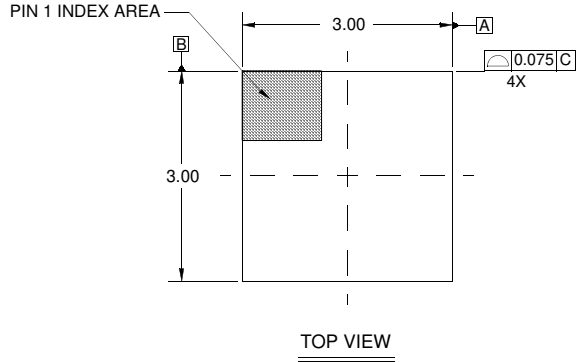| SYMBOL | INCHES | | | | | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | SO-8 | SO-14 | SO16 (0.150") | SO16 (0.300") (SOL-16) | SO20 (SOL-20) | SO24 (SOL-24) | SO28 (SOL-28) | | |
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | ±0.003 | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | ±0.002 | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | ±0.003 | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | ±0.004 | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.

2. Plastic interlead protrusions of 0.010" maximum per side are not included.

3. Dimensions "D" and "E1" are measured at Datum Plane "H".

4. Dimensioning and tolerancing per ASME Y14.5M-1994

# Package Outline Drawing

## L8.3x3D
**8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (DFN)**
**Rev 0, 9/06**

PIN 1 INDEX AREA

B

3.00

A

0.075 C
4X

3.00

TOP VIEW

1.45

PIN 1 INDEX AREA

6X 0.50 BSC

1.75

1.50
REF

8X 0.25

⊕ 0.10 Ⓜ C A B

2.20

8X 0.40

BOTTOM VIEW

(8X 0.25)

(8X 0.60)

(1.75)

(6X 0.50 BSC)

(1.45)

(2.20)

TYPICAL RECOMMENDED LAND PATTERN

SEE DETAIL X"

0.85

0.10 C

C

SEATING PLANE
0.08 C

SIDE VIEW

0.20 REF

5

C

0~0.05

DETAIL "X"
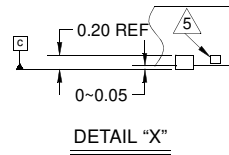
NOTES:
1. Controlling dimensions are in mm.
   Dimensions in ( ) for reference only.
2. Unless otherwise specified, tolerance : Decimal ±0.05
   Angular ±2°
3. Dimensioning and tolerancing conform to JEDEC STD MO220-D.
4. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
5. Tiebar shown (if present) is a non-functional feature.

## *Mini SO Package Family (MSOP)*
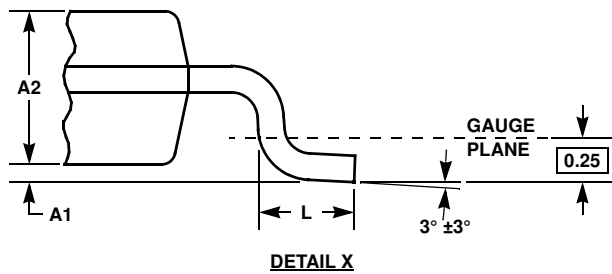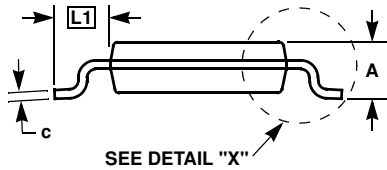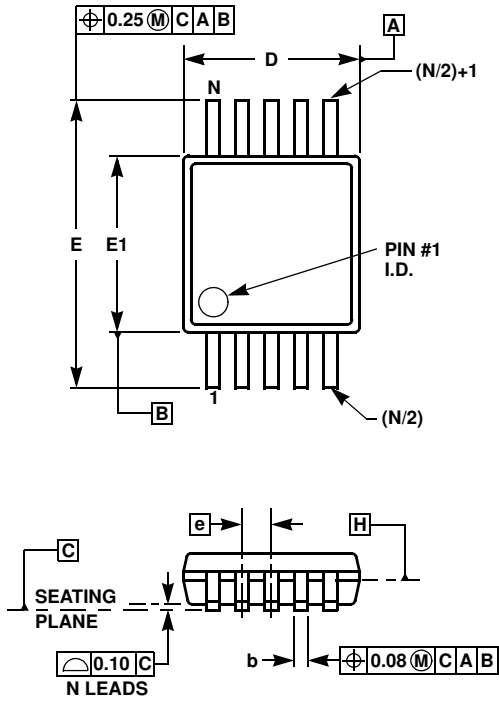


### MDP0043
**MINI SO PACKAGE FAMILY**

| SYMBOL | MILLIMETERS | | TOLERANCE | NOTES |
|--------|-------|--------|-----------|-------|
| | MSOP8 | MSOP10 | | |
| A | 1.10 | 1.10 | Max. | - |
| A1 | 0.10 | 0.10 | ±0.05 | - |
| A2 | 0.86 | 0.86 | ±0.09 | - |
| b | 0.33 | 0.23 | +0.07/-0.08 | - |
| c | 0.18 | 0.18 | ±0.05 | - |
| D | 3.00 | 3.00 | ±0.10 | 1, 3 |
| E | 4.90 | 4.90 | ±0.15 | - |
| E1 | 3.00 | 3.00 | ±0.10 | 2, 3 |
| e | 0.65 | 0.50 | Basic | - |
| L | 0.55 | 0.55 | ±0.15 | - |
| L1 | 0.95 | 0.95 | Basic | - |
| N | 8 | 10 | Reference | - |

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.

2. Plastic interlead protrusions of 0.25mm maximum per side are not included.

3. Dimensions "D" and "E1" are measured at Datum Plane "H".

4. Dimensioning and tolerancing per ASME Y14.5M-1994.