## Device Overview

The RC32332 device is a member of the IDT™ Interprise™ family of integrated communications processors. This product incorporates a high-performance, low-cost 32-bit CPU core with functionality common to a large number of embedded applications. The RC32332 integrates these functions to enable the use of low-cost PC commodity market memory and I/O devices, allowing the aggressive price/performance characteristics of the CPU to be realized quickly into low-cost systems.

The RC32332 device is available with either a 3.3V or 2.5V operating voltage. Differences between the two versions are noted where applicable.

## Features

- **RC32300 32-bit Microprocessor**
  - *Up to 150 MHz operation*
  - *Enhanced MIPS-II Instruction Set Architecture (ISA)*
  - *Cache prefetch instruction*
  - *Conditional move instruction*
  - *DSP instructions*
  - *Supports big or little endian operation*
  - *MMU with 32 page TLB*
  - *8KB Instruction Cache, 2-way set associative*
  - *2KB Data Cache, 2-way set associative*
  - *Cache locking per line*
  - *Programmable on a page basis to implement a write-through no write allocate, write-through write allocate, or write-back algorithms for cache management*
  - *Compatible with a wide variety of operating systems*
- **Local Bus Interface**
  - *Up to 75 MHz operation*
  - *23-bit address bus*
  - *32-bit data bus*
  - *Direct control of local memory and peripherals*
  - *Programmable system watch-dog timers*
  - *Big or little endian support*
- **Interrupt Controller simplifies exception management**
- **Four general purpose 32-bit timer/counters**
- **Programmable I/O (PIO)**
  - *Input/Output/Interrupt source*
  - *Individually programmable*
- **SDRAM Controller (32-bit memory only)**
  - *4 banks, non-interleaved*
  - *Up to 512MB total SDRAM memory supported*
  - *Implements full, direct control of discrete, SODIMM, or DIMM memories*
  - *Supports 16Mb through 512Mb SDRAM device depths*
  - *Automatic refresh generation*

## Block Diagram

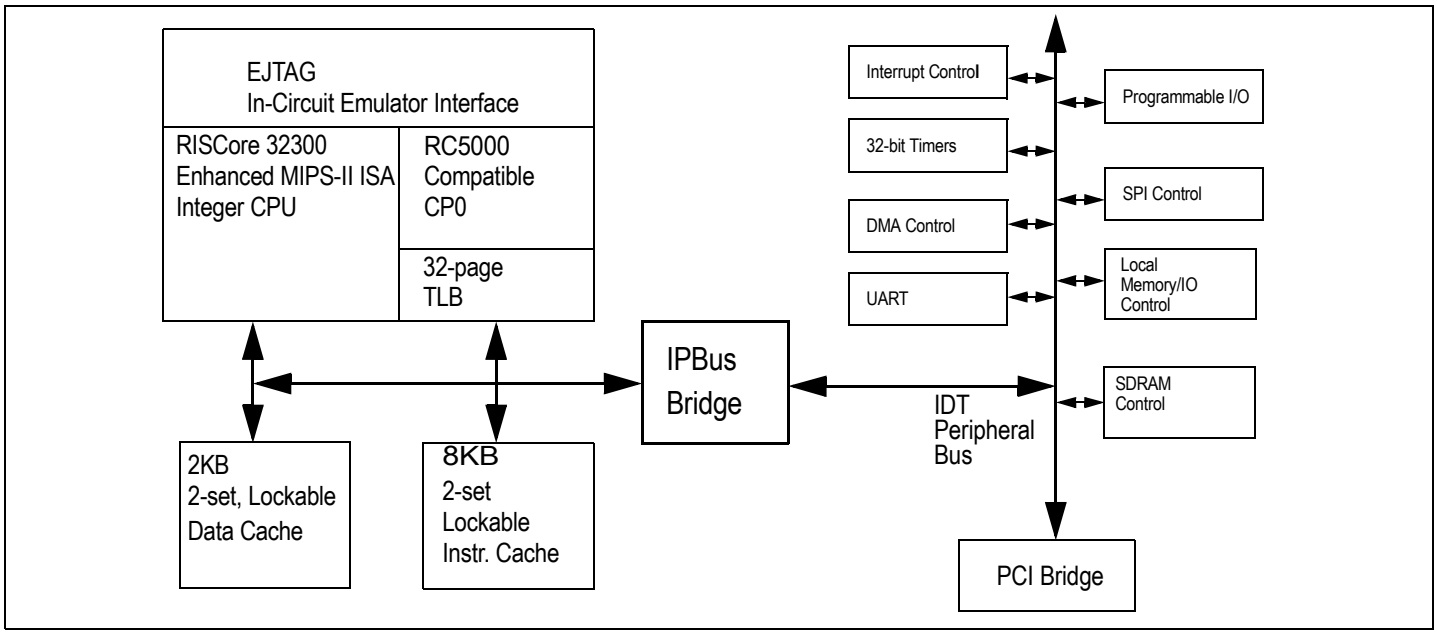



**Figure 1 RC32332 Block Diagram**

- **Serial Peripheral Interface (SPI) master mode interface**
- **UART Interface**
  - *16550 compatible UART*
  - *Baud rate support up to 1.5 Mb/s*
- **Memory & Peripheral Controller**
  - *6 banks, up to 8MB per bank*
  - *Supports 8-,16-, and 32-bit interfaces*
  - *Supports Flash ROM, SRAM, dual-port memory, and peripheral devices*
  - *Supports external wait-state generation*
  - *8-bit boot PROM support*
  - *Flexible I/O timing protocols*
- **4 DMA Channels**
  - *4 general purpose DMA, each with endianess swappers and byte lane data alignment*
  - *Supports scatter/gather, chaining via linked lists of records*
  - *Supports memory-to-memory, memory-to-I/O, memory-to-PCI, PCI-to-PCI, and I/O-to-I/O transfers*
  - *Supports unaligned transfers*
  - *Supports burst transfers*
  - *Programmable DMA bus transactions burst size (up to 16 bytes)*
- **PCI Bus Interface**
  - *32-bit PCI, up to 50 MHz*
  - *Revision 2.2 compatible*
  - *Target or master*
  - *Host or satellite*
  - *Two slot PCI arbiter*
  - *Serial EEPROM support, for loading configuration registers*
- **Off-the-shelf development tools**
- **JTAG Interface (IEEE Std. 1149.1 compatible)**
- **208 QFP Package**
- **3.3V or 2.5V core supply with 3.3V I/O supply**
  - *3.3V core supply is 5V I/O tolerant*
- **EJTAG in-circuit emulator interface**

## CPU Execution Core

The RC32332 integrates the RISCore 32300, the same CPU core found in the award-winning RC32364 microprocessor. The RISCore 32300 implements the Enhanced MIPS-II ISA. Thus, it is upwardly compatible with applications written for a wide variety of MIPS architecture processors, and it is kernel compatible with the modern operating systems that support IDT's 64-bit RISController product family. The RISCore 32300 was explicitly defined and designed for integrated processor products such as the RC32332. Key attributes of the execution core found within this product include:

- High-speed, 5-stage scalar pipeline executes to 150MHz. This high performance enables the RC32332 to perform a variety of performance intensive tasks, such as routing, DSP algorithms, etc.
- 32-bit architecture with enhancements of key capabilities. Thus, the RC32332 can execute existing 32-bit programs, while enabling designers to take advantage of recent advances in CPU architecture.
- Count leading-zeroes/ones. These instructions are common to a wide variety of tasks, including modem emulation, voice over IP compression and decompression, etc.
- Cache PREFetch instruction support, including a specialized form intended to help memory coherency. System programmers can allocate and stage the use of memory bandwidth to achieve maximum performance.
- 8KB of 2-way set associative instruction cache

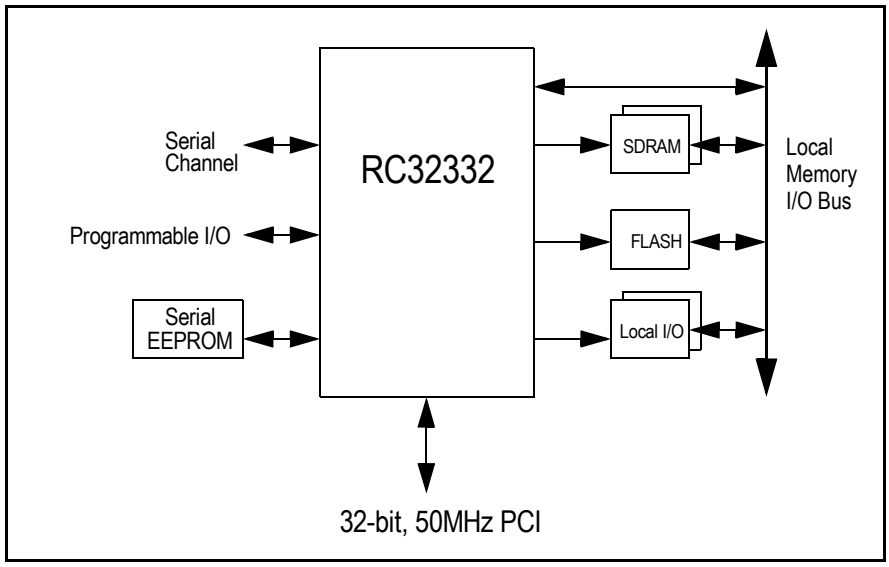



**Figure 2 RC32332 Based System Diagram**

- 2KB of 2-way set associative data cache, capable of write-back and write-through operation.
- Cache locking per line to speed real-time systems and critical system functions
- On-chip TLB to enable multi-tasking in modern operating systems
- EJTAG interface to enable sophisticated low-cost in-circuit emulation.

## Synchronous-DRAM Interface

The RC32332 integrates a SDRAM controller which provides direct control of system SyncDRAM running at speeds to 75MHz.

Key capabilities of the SDRAM controller include:

- Direct control of 4 banks of SDRAM (up to 2 64-bit wide DIMMs)
- On-chip page comparators optimize access latency.
- Speeds to 75MHz
- Programmable address map.
- Supports 16, 64, 128, 256, or 512Mb SDRAM devices
- Automatic refresh generation driven by on-chip timer
- Support for discrete devices, SODIMM, or DIMM modules.

Thus, systems can take advantage of the full range of commodity memory that is available, enabling system optimization for cost, real-estate, or other attributes.

## Local Memory and I/O Controller

The local memory and I/O controller implements direct control of external memory devices, including the boot ROM as well as other memory areas, and also implements direct control of external peripherals.

The local memory controller is highly flexible, allowing a wide range of devices to be directly controlled by the RC32332 processor. For example, a system can be built using an 8-bit boot ROM, 16-bit FLASH cards (possibly on PCMCIA), a 32-bit SRAM or dual-port memory, and a variety of low-cost peripherals.

Key capabilities include:

- Direct control of EPROM, FLASH, RAM, and dual-port memories
- 6 chip-select outputs, supporting up to 8MB per memory space
- Supports mixture of 8-, 16-, and 32-bit wide memory regions
- Flexible timing protocols allow direct control of a wide variety of devices
- Programmable address map for 2 chip selects
- Automatic wait state generation.

## PCI Bus Bridge

In order to leverage the wide availability of low-cost peripherals for the PC market as well as to simplify the design of add-in functions, the RC32332 integrates a full 32-bit PCI bus bridge. Key attributes of this bridge include:

- 50 MHz operation
- PCI revision 2.2 compliant
- Programmable address mappings between CPU/Local memory and PCI memory and I/O
- On-chip PCI arbiter
- Extensive buffering allows PCI to operate concurrently with local memory transfers
- Selectable byte-ordering swapper.

## On-Chip DMA Controller

To minimize CPU exception handling and maximize the efficiency of system bandwidth, the RC32332 integrates a very sophisticated 4-channel DMA controller on chip.

The RC32332 DMA controller is capable of:

- Chaining and scatter/gather support through the use of a flexible, linked list of DMA transaction descriptors
- Capable of memory<->memory, memory<->I/O, and PCI<->memory DMA
- Unaligned transfer support
- Byte, halfword, word, quadword DMA support.

## On-Chip Peripherals

The RC32332 also integrates peripherals that are common to a wide variety of embedded systems.

- Single 16550 compatible UART.
- SPI master mode interface for direct interface to EEPROM, A/D, etc.
- Interrupt Controller to speed interrupt decode and management
- Four 32-bit on-chip Timer/Counters
- Programmable I/O module

## Debug Support

To facilitate rapid time to market, the RC32332 provides extensive support for system debug.

First and foremost, this product integrates an EJTAG in-circuit emulation module, allowing a low-cost emulator to interoperate with programs executing on the controller. By using an augmented JTAG interface, the RC32332 is able to reuse the same low-cost emulators developed around the RC32364 CPU.

Secondly, the RC32332 implements additional reporting signals intended to simplify the task of system debugging when using a logic analyzer. This product allows the logic analyzer to differentiate transactions initiated by DMA from those initiated by the CPU and further allows CPU transactions to be sorted into instruction fetches vs. data fetches.

Finally, the RC32332 implements a full boundary scan capability, allowing board manufacturing diagnostics and debug.

## Packaging

The RC32332 is packaged using a 208 Quad Flat Pack (QFP) package.

## Thermal Considerations

The RC32332 consumes less than 2.0 W peak power. The device is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices; -40° to +85° C for industrial temperature devices.

## Revision History

**November 15, 2000:** Initial publication.

**December 12, 2000:** Changed Max values for cpu_masterclock period in Table 5 and added footnote. In Table 1, added 2nd alternate function for spi_mosi, spi_miso, spi_sck. In Table 11, added "2" in Alt column for pins 186, 187, 188. In RC32332 Alternate Signal Functions table, added pin names in Alt #2 column for pins 186, 187, 188.

**January 4, 2001**: In Table 6 under Interrupt Handling, changed Tdoh9 to Thld13 and moved the values for Tsu9 from the Max to the Min column.

**February 23, 2001**: In Table 1, changed alternate function for uart_tx[0] from PIO[3] to PIO[1]. In Table 11, changed the number of alternate pins for Pin 156 from 1 to 2. In Table 12, added PIO[7] to Alt #2 column for Pin 156 and changed PIO[3] to PIO[1] for Pin 207.

**March 13, 2001**: Changed upper ambient temperature for industrial and commercial uses from +70° C to +85° C.

**June 7, 2001**: In the Clock Parameters table, added footnote 3 to output_clk category and added NA to Min and Max columns. In Figure 3 (Reset Specification), enhanced signal line for cpu_masterclk. In Local System Interface section of AC Timing Characteristics table, changed values in Min column for last category of signals (Tdoh3) from 1.5 to 2.5 for both speeds. In SDRAM Controller section of same table, changed values in Min column for last category of signals (9 signals) from 1 to 2.5 for both speeds.

**September 14, 2001**: In the Reset category of Table 6: switched mem_addr[19:17] from Tsu22 and Thld22 to Tsu10 and Thld10; switched mem_addr[22:20] from Tsu10 and Thld10 to Tsu22 and Thld22; moved ejtag_pcst[2:0] from Reset to Debug Interface category under Tsu20 and Thld20.

**November 1, 2001**: Added Input Voltage Undershoot parameter and 2 footnotes to Table 10. Changed to DH package.

**May 2, 2002**: Changed from PCI 2.1 to 2.2 compliant. Added 512 MB SDRAM support. Changed upper ambient temperature for commercial uses back from +85° C to +70° C (changed erroneously from 70 to 85 on March 13, 2001). Added Reset State Status column to Table 1. Revised description of jtag_trst_n in Table 1 and changed this pin to a pull-down instead of a pull-up.

**July 3, 2002**: This data sheet now describes revision Y silicon and is no longer applicable to revision Z.

**July 12, 2002**: Added 150MHz speed grade. In Table 6: DMA section, changed Thld9 Min values from 2 to 1; in PIO section, changed Thld9 Min values from 2 to 1. Changed revision Y data sheet from Preliminary to Final.

**September 18, 2002**: Added cpu_coldreset_n rise time to Table 5, Clock Parameters. Added mem_addr[16] and sdram_addr[16] to Tables 1 and 12. Changed Logic Diagram to include sdram_addr[16].

**December 18, 2002**: In the Reset section of Table 6, AC Timing Characteristics, setup and hold time categories for cpu_coldreset_n have been deleted.

**September 2, 2003**: Added 2.5V version of device. Changed tables to include 2.5V values where appropriate. Added a Power Consumption table, Temperature and Voltage table, and Power Curves for the 2.5V device. In the PCI category of Table 6, created separate sections for 3.3V and 2.5V devices and in 2.5V section changed time to 4 ns for pci_cbe_n[3:0], pci_frame_n, pci_trdy_n, and pci_irdy_n. In Table 8, added 3 new categories (Input Pads, PCI Input Pads, and All Pads) and added footnotes 2 and 3. In Table 13, pins 181 and 184 were changed from Vcc Core to Vcc I/O.

**March 24, 2004**: In Table 1, changed description in Satellite Mode for pci_rst_n. Specified "cold" reset on pages 12 and 13. Changed several values in Table 12, Absolute Maximum Ratings, and changed footnote 1 to that table.

**May 4, 2004**: Revised values in Table 9, Power Consumption.

# Pin Description Table

The following table lists the pins provided on the RC32332. Note that those pin names followed by "_n" are active-low signals. All external pull-ups and pull-downs require 10 kΩ resistor.

| Name | Type | Reset State Status | Drive Strength Capability | Description |
|---|---|---|---|---|
| **Local System Interface** | | | | |
| mem_data[31:0] | I/O | Z | High | **Local system data bus**<br>Primary data bus for memory. I/O and SDRAM. |
| mem_addr[22:2] | I/O | [22:10] Z<br>[9:2] L | [22:17] Low<br>[16:2] High | **Memory Address Bus**<br>These signals provide the Memory or DRAM address, during a Memory or DRAM bus transaction. During each word data, the address increments either in linear or sub-block ordering, depending on the transaction type. The table below indicates how the memory write enable signals are used to address discreet memory port width types.<br>**Port Width** / **Pin Signals mem_we_n[3]** / **mem_we_n[2]** / **mem_we_n[1]** / **mem_we_n[0]**<br>DMA (32-bit): mem_we_n[3] / mem_we_n[2] / mem_we_n[1] / mem_we_n[0]<br>32-bit: mem_we_n[3] / mem_we_n[2] / mem_we_n[1] / mem_we_n[0]<br>16-bit: Byte High Write Enable / mem_addr[1] / Not Used (Driven Low) / Byte Low Write Enable<br>8-bit: Not Used (Driven High) / mem_addr[1] / mem_addr[0] / Byte Write Enable<br>mem_addr[22] Alternate function: reset_boot_mode[1].<br>mem_addr[21] Alternate function: reset_boot_mode[0].<br>mem_addr[20] Alternate function: reset_pci_host_mode.<br>mem_addr[19] Alternate function: modebit [9].<br>mem_addr[18] Alternate function: modebit [8].<br>mem_addr[17] Alternate function: modebit [7].<br>mem_addr[16] Alternate function: sdram_addr[16].<br>mem_addr[15] Alternate function: sdram_addr[15].<br>mem_addr[14] Alternate function: sdram_addr[14].<br>mem_addr[13] Alternate function: sdram_addr[13].<br>mem_addr[11] Alternate function: sdram_addr[11].<br>mem_addr[10] Alternate function: sdram_addr[10].<br>mem_addr[9] Alternate function: sdram_addr[9].<br>mem_addr[8] Alternate function: sdram_addr[8].<br>mem_addr[7] Alternate function: sdram_addr[7].<br>mem_addr[6] Alternate function: sdram_addr[6].<br>mem_addr[5] Alternate function: sdram_addr[5].<br>mem_addr[4] Alternate function: sdram_addr[4].<br>mem_addr[3] Alternate function: sdram_addr[3].<br>mem_addr[2] Alternate function: sdram_addr[2]. |
| mem_cs_n[5:0] | Output | H | Low | **Memory Chip Select Negated** Recommend an external pull-up.<br>Signals that a Memory Bank is actively selected. |
| mem_oe_n | Output | H | High | **Memory Output Enable Negated** Recommend an external pull-up.<br>Signals that a Memory Bank can output its data lines onto the cpu_ad bus. |
| mem_we_n[3:0] | Output | H | High | **Memory Write Enable Negated Bus**<br>Signals which bytes are to be written during a memory transaction. Bits act as Byte Enable and mem_addr[1:0] signals for 8-bit or 16-bit wide addressing. |

**Table 1 Pin Descriptions (Part 1 of 6)**

| Name | Type | Reset State Status | Drive Strength Capability | Description |
|---|---|---|---|---|
| mem_wait_n | Input | | — | **Memory Wait Negated** Requires an external pull-up.<br>SRAM/IOI/IOM modes: Allows external wait-states to be injected during the last cycle before data is sampled.<br>DPM (dual-port) mode: Allows dual-port busy signal to restart memory transaction.<br>Alternate function: sdram_wait_n. |
| mem_245_oe_n | Output | H | Low | **Memory FCT245 Output Enable Negated**<br>Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to a memory or I/O bank. |
| mem_245_dt_r_n | Output | Z | High | **Memory FCT245 Direction Xmit/Rcv Negated** Recommend an external pull-up.<br>Alternate function: cpu_dt_r_n. See CPU Core Specific Signals below. |
| output_clk | Output | cpu_masterclk | High | **Output Clock**<br>Optional clock output. |
| **PCI Interface** | | | | |
| pci_ad[31:0] | I/O | Z | PCI | **PCI Multiplexed Address/Data Bus**<br>Address driven by Bus Master during initial frame_n assertion, and then the Data is driven by the Bus Master during writes; or the Data is driven by the Bus Slave during reads. |
| pci_cbe_n[3:0] | I/O | Z | PCI | **PCI Multiplexed Command/Byte Enable Bus**<br>Command (not negated) Bus driven by the Bus Master during the initial frame_n assertion. Byte Enable Negated Bus driven by the Bus Master during the data phase(s). |
| pci_par | I/O | Z | PCI | **PCI Parity**<br>Even parity of the pci_ad[31:0] bus. Driven by Bus Master during Address and Write Data phases. Driven by the Bus Slave during the Read Data phase. |
| pci_frame_n | I/O | Z | PCI | **PCI Frame Negated**<br>Driven by the Bus Master. Assertion indicates the beginning of a bus transaction. De-assertion indicates the last datum. |
| pci_trdy_n | I/O | Z | PCI | **PCI Target Ready Negated**<br>Driven by the Bus Slave to indicate the current datum can complete. |
| pci_irdy_n | I/O | Z | PCI | **PCI Initiator Ready Negated**<br>Driven by the Bus Master to indicate that the current datum can complete. |
| pci_stop_n | I/O | Z | PCI | **PCI Stop Negated**<br>Driven by the Bus Slave to terminate the current bus transaction. |
| pci_idsel_n | Input | | — | **PCI Initialization Device Select**<br>Uses pci_req_n[2] pin. See the PCI subsection. |
| pci_perr_n | I/O | Z | PCI | **PCI Parity Error Negated**<br>Driven by the receiving Bus Agent 2 clocks after the data is received, if a parity error occurs. |
| pci_serr_n | I/O Open-collector | Z | PCI | **System Error** Requires an external pull-up.<br>Driven by any agent to indicate an address parity error, data parity during a Special Cycle command, or any other system error. |
| pci_clk | Input | | — | **PCI Clock**<br>Clock for PCI Bus transactions. Uses the rising edge for all timing references. |
| pci_rst_n | Input | L | — | **PCI Reset Negated**<br>Host mode: Resets all PCI related logic.<br>Satellite mode: Resets all PCI related logic and also warm resets the 32332. |
| pci_devsel_n | I/O | Z | PCI | **PCI Device Select Negated**<br>Driven by the target to indicate that the target has decoded the present address as a target address. |

**Table 1 Pin Descriptions (Part 2 of 6)**

| Name | Type | Reset State Status | Drive Strength Capability | Description |
|---|---|---|---|---|
| pci_req_n[2] | Input | Z | — | **PCI Bus Request #2 Negated** Requires an external pull-up.<br>Host mode: pci_req_n[2] is an input indicating a request from an external device.<br>Satellite mode: used as pci_idsel pin which selects this device during a configuration read or write.<br>Alternate function: pci_idsel (satellite). |
| pci_req_n[0] | I/O | Z | High | **PCI Bus Request #0 Negated** Requires an external pull-up for burst mode.<br>Host mode: pci_req_n[0] is an input indicating a request from an external device.<br>Satellite mode: pci_req_n[0] is an output indicating a request from this device. |
| pci_gnt_n[2] | Output | Z[1] | High | **PCI Bus Grant #2 Negated** Recommend an external pull-up.<br>Host mode: pci_gnt_n[2] is an output indicating a grant to an external device.<br>Satellite mode: pci_gnt_n[2] is used as the pci_inta_n output pin. External pull-up is required.<br>Alternate function: pci_inta_n (satellite). |
| pci_gnt_n[1] (can only be used as alternate function) | I/O | X for 1 pci clock then H[2] | High | **PCI Bus Grant #1 Negated** Recommend external pull-up.<br>Host mode: not used as pci_gnt_n[1]. Must be used as alternate function PIO[7].<br>Satellite mode: Not used as pci_gnt_n[1]. Used as pci_eprom_cs output pin for Serial Chip Select for loading PCI Configuration Registers in the RC32332 Reset Initialization Vector PCI boot mode. Defaults to the output direction at reset time.<br>1st Alternate function: pci_eeprom_cs (satellite).<br>2nd Alternate function: PIO[7]. |
| pci_gnt_n[0] | I/O | Z | High | **PCI Bus Grant #0 Negated**<br>Host mode: pci_gnt_n[0] is an output indicating a grant to an external device. Recommend external pull-up.<br>Satellite mode: pci_gnt_n[0] is an input indicating a grant to this device. Requires external pull-up. |
| pci_inta_n | Output Open-collector | Z | PCI | **PCI Interrupt #A Negated**<br>Uses pci_gnt_n[2]. See the PCI subsection. |
| pci_lock_n | Input | | — | **PCI Lock Negated**<br>Driven by the Bus Master to indicate that an exclusive operation is occurring. |

[1] Z in host mode; L in satellite non-boot mode; Z in satellite boot mode.
[2] H in host mode, L in satellite non-boot and boot modes. X = unknown.

**SDRAM Control Interface**

| | | | | |
|---|---|---|---|---|
| sdram_addr_12 | Output | L | High | **SDRAM Address Bit 12 and Precharge All**<br>SDRAM mode: Provides SDRAM address bit 12 (10 on the SDRAM chip) during row address and "pre-charge all" signal during refresh, read and write command. |
| sdram_ras_n | Output | H | High | **SDRAM RAS Negated**<br>SDRAM mode: Provides SDRAM RAS control signal to all SDRAM banks. |
| sdram_cas_n | Output | H | High | **SDRAM CAS Negated**<br>SDRAM mode: Provides SDRAM CAS control signal to all SDRAM banks. |
| sdram_we_n | Output | H | High | **SDRAM WE Negated**<br>SDRAM mode: Provides SDRAM WE control signal to all SDRAM banks. |
| sdram_cke | Output | H | High | **SDRAM Clock Enable**<br>SDRAM mode: Provides clock enable to all SDRAM banks. |
| sdram_cs_n[3:0] | Output | H | High | **SDRAM Chip Select Negated Bus** Recommend an external pull-up.<br>SDRAM mode: Provides chip select to each SDRAM bank.<br>SODIMM mode: Provides upper select byte enables [7:4]. |
| sdram_s_n[1:0] | Output | H | High | **SDRAM SODIMM Select Negated Bus**<br>SDRAM mode: Not used.<br>SDRAM SODIMM mode: Upper and lower chip selects. |

**Table 1 Pin Descriptions (Part 3 of 6)**

| Name | Type | Reset State Status | Drive Strength Capability | Description |
|---|---|---|---|---|
| sdram_bemask_n [3:0] | Output | H | High | **SDRAM Byte Enable Mask Negated Bus (DQM)**<br>SDRAM mode: Provides byte enables for each byte lane of all DRAM banks.<br>SODIMM mode: Provides lower select byte enables [3:0]. |
| sdram_245_oe_n | Output | H | Low | **SDRAM FCT245 Output Enable Negated** Recommend an external pull-up.<br>SDRAM mode: Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank. |
| sdram_245_dt_r_n | Output | Z | High | **SDRAM FCT245 Direction Transmit/Receive** Recommend an external pull-up.<br>Uses cpu_dt_r_n. See CPU Core Specific Signals below. |
| **On-Chip Peripherals** | | | | |
| dma_ready_n[0] | I/O | Z | Low | **DMA Ready Negated Bus** Requires an external pull-up.<br>Ready mode: Input pin for general purpose DMA channel 0 that can initiate the next datum in the current DMA descriptor frame.<br>Done mode: Input pin for general purpose DMA channel 0 that can terminate the current DMA descriptor frame.<br>dma_ready_n[0] 1st Alternate function PIO[0]; 2nd Alternate function: dma_done_n[0]. |
| pio[7:0] | I/O | See related pins | Low | **Programmable Input/Output**<br>General purpose pins that can each can be configured as a general purpose input or general purpose output. These pins are multiplexed with other pin functions:<br>pci_gnt_n[1] (pci_eeprom_cs), spi_mosi, spi_sck, spi_ss_n, spi_miso, uart_rx[0], uart_tx[0], dma_ready_n[0]. Note that pci_gnt_n[1], spi_mosi, spi_sck, and spi_ss_n default to outputs at reset time. The others default to inputs. |
| uart_rx[0] | I/O | Z | Low | **UART Receive Data Bus**<br>UART mode: UART channel receive data.<br>uart_rx[0] Alternate function: PIO[2]. |
| uart_tx[0] | I/O | Z | Low | **UART Transmit Data Bus** Recommend an external pull-up.<br>UART mode: UART channel send data. Note that this pin defaults to an input at reset time and must be programmed via the PIO interface before being used as a UART output.<br>uart_tx[0] Alternate function: PIO[1]. |
| spi_mosi | I/O | L | Low | **SPI Data Output**<br>Serial mode: Output pin from RC32332 as an Input to a Serial Chip for the Serial data input stream.<br>In PCI satellite mode, acts as an Output pin from RC32332 that connects as an Input to a Serial Chip for the Serial data input stream for loading PCI Configuration Registers in the RC32332 Reset Initialization Vector PCI boot mode.<br>1st Alternate function: PIO[6]. Defaults to the output direction at reset time.<br>2nd Alternate function: pci_eeprom_mdo. |
| spi_miso | I/O | Z | Low | **SPI Data Input**<br>Serial mode: Input pin to RC32332 from the Output of a Serial Chip for the Serial data output stream.<br>In PCI satellite mode, acts as an Input pin from RC32332 that connects as an output to a Serial Chip for the Serial data output stream for loading PCI Configuration Registers in the RC32332 Reset Initialization Vector PCI boot mode. Defaults to input direction at reset time.<br>1st Alternate function: PIO[3].<br>2nd Alternate function: pci_eeprom_mdi. |
| spi_sck | I/O | L | Low | **SPI Clock**<br>Serial mode: Output pin for Serial Clock.<br>In PCI satellite mode, acts as an Output pin for Serial Clock for loading PCI Configuration Registers in the RC323332 Reset Initialization Vector PCI boot mode.<br>1st Alternate function: PIO[5]. Defaults to the output direction at reset time.<br>2nd Alternate function: pci_eeprom_sk. |

**Table 1 Pin Descriptions (Part 4 of 6)**

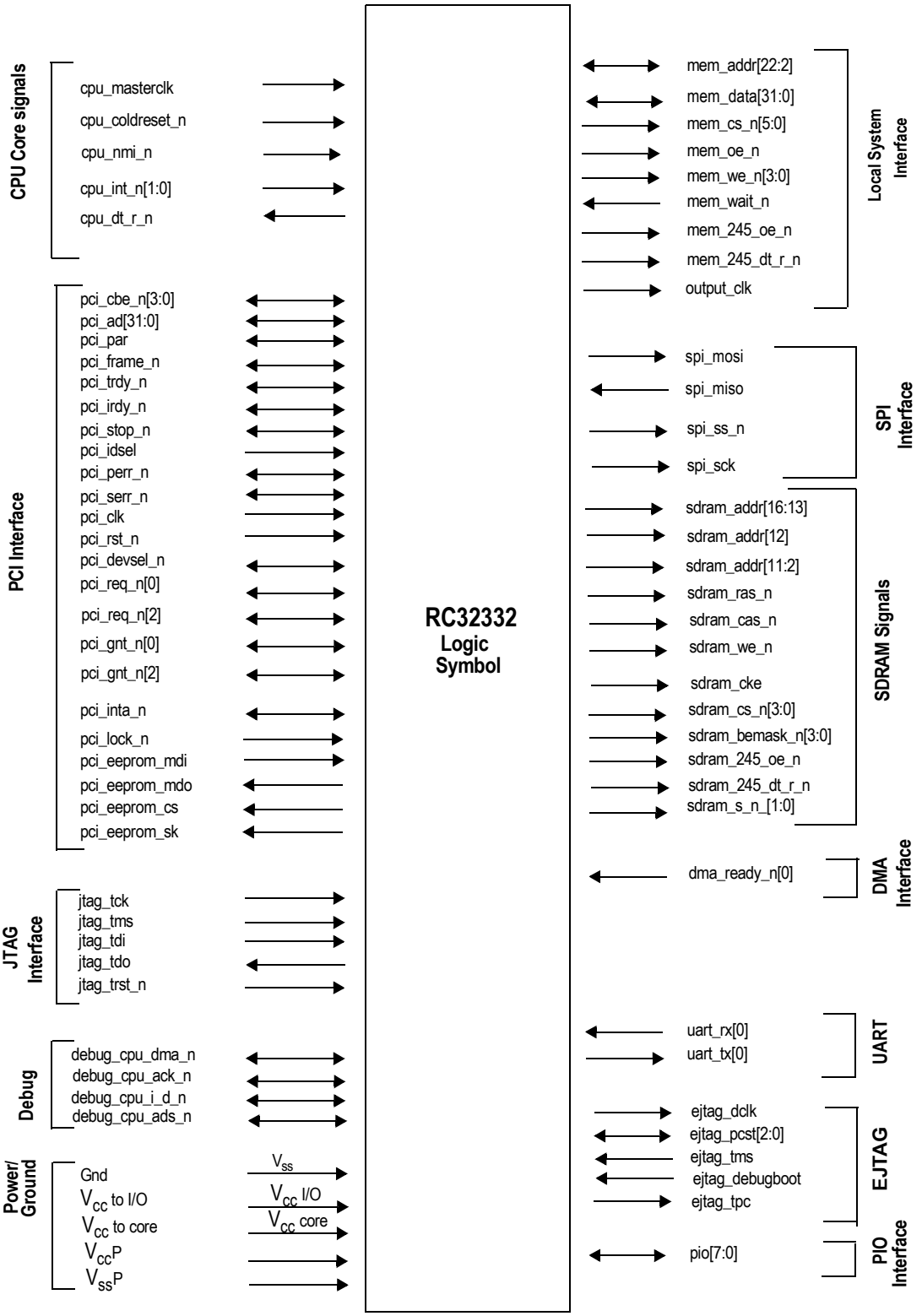
| Name | Type | Reset State Status | Drive Strength Capability | Description |
|---|---|---|---|---|
| spi_ss_n | I/O | H | Low | **SPI Chip Select**<br>Output pin selecting the serial protocol device as opposed to the PCI satellite mode EEPROM device.<br>Alternate function: PIO[4]. Defaults to the output direction at reset time. |
| **CPU Core Specific Signals** | | | | |
| cpu_nmi_n | Input | | — | **CPU Non-Maskable Interrupt** Requires an external pull-up.<br>This interrupt input is active low to the CPU. |
| cpu_masterclk | Input | | — | **CPU Master System Clock**<br>Provides the basic system clock. |
| cpu_int_n[1:0] | Input | | — | **CPU Interrupt** Requires an external pull-up.<br>These interrupt inputs are active low to the CPU. |
| cpu_coldreset_n | Input | L | — | **CPU Cold Reset**<br>This active-low signal is asserted to the RC32332 after $V_{cc}$ becomes valid on the initial power-up. The Reset initialization vectors for the RC32332 are latched by cold reset. |
| cpu_dt_r_n | Output | Z | — | **CPU Direction Transmit/Receive**<br>This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during read operations.<br>1st Alternate function: mem_245_dt_r_n.<br>2nd Alternate function: sdram_245_dt_r_n. |
| **JTAG Interface Signals** | | | | |
| jtag_tck | Input | | — | **JTAG Test Clock** Requires an external pull-down.<br>An input test clock used to shift into or out of the Boundary-Scan register cells. jtag_tck is independent of the system and the processor clock with nominal 50% duty cycle. |
| jtag_tdi,<br>ejtag_dint_n | Input | | — | **JTAG Test Data In** Requires an external pull-up.<br>On the rising edge of jtag_tck, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG). This pin is also used as the ejtag_dint_n signal in the EJTAG mode. |
| jtag_tdo,<br>ejtag_tpc | Output | Z | High | **JTAG Test Data Out**<br>The jtag_tdo is serial data shifted out from instruction or data register on the falling edge of jtag_tck. When no data is shifted out, the jtag_tdo is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock. This pin is also used as the ejtag_tpc signal in the EJTAG mode. |
| jtag_tms | Input | | — | **JTAG Test Mode Select** Requires an external pull-up.<br>The logic signal received at the jtag_tms input is decoded by the TAP controller to control test operation. jtag_tms is sampled on the rising edge of the jtag_tck. |
| jtag_trst_n | Input | L | — | **JTAG Test Reset**<br>When neither JTAG nor EJTAG are being used, jtag_trst_n must be driven low (pulled down) or the jtag_tms/ejtag_tms signals must be pulled up and jtag_clk actively clocked. |
| ejtag_dclk | Output | Z | — | **EJTAG Test Clock**<br>Processor Clock. During Real Time Mode, this signal is used to capture address and data from the ejtag_tpc signal at the processor clock speed or any division of the internal pipeline. |

**Table 1 Pin Descriptions (Part 5 of 6)**

| Name | Type | Reset State Status | Drive Strength Capability | Description |
|---|---|---|---|---|
| ejtag_pcst[2:0] | I/O | Z | Low | **EJTAG PC Trace Status Information**<br>111 (STL) Pipe line Stall<br>110 (JMP) Branch/Jump forms with PC output<br>101 (BRT) Branch/Jump forms with no PC output<br>100 (EXP) Exception generated with an exception vector code output<br>011 (SEQ) Sequential performance<br>010 (TST) Trace is outputted at pipeline stall time<br>001 (TSQ) Trace trigger output at performance time<br>000 (DBM) Run Debug Mode<br>Alternate function: modebit[2:0]. |
| ejtag_debugboot | Input | | — | **EJTAG DebugBoot** Requires an external pull-down.<br>The ejtag_debugboot input is used during reset and forces the CPU core to take a debug exception at the end of the reset sequence instead of a reset exception. This enables the CPU to boot from the ICE probe without having the external memory working. This input signal is level sensitive and is not latched internally. This signal will also set the JtagBrk bit in the JTAG_Control_Register[12]. |
| ejtag_tms | Input | | — | **EJTAG Test Mode Select** Requires an external pull-up.<br>The ejtag_tms is sampled on the rising edge of jtag_tck. |
| **Debug Signals** | | | | |
| debug_cpu_dma_n | I/O | Z | Low | **Debug CPU versus DMA Negated**<br>De-assertion high during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from the CPU.<br>Assertion low during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from DMA.<br>Alternate function: modebit[6]. |
| debug_cpu_ack_n | I/O | Z | Low | **Debug CPU Acknowledge Negated**<br>Indicates either a data acknowledge to the CPU or DMA.<br>Alternate function: modebit[4]. |
| debug_cpu_ads_n | I/O | Z | Low | **Debug CPU Address/Data Strobe Negated**<br>Assertion indicates that either a CPU or a DMA transaction is beginning and that the mem_data[31:4] bus has the current block address.<br>Alternate function: modebit[5]. |
| debug_cpu_i_d_n | I/O | Z | Low | **Debug CPU Instruction versus Data Negated**<br>Assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU or DMA data transaction.<br>De-assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU instruction transaction.<br>Alternate function: modebit[3]. |

**Table 1 Pin Descriptions (Part 6 of 6)**

# Logic Diagram — RC32332



# Mode Bit Settings to Configure Controller on Reset

The following table lists the mode bit settings to configure the controller on cold reset.

| Pin | Mode Bit | Description | Value | Mode Setting |
|---|---|---|---|---|
| ejtag_pcst[2:0] | 2:0 MSB (2) | Clock Multiplier<br>**MasterClock** is multiplied internally to generate PClock | 0 | Multiply by 2 |
| | | | 1 | Multiply by 3 |
| | | | 2 | Multiply by 4 |
| | | | 3 | Reserved |
| | | | 4 | Reserved |
| | | | 5 | Reserved |
| | | | 6 | Reserved |
| | | | 7 | Reserved |
| debug_cpu_i_d_n | 3 | EndBit | 0 | Little-endian ordering |
| | | | 1 | Big-endian ordering |
| debug_cpu_ack_n | 4 | Reserved | 0 | |
| debug_cpu_ads_n | 5 | Reserved | 0 | |
| debug_cpu_dma_n | 6 | TmrIntEn<br>Enables/Disables the timer interrupt on Int*[5] | 0 | Enables timer interrupt |
| | | | 1 | Disables timer interrupt |
| mem_addr[17] | 7 | Reserved for future use | 1 | |
| mem_addr[19:18] | 9:8 MSB (9) | Boot-Prom Width specifies the memory port width of the memory space which contains the boot prom. | 00 | 8 bits |
| | | | 01 | 16 bits |
| | | | 10 | 32 bits |
| | | | 11 | Reserved |

**Table 2 Boot-Mode Configuration Settings**

## reset_boot_mode Settings

By using the non-boot mode cold reset initialization mode the user can change the internal register addresses from base 1800_0000 to base 1900_0000, as required. The RC32332 cold reset-boot mode initialization setting values and mode descriptions are listed below.

| Pin | Reset Boot Mode | Description | Value | Mode Settings |
|---|---|---|---|---|
| mem_addr[22:21] | 1:0 MSB (1) | Tri-state memory bus and EEPROM bus during coldreset_n assertion | 11 | Tri-state_bus_mode |
| | | Reserved | 10 | |
| | | **PCI-boot mode** (pci_host_mode must be in satellite mode) RC32332 will reset either from a cold reset or from a PCI reset. Boot code is provided via PCI. | 01 | PCI_boot_mode |
| | | **Standard-boot mode** Boot from the RC32332's memory controller (typical system). | 00 | standard_boot_mode |

**Table 3 RC32332 reset_boot_mode Initialization Settings**

### pci_host_mode Settings

During cold reset initialization, the RC32332's PCI interface can be set to the Satellite or Host mode settings. When set to the Host mode, the CPU must configure the RC32332's PCI configuration registers, including the read-only registers. If the RC32332's PCI is in the PCI-boot mode Satellite mode, read-only configuration registers are loaded by the serial EEPROM.

| Pin | Reset Boot Mode | Description | Value | Mode Settings |
|---|---|---|---|---|
| mem_addr[20] | PCI host mode | PCI is in satellite mode | 1 | PCI_satellite |
| | | PCI is in host mode (typical system) | 0 | PCI_host |

**Table 4 RC32332 pci_host_mode Initialization Settings**

## Clock Parameters — RC32332

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: $V_{cc}$ Core = +3.3V±5%; $V_{cc}$ I/O = +3.3V±5%

2.5V version: $V_{cc}$ Core = +2.5V±5%; $V_{cc}$ I/O = +3.3V±5%

| Parameter | Symbol | Test Conditions | RC32332 100MHz | | RC32332 133MHz | | RC32332 150MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| cpu_masterclock HIGH | $t_{MCHIGH}$ | Transition ≤ 2ns | 8 | — | 6.75 | — | 6 | — | ns |
| cpu_masterclock LOW | $t_{MCLOW}$ | Transition ≤ 2ns | 8 | — | 6.75 | — | 6 | — | ns |
| cpu_masterclock period[1] - 3.3V ver. | $t_{MCP}$ | — | 20 | 66.6 | 15 | 66.6 | 13.33 | 66.6 | ns |
| cpu_masterclock period[1] - 2.5V ver. | $t_{MCP}$ | — | 20 | 40.0 | 15 | 40.0 | 13.33 | 40.0 | ns |
| cpu_masterclock Rise & Fall Time[2] | $t_{MCRise}$, $t_{MCFall}$ | — | — | 3 | — | 3 | — | 3 | ns |
| cpu_masterclock Jitter | $t_{JITTER}$ | — | — | ± 250 | — | ± 250 | — | ± 200 | ps |
| pci_clk Rise & Fall Time | $t_{PCRise}$, $t_{PCFall}$ | PCI 2.2 | — | 1.6 | — | 1.6 | — | 1.6 | ns |
| pci_clk Period[1] | $t_{PCP}$ | | 20 | — | 20 | — | 20 | — | ns |
| jtag_tck Rise & Fall Time | $t_{JCRise}$, $t_{JCFall}$ | — | — | 5 | — | 5 | — | 5 | ns |
| ejtag_dck period | $t_{DCK}$, $t_{11}$ | | 10 | — | 10 | — | 10 | — | ns |
| jtag_tck clock period | $t_{TCK}$, $t_3$ | | 100 | — | 100 | — | 100 | — | ns |
| ejtag_dclk High, Low Time | $t_{DCK\ High}$, $t_9$<br>$t_{DCK\ Low}$, $t_{10}$ | | 4 | — | 4 | — | 4 | — | ns |
| ejtag_dclk Rise, Fall Time | $t_{DCK\ Rise}$, $t_9$<br>$t_{DCK\ Fall}$, $t_{10}$ | | — | 1 | — | 1 | — | 1 | ns |
| output_clk[3] | $t_{DO}$21 | | N/A | N/A | N/A | N/A | N/A | N/A | — |
| cpu_coldreset_n<br>Asserted during power-up | | power-on sequence | 120 | — | 120 | — | 120 | — | ms |
| cpu_coldreset_n Rise Time | $t_{CRRise}$ | | — | 5 | — | 5 | — | 5 | ns |

**Table 5 Clock Parameters - RC32332**

1. cpu_masterclock frequency should never be below pci_clk frequency if PCI interface is used.

2. Rise and Fall times are measured between 10% and 90%.

3. Output_clk should not be used in a system. Only the cpu_masterclock or its derivative must be used to drive all the subsystems with designs based on the RC32334/RC32332. Refer to the RC32334/RC32332 Device Errata for more information.

## Reset Specification

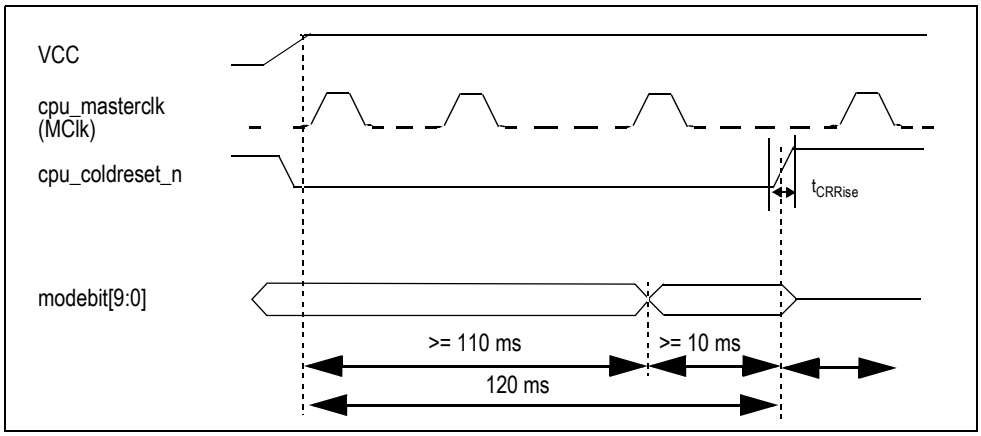



**Figure 3 Mode Configuration Interface Cold Reset Sequence**

## AC Timing Characteristics — RC32332

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: $V_{cc}$ Core = +3.3V±5%; $V_{cc}$ I/O = +3.3V±5%

2.5V version: $V_{cc}$ Core = +2.5V±5%; $V_{cc}$ I/O = +3.3V±5%

| Signal | Symbol | Reference Edge | 100MHz[1] | | 133MHz[1] | | 150MHz[1] | | Units | User Manual Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| **Local System Interface** | | | | | | | | | | |
| mem_data[31:0] (data phase) | Tsu2 | cpu_masterclk rising | 6 | — | 5 | — | 4.8 | — | ns | Chapter 9, Figures 9.2 and 9.3 |
| mem_data[31:0] (data phase) | Thld2 | cpu_masterclk rising | 1.5 | — | 1.5 | — | 1.5 | — | ns | |
| cpu_dt_r_n | Tdo3 | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns | |
| mem_data[31:0] | Tdo4 | cpu_masterclk rising | — | 12 | — | 10 | — | 9.3 | ns | |
| mem_data[31:0] output hold time | Tdoh1 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| mem_data[31:0] (tristate disable time) | Tdz | cpu_masterclk rising | — | 12[2] | — | 10[2] | — | 9.3[2] | ns | Chapter 10, Figures 10.6 through 10.8 |
| mem_data[31:0] (tristate to data time) | Tzd | cpu_masterclk rising | — | 12[2] | — | 10[2] | — | 9.3[2] | ns | |
| mem_wait_n | Tsu6 | cpu_masterclk rising | 9 | — | 7 | — | 6 | — | ns | |
| mem_wait_n | Thld8 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| mem_addr[22:2] | Tdo5 | cpu_masterclk rising | — | 12 | — | 9 | — | 8 | ns | |
| mem_cs_n[5:0] | Tdo6 | cpu_masterclk rising | — | 12 | — | 9 | — | 8 | ns | |
| mem_oe_n, mem_245_oe_n | Tdo7 | cpu_masterclk rising | — | 12 | — | 9 | — | 8 | ns | |
| mem_we_n[3:0] | Tdo7a | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns | |
| mem_245_dt_r_n | Tdo8 | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns | |
| mem_addr[25:2]<br>mem_cs_n[5:0]<br>mem_oe_n, mem_we_n[3:0],<br>mem_245_dt_r_n,<br>mem_245_oe_n | Tdoh3 | cpu_masterclk rising | 1.5 | — | 1.5 | — | 1.5 | — | ns | |
| **PCI for 3.3V Device[3]** | | | | | | | | | | |
| pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n | Tsu | pci_clk rising | 3 | — | 3 | — | 3 | — | ns | |
| pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n | Tsu | pci_clk rising | 5 | — | 5 | — | 5 | — | ns | |
| pci_gnt_n[0] | Tsu | pci_clk rising | 5 | — | 5 | — | 5 | — | ns | |
| pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n[4] | Thld | pci_clk rising | 0 | — | 0 | — | 0 | — | ns | |

**Table 6 AC Timing Characteristics - RC32332 (Part 1 of 4)**

| Signal | Symbol | Reference Edge | 100MHz[1] | | 133MHz[1] | | 150MHz[1] | | Units | User Manual Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n | Thld | pci_clk rising | 0 | — | 0 | — | 0 | — | ns | |
| pci_eeprom_mdi | Tsu | pci_clk rising, pci_eeprom_sk falling | 15 | — | 12 | — | 10 | — | ns | |
| pci_eeprom_mdi | Thld | pci_clk rising, pci_eeprom_sk falling | 15 | — | 12 | — | 10 | — | ns | |
| pci_eeprom_mdo, pci-eeprom_cs | Tdo | pci_clk rising, pci_eeprom_sk falling | — | 15 | — | 12 | — | 10 | ns | |
| pci_eeprom_sk | Tdo | pci_clk rising | — | 15 | — | 12 | — | 10 | ns | |
| pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n | Tdo | pci_clk rising | 2 | 7.5 | 2 | 7.5 | 2 | 7.5 | ns | |
| pci_req_n[0], pci_gnt_[2], pci_gnt_n[1], pci_gnt_n[0], pci_inta_n | Tdo | pci_clk rising | 2 | 7.5 | 2 | 7.5 | 2 | 7.5 | ns | |
| **PCI for 2.5V Device [3]** | | | | | | | | | | |
| pci_ad[31:0], pci_par, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n[4] | Tsu | pci_clk rising | 3 | — | 3 | — | 3 | — | ns | |
| pci_cbe_n[3:0], pci_frame_n, pci_trdy_n, pci_irdy_n | Tsu | pci_clk rising | 4 | — | 4 | — | 4 | — | ns | |
| pci_idsel, pci_req_n[2], pci_req_n[0], pci_gnt_n[0], pci_inta_n | Tsu | pci_clk rising | 5 | — | 5 | — | 5 | — | ns | |
| pci_gnt_n[0] | Tsu | pci_clk rising | 5 | — | 5 | — | 5 | — | ns | |
| pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n[4] | Thld | pci_clk rising | 0 | — | 0 | — | 0 | — | ns | |
| pci_idsel, pci_req_n[2], pci_req_n[0], pci_gnt_n[0], pci_inta_n | Thld | pci_clk rising | 0 | — | 0 | — | 0 | — | ns | |
| pci_eeprom_mdi | Tsu | pci_clk rising, pci_eeprom_sk falling | 15 | — | 12 | — | 10 | — | ns | |
| pci_eeprom_mdi | Thld | pci_clk rising, pci_eeprom_sk falling | 15 | — | 12 | — | 10 | — | ns | |
| pci_eeprom_mdo, pci-eeprom_cs | Tdo | pci_clk rising, pci_eeprom_sk falling | — | 15 | — | 12 | — | 10 | ns | |
| pci_eeprom_sk | Tdo | pci_clk rising | — | 15 | — | 12 | — | 10 | ns | |

**Table 6 AC Timing Characteristics - RC32332 (Part 2 of 4)**

| Signal | Symbol | Reference Edge | 100MHz[1] | | 133MHz[1] | | 150MHz[1] | | Units | User Manual Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n | Tdo | pci_clk rising | 2 | 7.5 | 2 | 7.5 | 2 | 7.5 | ns | |
| pci_req_n[0], pci_gnt_[2], pci_gnt_n[1], pci_gnt_n[0], pci_inta_n | Tdo | pci_clk rising | 2 | 7.5 | 2 | 7.5 | 2 | 7.5 | ns | |
| **SDRAM Controller** | | | | | | | | | | |
| sdram_245_dt_r_n | Tdo8 | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns | Chapter 11, Figures 11.4 and 11.5 |
| sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0], sdram_cke | Tdo9 | cpu_masterclk rising | — | 12 | — | 9 | — | 8 | ns | |
| sdram_addr_12 | Tdo10 | cpu_masterclk rising | — | 12 | — | 9 | — | 8 | ns | |
| sdram_245_oe_n | Tdo11 | cpu_masterclk rising | — | 12 | — | 9 | — | 8 | ns | |
| sdram_245_dt_r_n | Tdoh4 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0] sdram_cke, sdram_addr_12, sdram_245_oe_n | Tdoh4 | cpu_masterclk rising | 2.5 | — | 2.5 | — | 2.5 | — | ns | |
| **DMA** | | | | | | | | | | |
| dma_ready_n[0], dma_done_n[0] | Tsu7 | cpu_masterclk rising | 9 | — | 7 | — | 6 | — | ns | Chapter 13, Figure 13.4 |
| dma_ready_n[0], dma_done_n[0] | Thld9 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| **Interrupt Handling** | | | | | | | | | | |
| cpu_int_n[1:0], cpu_nmi_n | Tsu9 | cpu_masterclk rising | 9 | — | 7 | — | 6 | — | ns | Chapter 14, Figure 14.12 |
| cpu_int_n[1:0], cpu_nmi_n | Thld13 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| **PIO** | | | | | | | | | | |
| PIO[7:0] | Tsu7 | cpu_masterclk rising | 9 | — | 7 | — | 6 | — | ns | Chapter 15, Figures 15.9 and 15.10 |
| PIO[7:0] | Thld9 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| PIO[7:6], PIO[4:0] | Tdo16 | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns | |
| PIO[5] | Tdo19 | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns | |
| PIO[7:6], PIO[4:0] | Tdoh7 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| PIO[5] | Tdoh7 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| **UARTs** | | | | | | | | | | |
| uart_rx[0], uart_tx[0] | Tsu7 | cpu_masterclk rising | 15 | — | 12 | — | 10 | — | ns | Chapter 17, Figure 17.16 |
| uart_rx[0], uart_tx[0] | Thld9 | cpu_masterclk rising | 15 | — | 12 | — | 10 | — | ns | |
| uart_rx[0], uart_tx[0] | Tdo16 | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns | |
| uart_rx[0], uart_tx[0] | Tdoh8 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |

**Table 6 AC Timing Characteristics - RC32332 (Part 3 of 4)**

| Signal | Symbol | Reference Edge | 100MHz[1] | | 133MHz[1] | | 150MHz[1] | | Units | User Manual Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| **Reset** | | | | | | | | | | |
| mem_addr[19:17] | Tsu10 | cpu_coldreset_n rising | 10 | — | 10 | — | 10 | — | ms | Chapter 19, Figures 19.8 and 19.9 |
| mem_addr[19:17] | Thld10 | cpu_coldreset_n rising | 1 | — | 1 | — | 1 | — | ns | |
| mem_addr[22:20] | Tsu22 | cpu_masterclk rising | 9 | — | 7 | — | 6 | — | ns | |
| mem_addr[22:20] | Thld22 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| **Debug Interface** | | | | | | | | | | |
| debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0] | Tsu20 | cpu_coldreset_n rising | 10 | — | 10 | — | 10 | — | ms | Chapter 19, Figure 19.9 and Chapter 9, Figure 9.2 |
| debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0] | Thld20 | cpu_coldreset_n rising | 1 | — | 1 | — | 1 | — | ns | |
| debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n | Tdo20 | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns | |
| debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n | Tdoh20 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns | |
| **JTAG Interface** | | | | | | | | | | |
| jtag_tms, jtag_tdi, jtag_trst_n | $t_5$ | jtag_tck rising | 10 | — | 10 | — | 10 | — | ns | See Figure 4 below. |
| jtag_tms, jtag_tdi, jtag_trst_n | $t_6$ | jtag_tck rising | 10 | — | 10 | — | 10 | — | ns | |
| jtag_tdo | $t_4$ | jtag_tck falling | — | 10 | — | 10 | — | 10 | ns | |
| **EJTAG Interface** | | | | | | | | | | |
| ejtag_tms, ejtag_debugboot | $t_5$ | jtag_tclk rising | 4 | — | 4 | — | 4 | — | ns | See Figure 4 below. |
| ejtag_tms, ejtag_debugboot | $t_6$ | jtag_clk rising | 2 | — | 2 | — | 2 | — | ns | |
| jtag_tdo Output Delay Time | $t_{TDODO}$, $t_4$ | jtag_tck falling | — | 6 | — | 6 | — | 6 | ns | |
| jtag_tdi Input Setup Time | $t_{TDIS}$, $t_5$ | jtag_tck rising | 4 | — | 4 | — | 4 | — | ns | |
| jtag_tdi Input Hold Time | $t_{TDIH}$, $t_6$ | jtag_tck rising | 2 | — | 2 | — | 2 | — | ns | |
| jtag_trst_n Low Time | $t_{TRSTLow}$, $t_{12}$ | — | 100 | — | 100 | — | 100 | — | ns | |
| jtag_trst_n Removal Time | $t_{TRSTR}$, $t_{13}$ | jtag_tck rising | 3 | — | 3 | — | 3 | — | ns | |
| ejtag_tpc Output Delay Time | $t_{TPCDO}$, $t_8$ | ejtag_dclk rising | -1 | 3 | -1 | 3 | -1 | 3 | ns | |
| ejtag_pcst Output Delay Time | $t_{PCSTDO}$, $t_7$ | ejtag_dclk rising | -1 | 3 | -1 | 3 | -1 | 3 | ns | |

**Table 6 AC Timing Characteristics - RC32332 (Part 4 of 4)**

1. At all pipeline frequencies.

2. Guaranteed by design.

3. This PCI interface conforms to the PCI Local Bus Specification, Rev 2.2 at 33MHz.

4. pci_rst_n is tested per PCI 2.2 as an asynchronous signal.

## Standard EJTAG Timing — RC32332

Figure 4 represents the timing diagram for the EJTAG interface signals.

The standard JTAG connector is a 10-pin connector providing 5 signals and 5 ground pins. For Standard EJTAG, a 24-pin connector has been chosen providing 12 signals and 12 ground pins. This guarantees elimination of noise problems by incorporating signal-ground type arrangement. Refer to the RC32334/RC32332 User Reference Manual for connector pinout and mechanical specifications.

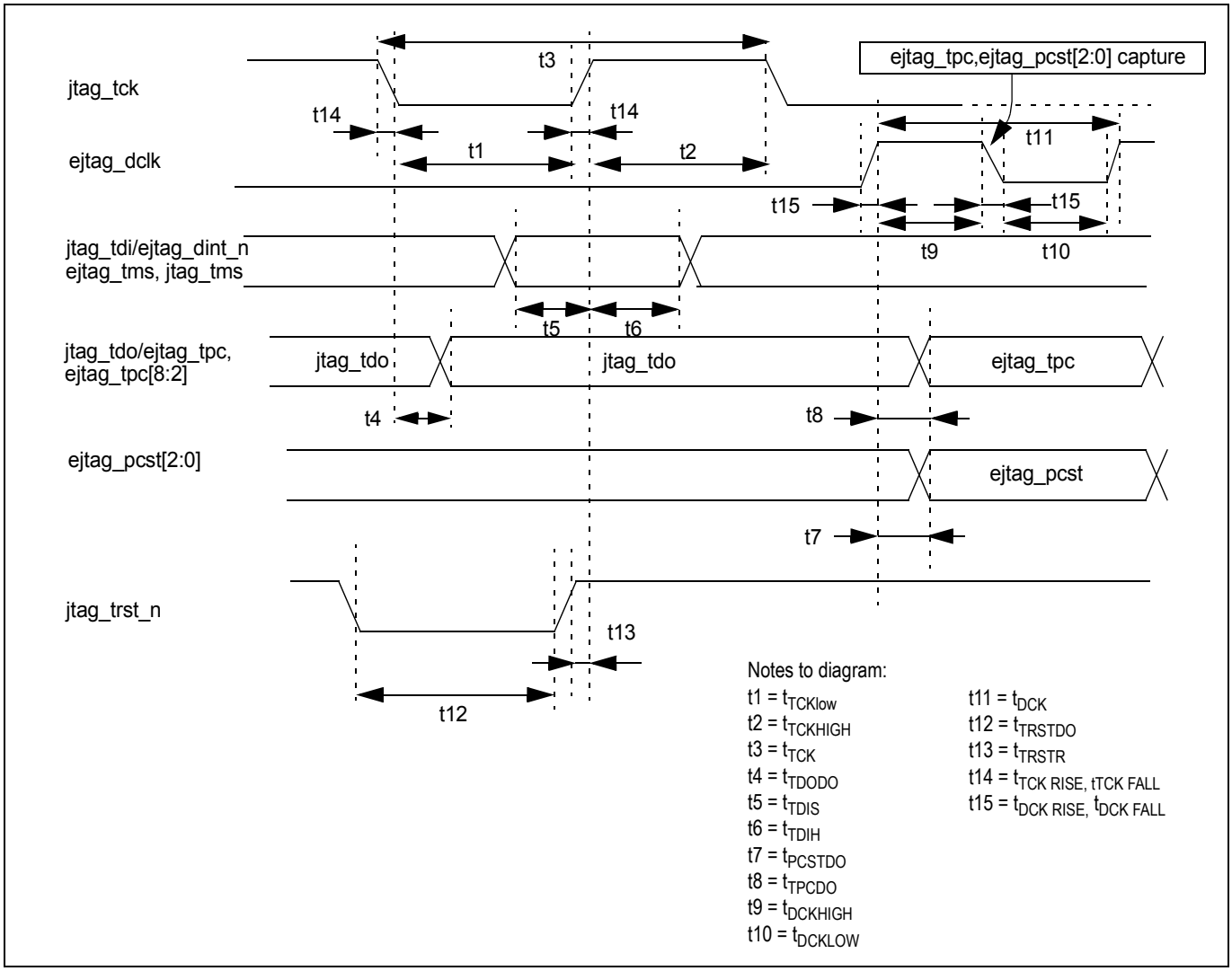
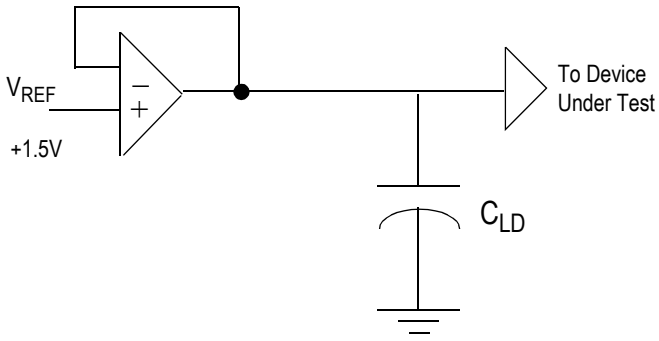



**Figure 4 Standard EJTAG Timing**

# Output Loading for AC Testing




| Signal | Cld |
|---|---|
| All High Drive Signals | 50 pF |
| All Low Drive Signals | 25 pF |

**Figure 5 Output Loading for AC Testing**

**Note:** PCI pins have been correlated to PCI 2.2.

# Recommended Operation Temperature and Supply Voltage

## 3.3V Device

| Grade | Ambient Temperature | Gnd | $V_{cc}IO$ | $V_{cc}Core$ | $V_{cc}P$ |
|---|---|---|---|---|---|
| Commercial | 0°C to +70°C Ambient | 0V | 3.3V±5% | 3.3V±5% | 3.3V±5% |
| Industrial | -40°C to +85°C Ambient | 0V | 3.3V±5% | 3.3V±5% | 3.3V±5% |

**Table 7 Temperature and Voltage — 3.3V Device**

## 2.5V Device

| Grade | Ambient Temperature | Gnd | $V_{cc}IO$ | $V_{cc}Core$ | $V_{cc}P$ |
|---|---|---|---|---|---|
| Commercial | 0°C to +70°C Ambient | 0V | 3.3V±5% | 2.5V±5% | 2.5V±5% |
| Industrial | -40°C to +85°C Ambient | 0V | 3.3V±5% | 2.5V±5% | 2.5V±5% |

**Table 8 Temperature and Voltage — 2.5V Device**

# DC Electrical Characteristics — RC32332

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: $V_{cc}$ Core = +3.3V±5%; $V_{cc}$ I/O = +3.3V±5%

2.5V version: $V_{cc}$ Core = +2.5V±5%; $V_{cc}$ I/O = +3.3V±5%

| | Parameter | RC32332[1] | | Pin Numbers | Conditions |
|---|---|---|---|---|---|
| | | Minimum | Maximum | | |
| Input Pads | $V_{IL}$ | — | 0.8V | 52, 64, 95, 160, 161, 164, 166-169, 176, 191 | — |
| | $V_{IH}$ | 2.0V | — | | — |
| LOW Drive Output Pads | $V_{OL}$ | — | 0.4V | 41-45, 48, 170, 171, 174, 175, 177-180, 185-190, 195-200, 207, 208 | $\|I_{OUT}\|$ = 6mA |
| | $V_{OH}$ | $V_{cc}$ - 0.4V | — | | $\|I_{OUT}\|$ = 8mA |
| | $V_{IL}$ | — | 0.8V | | — |
| | $V_{IH}$ | 2.0V | — | | — |
| HIGH Drive Output Pads | $V_{OL}$ | — | 0.4V | 1- 5, 8, 13-15, 18-25, 28-35, 38-40, 49-51, 53- 57, 60, 61, 63, 65-67,70-76, 79, 80, 83-87, 90-94, 153, 154, 156, 158, 165, 194, 201, 204, 205, 206 | $\|I_{OUT}\|$ = 7mA |
| | $V_{OH}$ | $V_{cc}$ - 0.4V | — | | $\|I_{OUT}\|$ = 16mA |
| | $V_{IL}$ | — | 0.8V | | — |
| | $V_{IH}$ | 2.0V | — | | — |
| PCI Drive Input Pads | $V_{IL}$ | — | — | 123, 155, 157, 159 | Per PCI 2.2 |
| | $V_{IH}$ | — | — | | |
| PCI Drive Output Pads | $V_{OL}$ | — | — | 96, 97, 100-109, 112-119, 122, 124-129, 132-139, 142-149, 152 | Per PCI 2.2 |
| | $V_{OH}$ | — | — | | |
| | $V_{IL}$ | — | — | | |
| | $V_{IH}$ | — | — | | |
| All Pads | $C_{IN}$ | — | 10pF | All input pads except 155 and 156 | — |
| | $C_{IN}$[2] | 5pf | 12pF | 155 | Per PCI 2.2 |
| | $C_{IN}$[3] | | 8pF | 156 | Per PCI 2.2 |
| | $C_{OUT}$ | — | 10pF | All output pads | — |
| | $I/O_{LEAK}$ | — | 10µA | All non-internal pull-up pins | Input/Output Leakage |
| | $I/O_{LEAK}$ | — | 50µA | All internal pull-up pins | Input/Output Leakage |

**Table 9 DC Electrical Characteristics - RC32332**

1. At all pipeline frequencies.
2. Applies only to pad 155.
3. Applies only to pad 156.

## Capacitive Load Deration — RC32332

Refer to the IDT document 79RC32332 IBIS Model located on the company's web site.

# Power Consumption

## 3.3V Device

**Note:** This table is based on a 2:1 pipeline-to-bus clock ratio.

| Parameter | | 100MHz | | 133MHz | | 150MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Typical | Max. | Typical | Max. | Typical | Max. | | |
| $I_{CC}$ | Normal mode | 360 | 480 | 480 | 630 | 550 | 700 | mA | $C_L$ = (See Figure 5, Output Loading for AC Testing)<br>$T_a$ = 25°C<br>$V_{cc}$ Core = 3.46V (for max. values)<br>$V_{cc}$ I/O = 3.46V (for max. values)<br>$V_{cc}$ Core = 3.3V (for typical values)<br>$V_{cc}$ I/O = 3.3V (for typical values) |
| | Standby mode[1] | 250 | 370 | 330 | 480 | 390 | 540 | mA | |
| Power Dissipation | Normal mode | 1.2 | 1.7 | 1.5 | 2.2 | 1.7 | 2.4 | W | |
| | Standby mode[1] | 0.83 | 1.3 | 1.1 | 1.7 | 1.3 | 1.9 | W | |

**Table 10 Power Consumption — 3.3V Device**

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

## 2.5V Device

**Note:** This table is based on a 2:1 pipeline-to-bus clock ratio.

| Parameter | | 100MHz | | 133MHz | | 150MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Typical | Max. | Typical | Max. | Typical | Max. | | |
| $I_{CC}$ I/O | Normal mode | 24 | 81 | 32 | 93 | 35 | 104 | mA | $C_L$ = (See Figure 5, Output Loading for AC Testing)<br>$T_a$ = 25°C<br>$V_{cc}$ Core = 2.625V (for max. values)<br>$V_{cc}$ I/O = 3.46V (for max. values)<br>$V_{cc}$ Core = 2.5V (for typical values)<br>$V_{cc}$ I/O = 3.3V (for typical values) |
| | Standby mode[1] | 2 | 81 | 2 | 93 | 2 | 104 | mA | |
| $I_{CC}$ core | Normal mode | 232 | 301 | 298 | 392 | 333 | 438 | mA | |
| | Standby mode[1] | 120 | 269 | 151 | 319 | 168 | 345 | mA | |
| Power Dissipation | Normal mode | 0.66 | 1.07 | 0.85 | 1.35 | 0.95 | 1.51 | W | |
| | Standby mode[1] | 0.31 | 0.94 | 0.38 | 1.10 | 0.43 | 1.21 | W | |

**Table 11 Power Consumption — 2.5V Device**

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

## Power Ramp-up

3.3V Device

There is no special requirement for how fast $V_{cc}$ I/O ramps up to 3.3V. However, all timing references are based on a stable $V_{cc}$ I/O.

2.5V Device

The 2.5V core supply (and 2.5V $V_{cc}$P supply) can be fully powered without the 3.3V I/O supply. However, the 3.3V I/O supply cannot exceed the 2.5V core supply by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the 3.3V I/O supply is powered.

There is no special requirement for how fast $V_{cc}$ I/O ramps up to 3.3V. However, all timing references are based on a stable $V_{cc}$ I/O.

## Power Curves

The following four graphs contain the simulated power curves that show power consumption at various bus frequencies. Figures 6 and 7 apply to the 3.3V device, while Figures 8 and 9 apply to the 2.5V device.

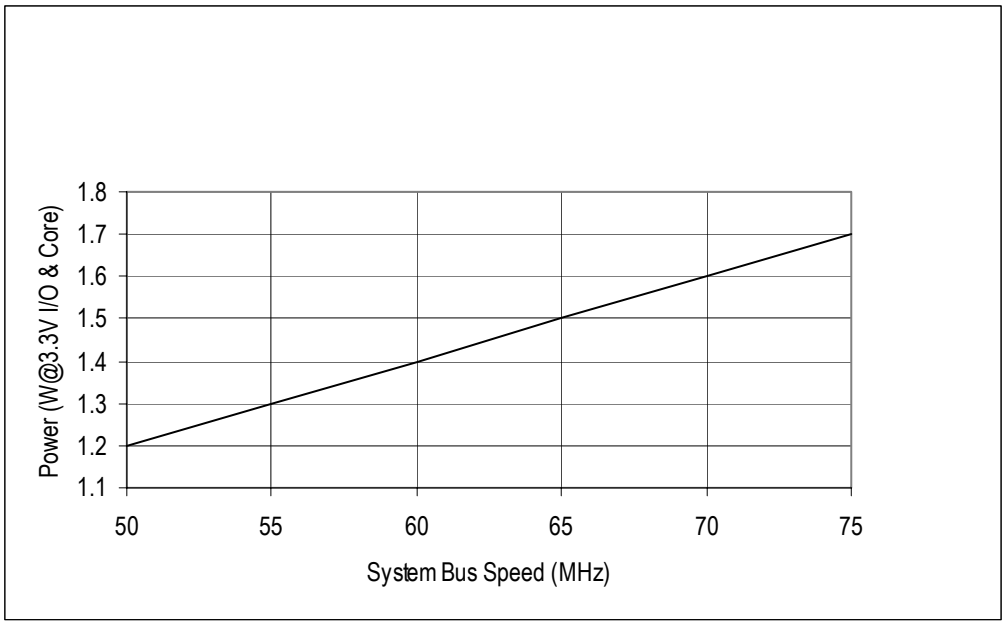



**Figure 6 Typical Power Usage — RC32V332 Device**

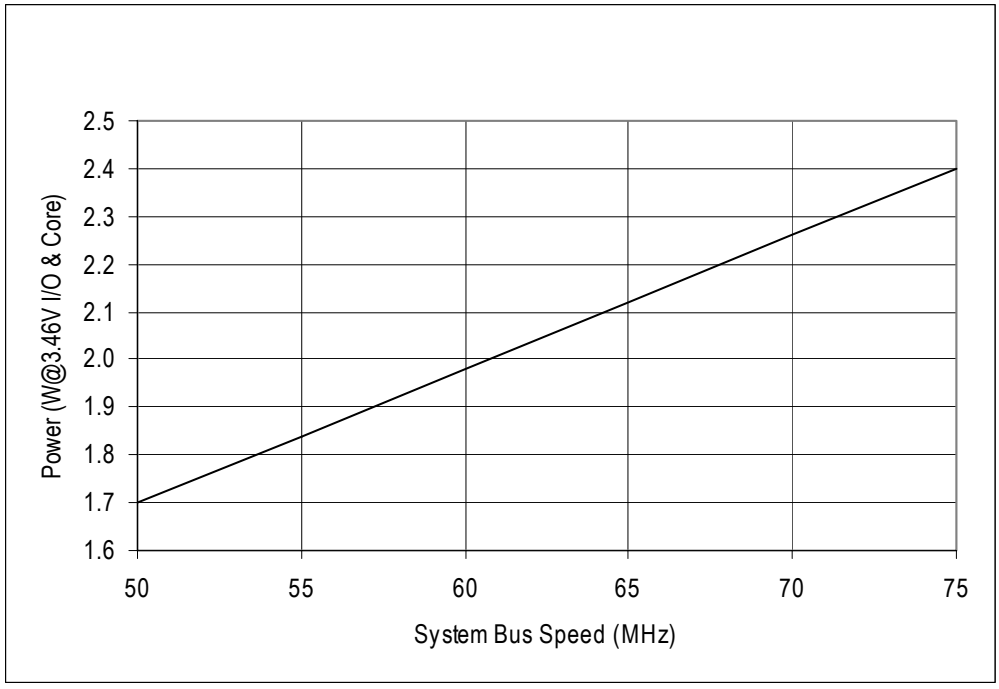



**Figure 7 Maximum Power Usage — RC32V332 Device**

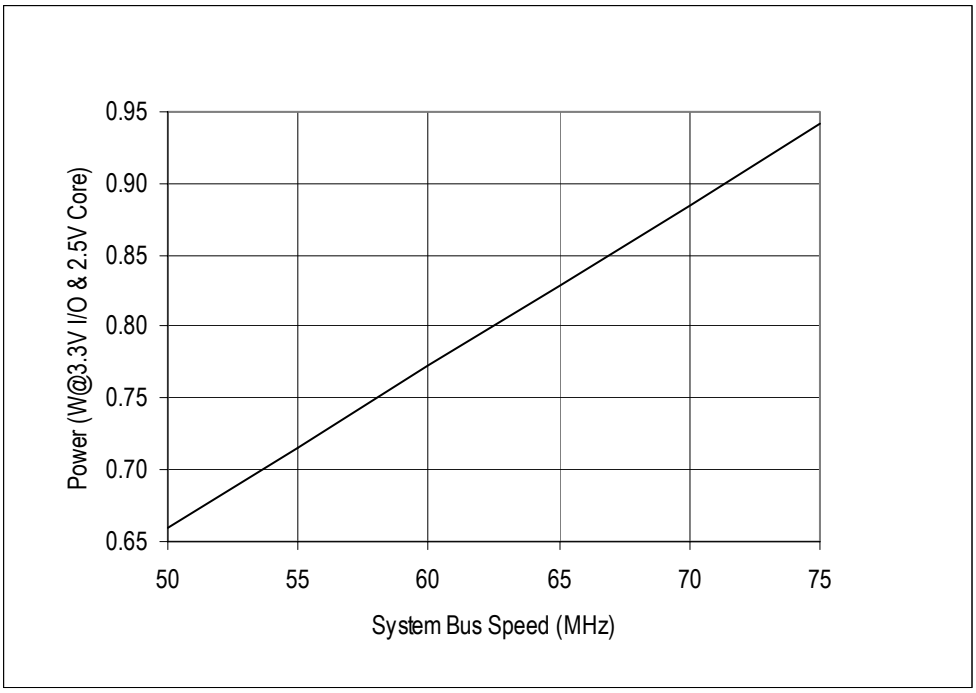



**Figure 8 Typical Power Usage — RC32T332 Device**

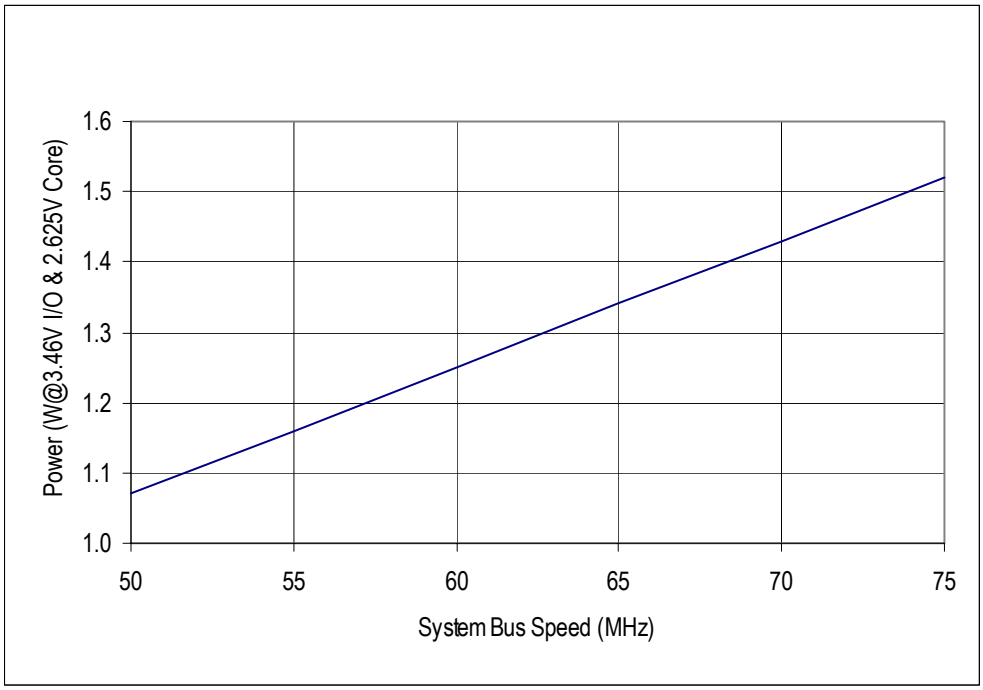



**Figure 9 Maximum Power Usage — RC32T332 Device**

# Absolute Maximum Ratings

| Symbol | Parameter | Min[1] | Max[1] | Unit |
|---|---|---|---|---|
| $V_{cc}$ Core 3.3V Device | Supply Voltage | -0.3 | 4.0 | V |
| $V_{cc}$ Core 2.5V Device | Supply Voltage | -0.3 | 3.0 | V |
| $V_{CC}$ I/O | I/O Supply Voltage | -0.3 | 4.0 | V |
| Vi 3.3V Device | Input Voltage | -0.3 | 5.5 | V |
| Vi 2.5V Device | Input Voltage | -0.3 | $V_{CC}$I/O+0.3 | V |
| Vimin | Input Voltage - undershoot[2] | -0.6 | — | V |
| Tstg | Storage Temperature | -40 | 125 | degrees C |

**Table 12 Absolute Maximum Ratings**

1. Functional and tested operating conditions are given in Table 7. Absolute maximum ratings are stress ratings only, and functional operation is not guaranteed beyond recommended operating voltages and temperatures. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. All PCI pads are fully compatible with PCI Specification version 2.2.

# Package Pin-out — 208-PQFP for RC32332

The following table lists the pin numbers and signal names for the RC32332. Signal names ending with an _n are active when low.

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | sdram_245_oe_n | | 53 | mem_data[12] | | 105 | pci_ad[7] | | 157 | pci_req_n[2] | 1 |
| 2 | sdram_we_n | | 54 | mem_data[19] | | 106 | pci_cbe_n[0] | | 158 | pci_gnt_n[2] | 1 |
| 3 | sdram_cas_n | | 55 | mem_data[13] | | 107 | pci_ad[8] | | 159 | pci_rst_n | |
| 4 | sdram_bemask_n[0] | | 56 | mem_data[18] | | 108 | pci_ad[9] | | 160 | cpu_int_n[0] | |
| 5 | sdram_bemask_n[1] | | 57 | mem_data[14] | | 109 | pci_ad[10] | | 161 | cpu_int_n[1] | |
| 6 | $V_{ss}$ | | 58 | $V_{ss}$ | | 110 | $V_{ss}$ | | 162 | $V_{ss}$ | |
| 7 | $V_{cc}$ I/O | | 59 | $V_{cc}$ I/O | | 111 | $V_{cc}$ I/O | | 163 | $V_{cc}$ I/O | |
| 8 | sdram_cs_n[0] | | 60 | mem_data[17] | | 112 | pci_ad[11] | | 164 | jtag_tdi | |
| 9 | sdram_cs_n[1] | | 61 | mem_data[16] | | 113 | pci_ad[12] | | 165 | jtag_tdo | |
| 10 | sdram_ras_n | | 62 | $V_{cc}$ core | | 114 | pci_ad[13] | | 166 | jtag_tms | |
| 11 | sdram_s_n[0] | | 63 | mem_data[15] | | 115 | pci_ad[14] | | 167 | ejtag_tms | |
| 12 | sdram_s_n[1] | | 64 | cpu_masterclk | | 116 | pci_ad[15] | | 168 | jtag_tck | |
| 13 | mem_addr[2] | 1 | 65 | mem_data[31] | | 117 | pci_cbe_n[1] | | 169 | jtag_trst_n | |
| 14 | mem_addr[3] | 1 | 66 | mem_data[0] | | 118 | pci_par | | 170 | ejtag_pcst[0] | 1 |
| 15 | mem_addr[4] | 1 | 67 | mem_data[30] | | 119 | pci_serr_n | | 171 | ejtag_pcst[1] | 1 |
| 16 | $V_{ss}$ | | 68 | $V_{ss}$ | | 120 | $V_{ss}$ | | 172 | $V_{ss}$ | |
| 17 | $V_{cc}$ I/O | | 69 | $V_{cc}$ I/O | | 121 | $V_{cc}$ I/O | | 173 | $V_{cc}$ I/O | |
| 18 | mem_addr[5] | 1 | 70 | mem_data[1] | | 122 | pci_perr_n | | 174 | ejtag_pcst[2] | 1 |
| 19 | mem_addr[6] | 1 | 71 | mem_data[29] | | 123 | pci_lock_n | | 175 | ejtag_dclk | |

**Table 13 RC32332 208-pin QFP Package Pin-Out (Part 1 of 2)**

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 20 | mem_addr[7] | 1 | 72 | mem_data[2] | | 124 | pci_stop_n | | 176 | ejtag_debugboot | |
| 21 | mem_addr[8] | 1 | 73 | mem_data[28] | | 125 | pci_devsel_n | | 177 | debug_cpu_i_d_n | 1 |
| 22 | mem_addr[9] | 1 | 74 | mem_data[3] | | 126 | pci_trdy_n | | 178 | debug_cpu_ads_n | 1 |
| 23 | mem_addr[10] | 1 | 75 | mem_data[27] | | 127 | pci_irdy_n | | 179 | debug_cpu_ack_n | 1 |
| 24 | mem_addr[11] | 1 | 76 | mem_data[4] | | 128 | pci_frame_n | | 180 | debug_cpu_dma_n | 1 |
| 25 | output_clk | | 77 | $V_{cc}$p | | 129 | pci_cbe_n[2] | | 181 | $V_{cc}$ I/O | |
| 26 | $V_{ss}$ | | 78 | $V_{ss}$p | | 130 | $V_{ss}$ | | 182 | $V_{ss}$ | |
| 27 | $V_{cc}$ core | | 79 | mem_data[26] | | 131 | $V_{cc}$ core | | 183 | $V_{cc}$ core | |
| 28 | mem_addr_12 | | 80 | mem_data[5] | | 132 | pci_ad[16] | | 184 | $V_{cc}$ I/O | |
| 29 | sdram_addr_12 | | 81 | $V_{ss}$ | | 133 | pci_ad[17] | | 185 | spi_ss_n | 1 |
| 30 | sdram_cke | | 82 | $V_{cc}$ core | | 134 | pci_ad[18] | | 186 | spi_sck | 2 |
| 31 | sdram_cs_n[2] | | 83 | cpu_dt_r_n | 2 | 135 | pci_ad[19] | | 187 | spi_miso | 2 |
| 32 | sdram_cs_n[3] | | 84 | mem_data[25] | | 136 | pci_ad[20] | | 188 | spi_mosi | 2 |
| 33 | sdram_bemask_n[2] | | 85 | mem_data[6] | | 137 | pci_ad[21] | | 189 | dma_ready_n[0] | 2 |
| 34 | sdram_bemask_n[3] | | 86 | mem_data[24] | | 138 | pci_ad[22] | | 190 | mem_245_oe_n | |
| 35 | mem_addr[13] | | 87 | mem_data[7] | | 139 | pci_ad[23] | | 191 | mem_wait_n | 2 |
| 36 | $V_{ss}$ | | 88 | $V_{ss}$ | | 140 | $V_{ss}$ | | 192 | $V_{ss}$ | |
| 37 | $V_{cc}$ I/O | | 89 | $V_{cc}$ I/O | | 141 | $V_{cc}$ I/O | | 193 | $V_{cc}$ I/O | |
| 38 | mem_addr[14] | | 90 | mem_data[23] | | 142 | pci_cbe_n[3] | | 194 | mem_oe_n | |
| 39 | mem_addr[15] | 1 | 91 | mem_data[8] | | 143 | pci_ad[24] | | 195 | mem_cs_n[0] | |
| 40 | mem_addr[16] | 1 | 92 | mem_data[22] | | 144 | pci_ad[25] | | 196 | mem_cs_n[1] | |
| 41 | mem_addr[17] | 1 | 93 | mem_data[9] | | 145 | pci_ad[26] | | 197 | mem_cs_n[2] | |
| 42 | mem_addr[18] | 1 | 94 | mem_data[21] | | 146 | pci_ad[27] | | 198 | mem_cs_n[3] | |
| 43 | mem_addr[19] | 1 | 95 | cpu_nmi_n | | 147 | pci_ad[28] | | 199 | mem_cs_n[4] | |
| 44 | mem_addr[20] | 1 | 96 | pci_ad[0] | | 148 | pci_ad[29] | | 200 | mem_cs_n[5] | |
| 45 | mem_addr[21] | 1 | 97 | pci_ad[1] | | 149 | pci_ad[30] | | 201 | mem_we_n[0] | |
| 46 | $V_{ss}$ | | 98 | $V_{ss}$ | | 150 | $V_{ss}$ | | 202 | $V_{ss}$ | |
| 47 | $V_{cc}$ I/O | | 99 | $V_{cc}$ I/O | | 151 | $V_{cc}$ I/O | | 203 | $V_{cc}$ I/O | |
| 48 | mem_addr[22] | 1 | 100 | pci_ad[2] | | 152 | pci_ad[31] | | 204 | mem_we_n[1] | |
| 49 | mem_data[10] | | 101 | pci_ad[3] | | 153 | pci_req_n[0] | | 205 | mem_we_n[2] | |
| 50 | mem_data[11] | | 102 | pci_ad[4] | | 154 | pci_gnt_n[0] | | 206 | mem_we_n[3] | |
| 51 | mem_data[20] | | 103 | pci_ad[5] | | 155 | pci_clk | | 207 | uart_tx[0] | 1 |
| 52 | cpu_coldreset_n | | 104 | pci_ad[6] | | 156 | pci_gnt_n[1] | 2 | 208 | uart_rx[0] | 1 |

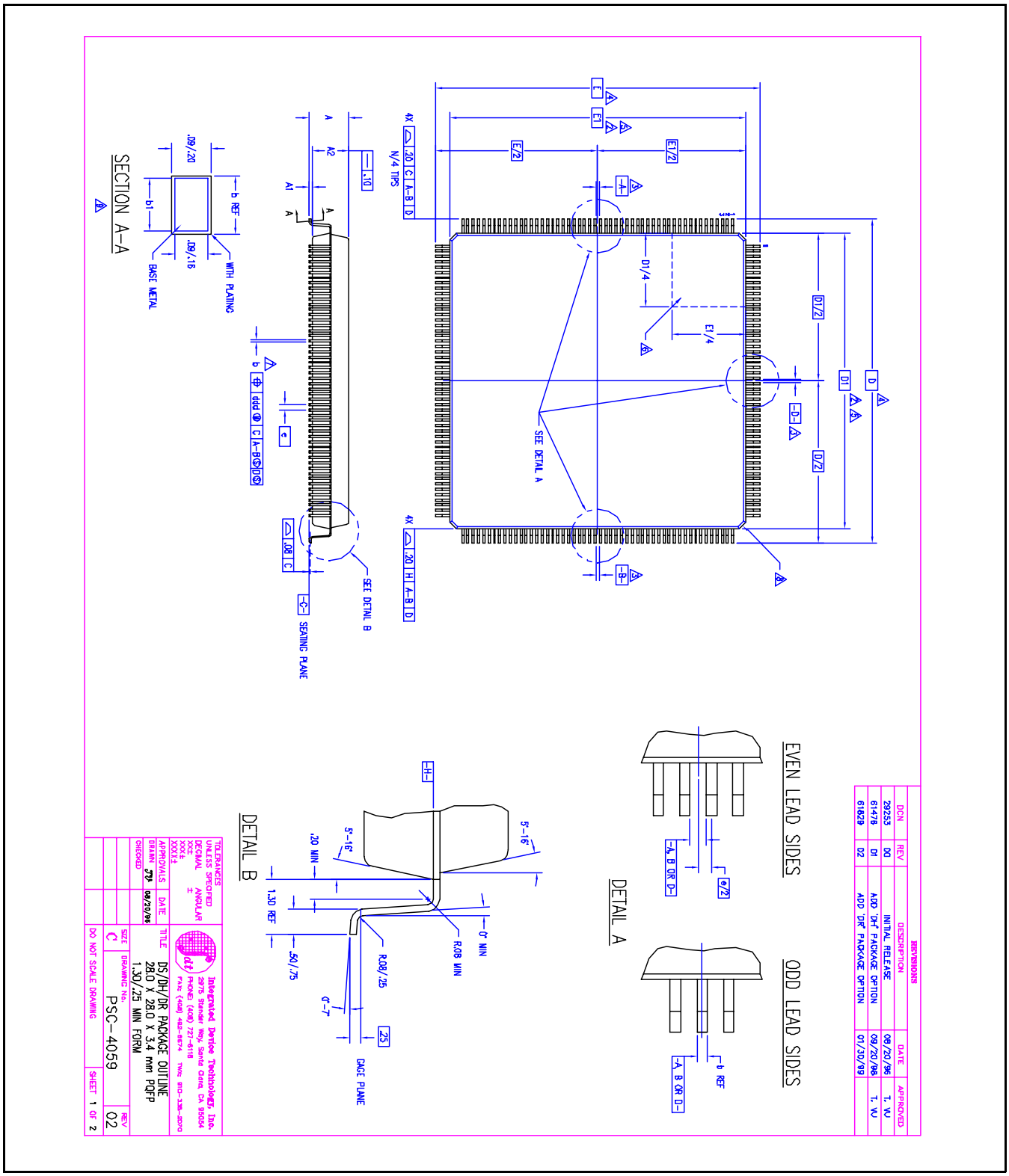
**Table 13 RC32332 208-pin QFP Package Pin-Out (Part 2 of 2)**

# RC32332 Alternate Signal Functions

| Pin | Alt #1 | Alt #2 | Pin | Alt #1 | Alt #2 | Pin | Alt #1 | Alt #2 |
|---|---|---|---|---|---|---|---|---|
| 13 | sdram_addr[2] | | 40 | sdram_addr[16] | | 174 | modebit[2] | |
| 14 | sdram_addr[3] | | 41 | modebit[7] | | 177 | modebit[3] | |
| 15 | sdram_addr[4] | | 42 | modebit[8] | | 178 | modebit[5] | |
| 18 | sdram_addr[5] | | 43 | modebit[9] | | 179 | modebit[4] | |
| 19 | sdram_addr[6] | | 44 | reset_pci_host_mode | | 180 | modebit[6] | |
| 20 | sdram_addr[7] | | 45 | reset_boot_mode[0] | | 185 | PIO[4] | |
| 21 | sdram_addr[8] | | 48 | reset_boot_mode[1] | | 186 | PIO[5] | pci_eeprom_sk |
| 22 | sdram_addr[9] | | 83 | mem_245_dt_r_n | sdram_245_dt_r_n | 187 | PIO[3] | pci_eeprom_mdi |
| 23 | sdram_addr[10] | | 156 | pci_eeprom_cs (satellite) | PIO[7] | 188 | PIO[6] | pci_eeprom_mdo |
| 24 | sdram_addr[11] | | 157 | pci_idsel (satellite) | | 189 | PIO[0] | dma_done_n[0] |
| 35 | sdram_addr[13] | | 158 | pci_inta_n (satellite) | | 191 | sdram_wait_n | mem_wait_n |
| 38 | sdram_addr[14] | | 170 | modebit[0] | | 207 | PIO[1] | |
| 39 | sdram_addr[15] | | 171 | modebit[1] | | 208 | PIO[2] | |

**Table 14 RC32332 Alternate Signal Functions**

# RC32332 Package Drawing — 208-pin PQFP



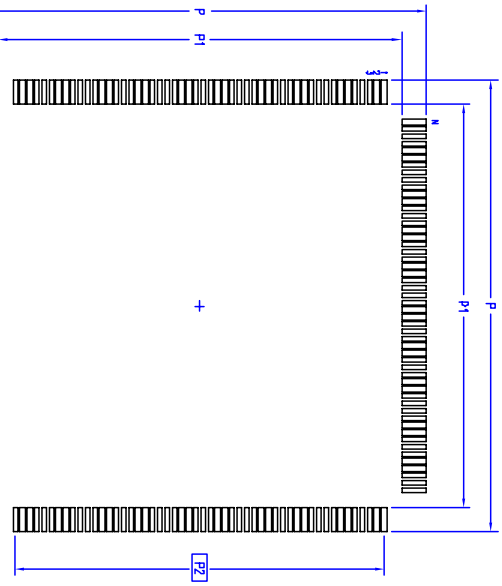
## RC32332 Package Drawing — Page Two

| SYMBOL | JEDEC VARIATION FA-1 MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | - | - | 4.10 | |
| A1 | .25 | - | - | |
| A2 | 3.20 | 3.40 | 3.60 | |
| D | 30.60 BSC | | | 4 |
| D1 | 28.00 BSC | | | 5,2 |
| E | 30.60 BSC | | | 4 |
| E1 | 28.00 BSC | | | 5,2 |
| N | 208 | | | |
| e | .50 BSC | | | |
| b | .17 | - | .27 | 7 |
| b1 | .17 | .20 | .23 | |
| ddd | - | - | .08 | |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-143, VARIATION FA-1

LAND PATTERN DIMENSIONS




| | MIN | MAX |
|---|---|---|
| P | 31.20 | 31.40 |
| P1 | 27.80 | 28.00 |
| P2 | 25.50 BSC | |
| X | .30 | .40 |
| e | .50 BSC | |
| N | 208 | |

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 29253 | 00 | INITIAL RELEASE | 08/20/96 | T. VU |
| 61476 | 01 | ADD "DH" PACKAGE OPTION | 09/20/98 | T. VU |
| 61829 | 02 | ADD "DR" PACKAGE OPTION | 01/10/99 | |

TOLERANCES UNLESS SPECIFIED DECIMAL XX± .XXX± ANGULAR ± XX.X± XXX.X±

APPROVALS DATE
DRAWN 09/20/96
CHECKED

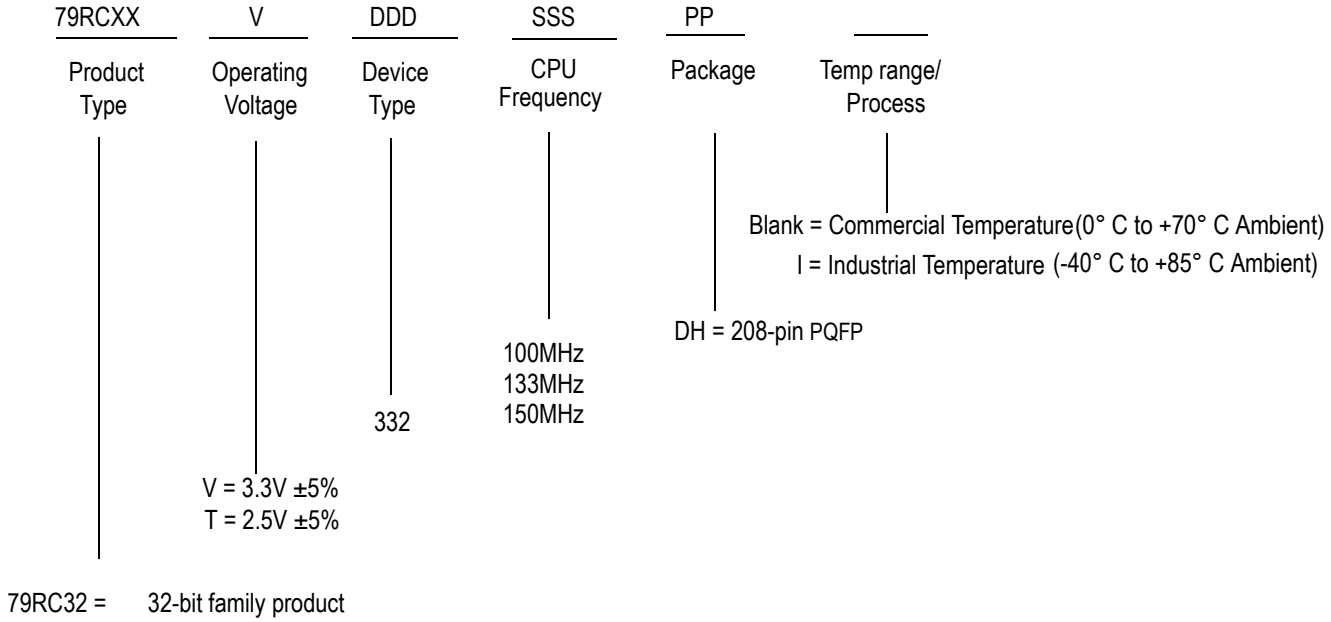
Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070

TITLE: D5/DH/DR PACKAGE OUTLINE 28.0 X 28.0 X 3.4 mm PQFP 1.30/.25 MIN FORM

SIZE: C | DRAWING No.: PSC-4059 | REV: 02

DO NOT SCALE DRAWING | SHEET 2 OF 2

# Ordering Information




# Valid Combinations

**3.3V Device**

| | |
|---|---|
| 79RC32V332 - 100DH, 133DH, 150DH | Commercial |
| 79RC32V332 - 100DHI, 133DHI, 150DHI | Industrial |

**2.5V Device**

| | |
|---|---|
| 79RC32T332 - 100DH, 133DH, 150DH | Commercial |
| 79RC32T332 - 100DHI, 133DHI, 150DHI | Industrial |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/


### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.