Discontinuous Conduction Mode (DCM) Interleaved PFC IC

SSC2102S

General Descriptions

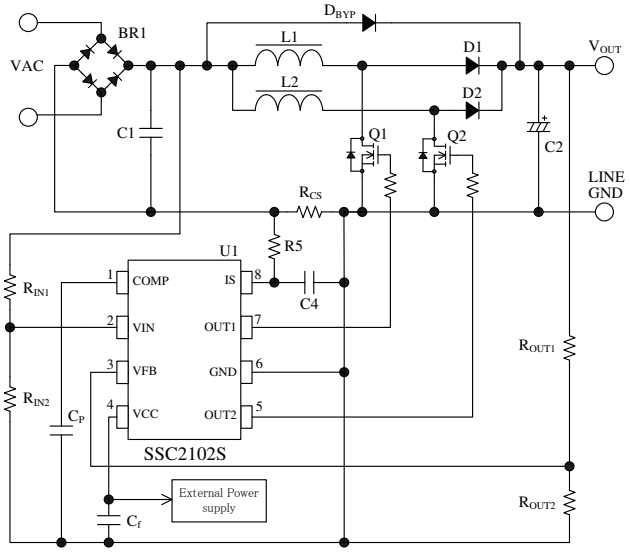
SSC2102S is controller ICs intended to implement a DCM (Discontinuous Conduction Mode) interleaved PFC (Power Factor Correction) circuit.

Using the two-phase interleaved control incorporated in this IC, it is possible to achieve a low cost, high performance PFC system with low input / output ripple currents, low noises and few external components.

Features

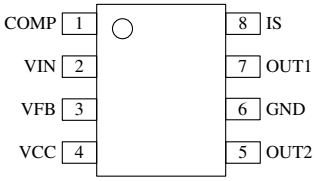
- No Auxiliary Windings on Inductors Required
- Voltage Mode Control
- Maximum ON Time Control Circuit
- Soft-start Function
- Built-in High Speed Response Function (HSR)
- Protections
  Dual level Overcurrent Protection (OCP) Pulse-by Pulse
  Dual level Overvoltage Protection (OVP)---Auto-Restart
  Under Voltage Protection (UVP) ---------- Auto-Restart
  Thermal Shutdown with Hysteresis (TSD)
  ---------- Auto-Restart
  Open Loop Detection (OLD) ---------- Auto-Restart
  VFB pin /VIN pin / IS pin Open Pin Protection (OPP)

Typical Application Circuit



Package

SOP8



Not to scale

Electrical Characteristics

Maximum ON Time, t_{ONMAX} = 20.7 µs(typ.)
Error Amplifier Reference Voltage, $V_{FB(REF)}$ = 3.5 V(typ.)
OUT Pin Peak Source Current, $I_{OUT(SO)}$ = – 0.5 A*
OUT Pin Peak Sink Current, $I_{OUT(SI)}$ = 0.5 A*

*Design assurance item

Applications

PFC Circuit up to 300 W of Output Power such as:

- AC/DC Power Supply
- Digital Appliances (Large Size LCD Television and so forth)
- OA Equipment (Computer, Server, Monitor, and so forth)
- Communication Facilities
- Other SMPS

CONTENTS

1. Absolute Maximum Ratings

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified T_A = 25 °C

Parameter	Symbol	Test Conditions	Pins	Rating	Units
COMP Pin Voltage	V_{COMP}		1 – 6	− 0.3 to 5.5	V
VIN Pin Voltage	V_{IN}		2 – 6	− 0.3 to 5.5	V
VIN Pin Current	I_{IN}		2 – 6	− 1 to 1	mA
VFB Pin Voltage	V_{FB}		3 – 6	− 0.3 to 5.5	V
VFB Pin Current	I_{FB}		3 – 6	− 1 to 1	mA
VCC Pin Voltage	V_{CC}		4 – 6	− 0.3 to 30	V
OUT2 Pin Voltage	V_{DR2}		5 – 6	− 0.3 to 30	V
OUT1 Pin Voltage	V_{DR1}		7 – 6	− 0.3 to 30	V
IS Pin Voltage	V_{IS}		8 – 6	− 16.0 to 5.5	V
IS Pin Current	I_{IS}		8 – 6	− 1.75 to 1	mA
Operating Frame Temperature	T_{FOP}		−	− 40 to 85	°C
Storage Temperature	T_{stg}			− 40 to 125	°C
Junction Temperature	T_j		−	− 40 to 125	°C

2. Electrical Characteristics

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified, T_A = 25 °C, V_{CC} =15 V

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units
Power Supply Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		4 – 6	10.8	11.6	12.4	V
Operation Stop Voltage	$V_{CC(OFF)}$		4 – 6	9.8	10.6	11.4	V
VCC Pin Voltage Hysteresis	$V_{CC(HYS)}$		4 – 6	0.8	1.0	1.2	V
Circuit Current in Pre-operation	$I_{CC(OFF)}$	V_{CC} = 11 V	4 – 6	−	40	100	µA
Circuit Current in Operation	$I_{CC(ON)}$		4 – 6	−	11.0	15.0	mA
Circuit Current in Overvoltage Protection Operation	$I_{CC(OVP)}$	V_{FB} = 3.9 V	4 – 6	−	8.0	10.0	mA
Circuit Current in Standby Operation	$I_{CC(Standby)}$	V_{FB} = 0.5 V	4 – 6	−	100	200	µA
Oscillation Control							
OUT1 Pin Maximum ON Time	t_{ONMAX}		7 – 6	19.2	20.7	22.2	µs
On-time matching between OUT1 and OUT1	t_{RATIO}		5 – 6 7 – 6	− 5	0	5	%
OUT1 Pin and OUT2 pin Phase Difference	PHASE		5 – 6 7 – 6	170	180	190	deg

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units
Error Amplifier Operation							
Error Amplifier Reference Voltage	$V_{FB(REF)}$		3–6	3.4	3.5	3.6	V
Error Amplifier Transconductance Gain	gm_{EA}		—	80	100	120	µS
Error Amplifier Maximum Source Current	$I_{COMP(SO)}$	V_{FB} = 2.8 V	1–6	– 36	– 30	– 24	µA
Error Amplifier Maximum Voltage	$V_{COMP(MAX)}$	V_{FB} = 3.0 V	1–6	4.00	4.12	4.25	V
VFB Pin High Speed Response Enable Voltage(1)	$V_{FB(HSR)EN}$		3–6	3.3	3.4	3.5	V
VFB Pin High Speed Response Activating Voltage	$V_{FB(HSR)AC}$		3–6	3.1	3.2	3.3	V
COMP Pin Source Current in High Speed Response Operation	$I_{COMP(SO)HSR}$	V_{FB} = 2.5 V	1–6	– 120	– 100	– 80	µA
VFB Pin Input Bias Current	$I_{FB(BIAS)}$	V_{FB} = 3.5 V	3–6	—	—	1.5	µA
COMP Pin Voltage in Output Open Loop Detection Operation	$V_{COMP(OLD)}$	I_{COMP} = 100 µA	1–6	0.7	0.9	1.1	V
Drive Output							
OUT1 and OUT2 Pin Voltage (Low)	$V_{OUT(L)}$	I_{OUT} = 20 mA	5 – 6 7 – 6	–	–	0.3	V
OUT1 and OUT2 Pin Voltage (High)	$V_{OUT(H)}$	V_{CC} = 12 V	5 – 6 7 – 6	–	10.2	–	V
OUT1 and OUT2 Pin Rise Time(2)	t_r	V_{CC} = 20 V	5 – 6 7 – 6	–	70	–	ns
OUT1 and OUT2 Pin Fall Time(2)	t_f	V_{CC} = 20 V	5 – 6 7 – 6	–	35	–	ns
OUT1 and OUT2 Pin Peak Source Current(1)	$I_{OUT(SO)}$		5 – 6 7 – 6	–	– 0.5	–	A
OUT1 and OUT2 Pin Peak Sink Current(1)	$I_{OUT(SI)}$		5 – 6 7 – 6	–	0.5	–	A

(1) Design assurance item
(2) Shown in Figure 3-1

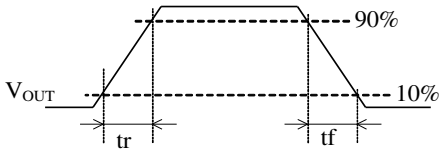
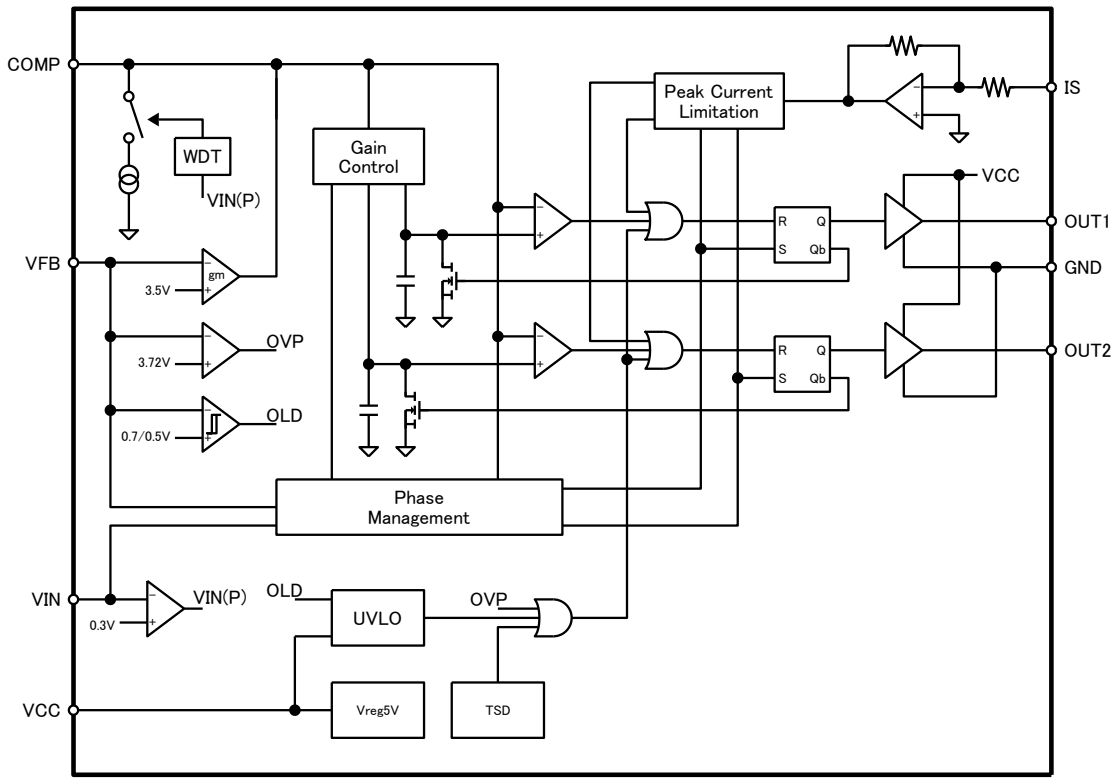


Figure 3-1 Switching time

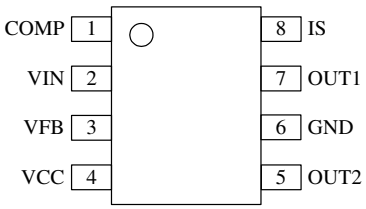
Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units
Protection Operation							
VFB Pin Output Open Loop Detection Voltage	$V_{FB(OLDL)}$		3 – 6	0.46	0.50	0.54	V
VFB Pin Output Open Loop Detection Release Voltage	$V_{FB(OLDH)}$		3 – 6	0.64	0.70	0.76	V
VFB Pin Soft Overvoltage Protection Threshold Voltage	$V_{FB(SOVP)}$		3 – 6	3.60	3.68	3.76	V
VFB Pin Overvoltage Protection Threshold Voltage	$V_{FB(OVP)}$		3 – 6	3.64	3.72	3.80	V
IS Pin Overcurrent Protection Threshold Voltage (Low)	$V_{IS(OCPL)}$		8 – 6	− 0.48	− 0.42	− 0.36	V
IS Pin Overcurrent Protection Threshold Voltage (High)	$V_{IS(OCPH)}$		8 – 6	− 0.62	− 0.55	− 0.48	V
COMP Sink Current in Protection Mode	$I_{COMP(SI)}$	V_{IS} = − 0.5 V	1 – 6	80	100	120	μA
VIN Pin Protection Threshold Voltage	$V_{IN(P)}$		2 – 6	0.1	0.3	0.5	V
VIN Pin Protection Delay Time	t_{VIN}		2 – 6	7	14	21	ms
Thermal Shutdown Activating Temperature (1)	T_{jTSDH}		–	150	–	–	°C
Thermal Shutdown Release Temperature (1)	T_{jTSDL}		–	140	–	–	°C
Hysteresis Temperature of Thermal Shutdown(1)	$T_{jTSDHYS}$		–	–	10	–	°C
Thermal Resistance							
Thermal Resistance from Junction to Frame	θ_{j-F}		–	–	65	85	°C/W

(1) Design assurance item

3. Functional Block Diagram

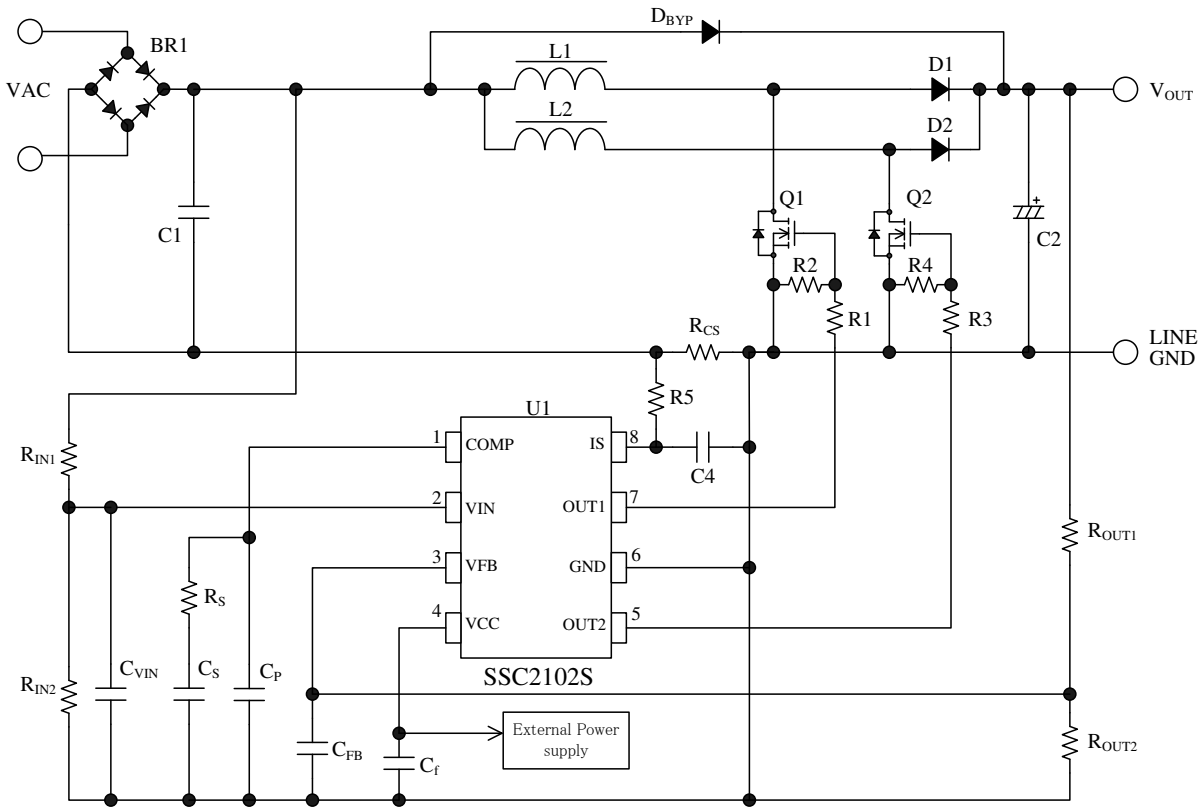


4. Pin Configuration Definitions



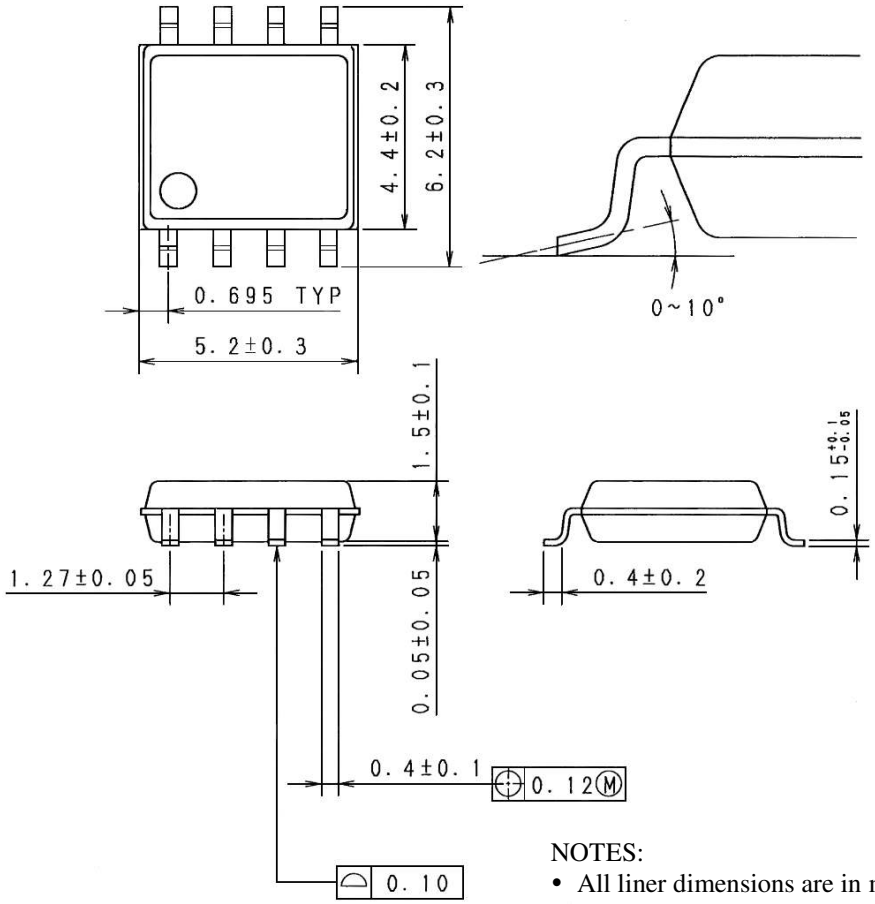
Pin	Name	Descriptions
1	COMP	Error amplifier output and phase compensation
2	VIN	Rectified input voltage detection
3	VFB	Constant voltage control signal input / Overvoltage signal input / Open loop detection signal input
4	VCC	Power supply for control circuit input
5	OUT2	2nd Gate driver output
6	GND	Ground
7	OUT1	1st Gate driver output
8	IS	Peak current detection signal input

5. Typical Application Circuit



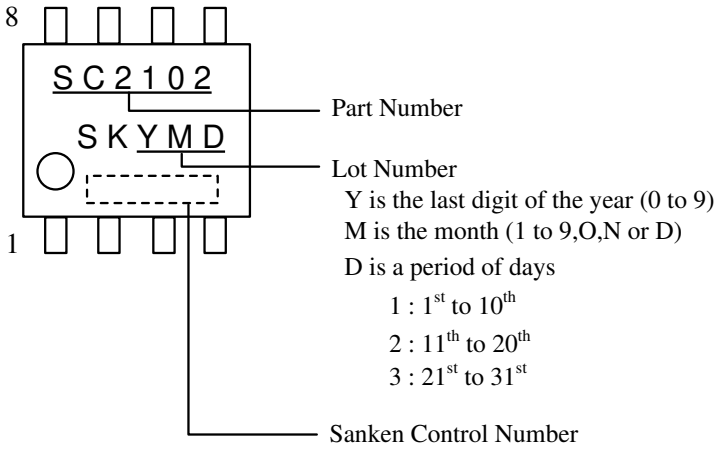
6. Package Outline

SOIC8



NOTES:
- All liner dimensions are in mm
- Pb-free. Device composition compliant with the RoHS directive

7. Marking Diagram



8. Operational Description

All of the parameter values used in these descriptions are typical values. With regard to current direction, "+" indicates sink current (toward the IC) and "−" indicates source current (from the IC).

8.1 Operational Description of Interleaved DCM

Figure 8-1 through Figure 8-4 show the PFC (Power Factor Correction) circuits and the operational waveforms of both single phase and two phase interleaved DCM (Discontinuous Conduction Mode).

Single phase DCM is well known as a technique that achieves low switching noises because the drain current increases from zero when a power MOSFET turns on, and is not steep shape waveforms as shown in Figure 8-2. However, the usable power level of the single phase DCM is limited by the very high input / output ripple currents.

The two phase interleaved DCM incorporates two boost converters, and is able to cancel the input ripple currents and to reduce the output ripple currents due to the phase difference of 180° between two converters as shown in Figure 8-3.

The interleaved DCM achieves a PFC system with lower switching noise and smaller input filter areas, compared with the single phase DCM. Because lower input / output ripple currents increase the filtering effect of EMI filters and reduce switching noises.

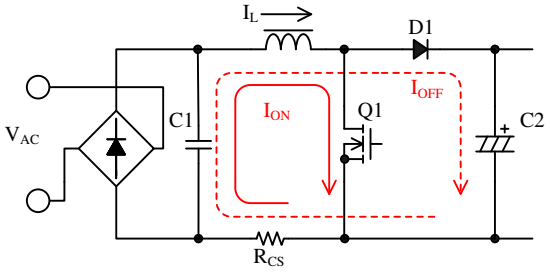


Figure 8-1 Single phase PFC circuit

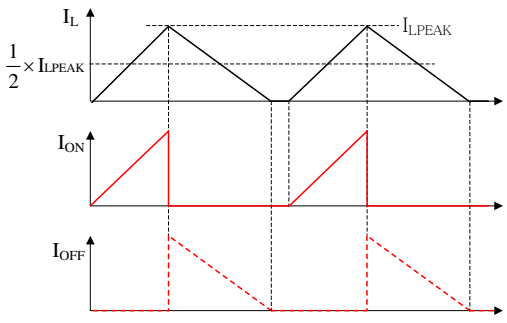


Figure 8-2 Operational waveform of single phase DCM

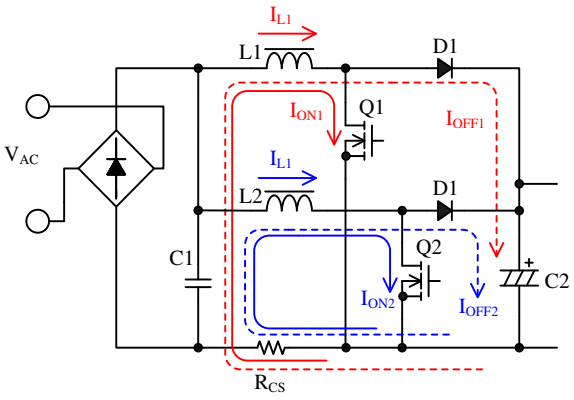


Figure 8-3 Two phase interleaved DCM PFC circuit

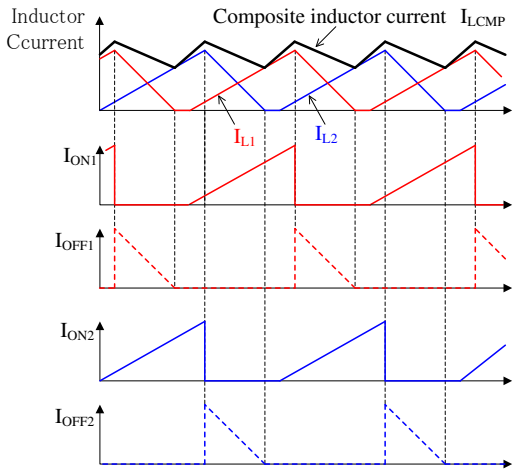


Figure 8-4 Operational waveform of two phase interleaved DCM

8.2 Startup Operation

The peripheral circuits around VCC pin and COMP pin is shown in Figure 8-5.

VCC pin is the external power supply for the IC. AC input voltage and the external voltage for VCC terminal are provided, and when following conditions are satisfied, the control circuit starts switching operation.

- FB pin voltage increases to more than $V_{FB(OLDH)}$ = 0.70 which is equivalent to about 20% of rated output voltage.
- VCC pin voltage increases to more than $V_{CC(ON)}$ = 11.6 V.

When VFB pin voltage decreases to $V_{FB(OLDL)}$ = 0.50 V or less, the control circuit stops switching operation and enters into the standby mode even if VCC pin voltage increases to $V_{CC(ON)}$ or more.

Figure 8-6 shows the operational waveform at startup. At startup, COMP pin is charged by $I_{COMP(SO)}$ = − 30 µA, and thus the output power increases gradually until VFB

pin voltage becomes 3.2V (corresponds to about 90% of rated output voltage). This Soft-start Function reduces the stress on power devices.

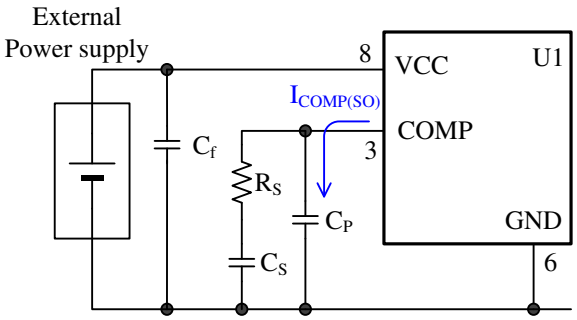


Figure 8-5 Peripheral circuit of VCC pin and COMP pin

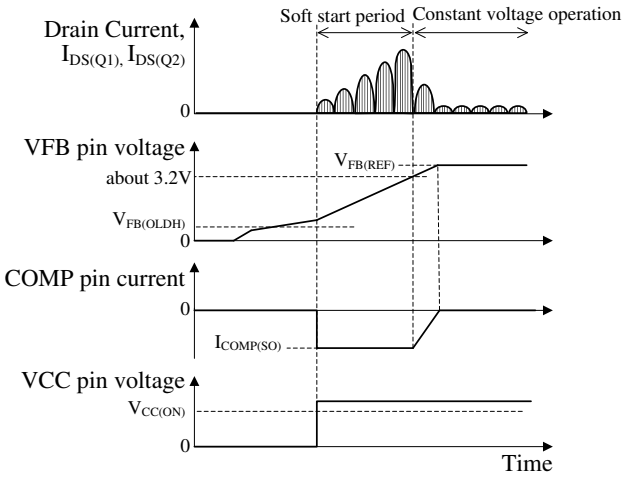


Figure 8-6 operational waveforms at startup

As shown in Figure 8-7, when VCC pin voltage decreases to $V_{CC(OFF)}$ = 10.6 V or less, the control circuit stops switching operation by UVLO (Undervoltage lockout) circuit, and reverts to the standby mode before startup.

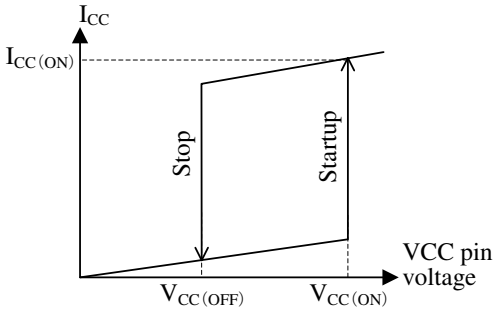


Figure 8-7 Relationship of VCC pin voltage and circuit current I_{CC}

8.3 Voltage Control Operation

The PFC circuit with a general single phase DCM is shown in Figure 8-8. The L1 current is detected by auxiliary winding D and the off time of MOSFET is controlled.

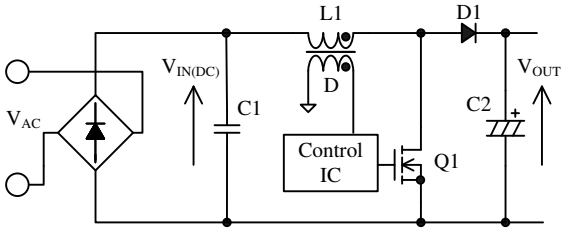


Figure 8-8 General current detection circuit of single phase PFC

In the boost PFC converter, the t_{ON} is a function of load power. In case of DCM, t_{OFF} is expressed as follows:

$$t_{OFF} > \frac{V_{IN(DC)}}{V_{OUT} - V_{IN(DC)}} \times t_{ON} \quad (8\text{-}1)$$

where,
$V_{IN(DC)}$: C1 voltage
V_{OUT}: Output voltage
t_{ON}: On time of MOSFET

Since the IC does not require the D winding for current detection, simple PFC circuit is achieved. Figure 8-9 shows the peripheral circuit of VIN pin, VFB pin and COMP pin.

The IC makes both t_{ON} and t_{OFF} internally using VIN pin voltage, FB pin voltage and COMP pin voltage.

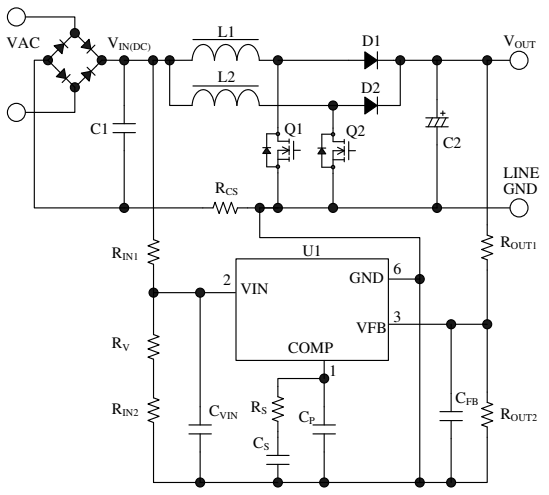


Figure 8-9 Peripheral circuit of VIN, VFB and COMP

t_{ON} is proportional to COMP pin voltage which depends on the output voltage. The maximum on time t_{ONMAX} = 20.7 μs is specified by V_{IN}= 0.5 V and V_{COMP}= 4V.

The maximum on time depends on VIN pin voltage. Figure 8-10 shows the typical relationship between VIN pin voltage and the maximum on time $t_{ONMAX(VIN)}$ (V_{COMP}= 4V).

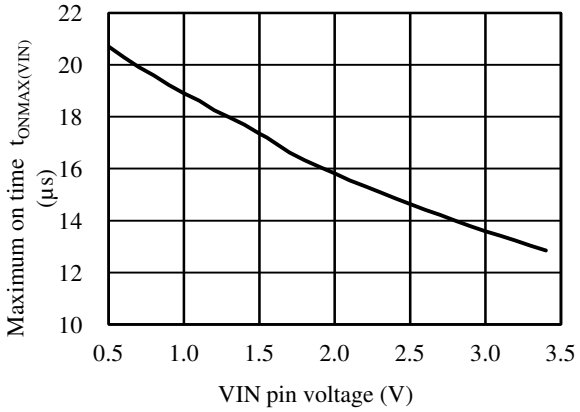


Figure 8-10 relation between VIN pin voltage and maximum on time (V_{COMP}= 4 V)

- **VIN Pin and VFB Pin Parameter Design**

  VIN pin detects input voltage and VFB pin detects output voltage. Since these voltages are used for internal calculation of off time, the voltage detection circuits should be well matched. Thus R_{IN1}、R_{IN2}、C_{VIN} values of the input portion should be equal to R_{OUT1}、R_{OUT2}、C_{FB} values of the output portion. R_{IN1} and R_{OUT1} are recommended the resistors in several hundreds kΩ to several MΩ range and anti-electromigration type, such as metal oxide film resistor. The variation in the value of R_{IN1}, R_{IN2}, R_{OUT1} and R_{OUT2} affect the accuracy of output voltage. Thus these resistors are recommended to be high accuracy type. As shown in Figure 8-9, resistor R_V is recommended to add for adjustment.C_{IN} and C_{FB} are for noise reduction. Capacitors of about 0.1 nF to 10 nF are recommended, if necessary.

  Since the dividers of input portion and output portion are designed to be equal, Equation(8-1) can be expressed as Equation(8-2) using VIN pin voltage and VFB voltage.

$$t_{OFF} > \frac{V_{IN}}{V_{FB} - V_{IN}} \times t_{ON} \qquad (8\text{-}2)$$

  where,
  V_{IN}: VIN pin voltage
  V_{FB}: FB pin voltage
  t_{ON}: On time of MOSFET

- **COMP Pin Parameter Design（Error Amplifier Phase Compensation）**

  COMP pin is the output of the internal error amplifier. The error amplifier system consists of a transconductance amplifier and switched current sources that implement the enhanced response functions. The phase compensation circuit is connected between COMP and GND COMP pins. This response is set below 20 Hz to maintain power factor correction at standard commercial power frequencies of 50 or 60 Hz.

  In Figure 8-9, the phase compensation components, C_P, C_S and R_S, are recommended as follows and may be adjusted to reduce ripple or to enhance transient load response at the output voltage.

  C_P: 0.047 μF to 0.47 μF
  C_S: 0.47 μF to 10 μF
  R_S: 10 kΩ to 100 kΩ

8.4 High Speed Response Function (HSR)

The boost PFC is input the sinusoidal waveform of AC input voltage with commercial frequency, and the voltage control has the characteristic of responding to low frequency. As a result, the dynamic load response becomes slow, and may cause the output voltage V_{OUT} to drop more easily.

High Speed Response Function (HSR) is built-in to reduce variation of the output voltage under dynamic load change conditions.

Figure 8-11 shows the operational waveform of HSR.

When VFB terminal voltage increases to $V_{FB(HSR)EN}$ = 3.4 V or more, the control circuit enables HSR operation.

After this, when VFB terminal voltage decreases to $V_{FB(HSR)AC}$ = 3.2 V or less due to dynamic load change conditions or others, the control circuit starts HSR operation. During this operation, COMP terminal is charged by $I_{COMP(SO)HSR}$ = − 100 μA and the output power increases until VFB pin voltage increases to 3.2 V. $V_{FB(HSR)AC}$ = 3.2 V is equivalent to about 91.4% of the rated output voltage, V_{OUT}.

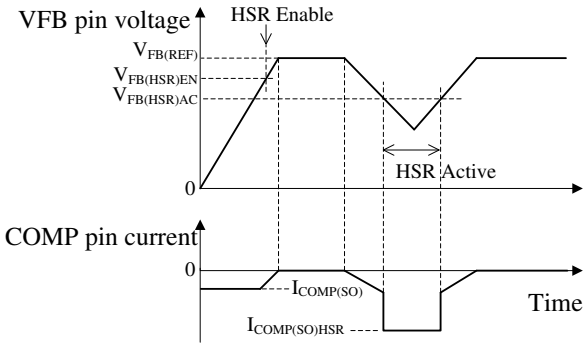


Figure 8-11 Operational waveform of HSR

8.5 Gate Drive

OUT1 pin and OUT2 pin are the gate drive pins for driving the external MOSFET directly. The specification is listed in Table 8-1.

Table 8-1 Current and Voltage specifications of OUT1pin and OUT2 pin

Parameter	Symbol	Rating
OUT1, OUT2 Pin Voltage (Low)	$V_{OUT(L)}$	0.3 V(max.)
OUT1, OUT2 Pin Voltage (High)	$V_{OUT(H)}$	10.2 V
OUT1, OUT2 Pin Peak Source Current	$I_{OUT(SO)}$	– 0.5 A
OUT1, OUT2 Pin Peak Source Current	$I_{OUT(SI)}$	0.5 A

Figure 8-12 shows the peripheral circuit of OUT1 and OUT2.

Resistors, R1, R2, R3 and R4 in Figure 8-12 should be adjusted for actual operation because these values relate to the board layout patterns and power MOSFET capacitances.

The gate resistors R1 and R3 are recommended in several to several tens of Ω range, and should be adjusted to reduce gate voltage ringing and EMI noise.

R2 and R4 help to prevent malfunctions caused by steep dV/dt during power MOSFET turns off. The recommended values are in the 10k to 100kΩ range, and should be placed close to power MOSFET's gate and source terminals.

Power MOSFET should be selected so that these $V_{GS(th)}$ threshold voltages are less than $V_{OUT(H)}$ enough over entire operating temperature range.

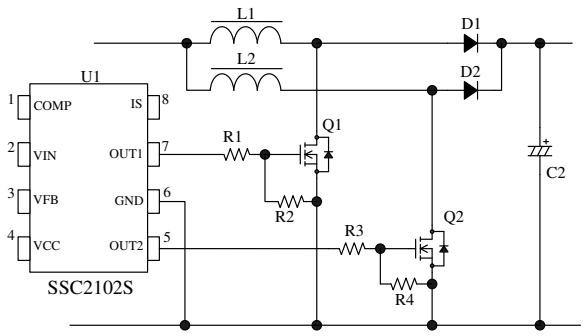


Figure 8-12 Peripheral circuit of OUT1 pin and OUT2 pin

8.6 Overcurrent Protection (OCP)

Figure 8-13 shows IS pin peripheral circuit. The Overcurrent Protection (OCP) detects the inductor current of both L1 and L2 by using current detection resistor R_{CS}. The voltage of both ends of R_{CS} is induced into IS pin

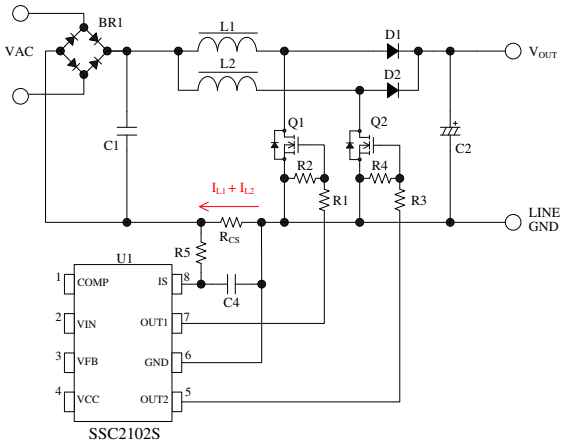


Figure 8-13 Peripheral circuit of IS pin

There are two threshold voltages, $V_{IS(OCPL)}$ and $V_{IS(OCPH)}$ in OCP operation. The details are as follows.

- **IS Pin Overcurrent Protection Threshold Voltage (Low) : $V_{IS(OCPL)}$**
  When the inductor current increases and IS terminal voltage decreases to $V_{IS(OCPL)}$ = − 0.42 V, control circuit turns off the external power MOSFET. The control is different depending on the state of V_{OUT1} and V_{OUT2}.

  1) When either V_{OUT1} or V_{OUT2} is High, the output, which is set High, is set to Low as shown in Figure 8-14.

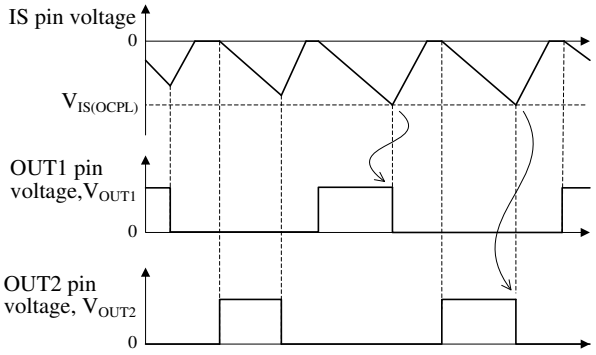


Figure 8-14 OCP operation by $V_{IS(OCPL)}$ (either V_{OUT1} or V_{OUT2} is high)

2) When both V_{OUT1} and V_{OUT2} are High, the output which is set to High ahead is set to Low as shown in Figure 8-15。.

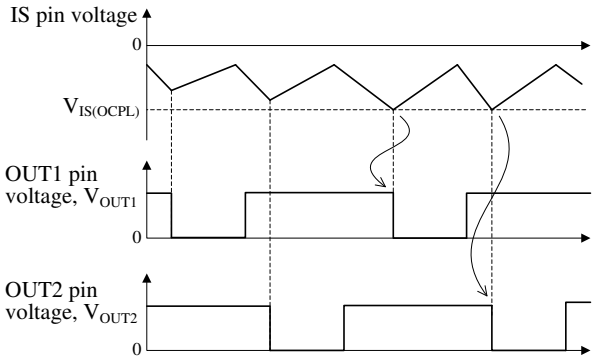


Figure 8-15 OCP operation by $V_{IS(OCPL)}$
(Both V_{OUT1} and V_{OUT2} are High)

- **IS Pin Overcurrent Protection Threshold Voltage (High) : $V_{IS(OCPH)}$**
  This protection operates on such abnormal conditions as the inductor is shorted or is saturated. When the inductor current of L1 and L2 increases abnormally and IS terminal voltage decreases to $V_{IS(OCPH)} = -0.55$ V or less, the control circuit sets both V_{OUT1} and V_{OUT2} to Low on pulse-by-pulse basis as shown in Figure 8-16.

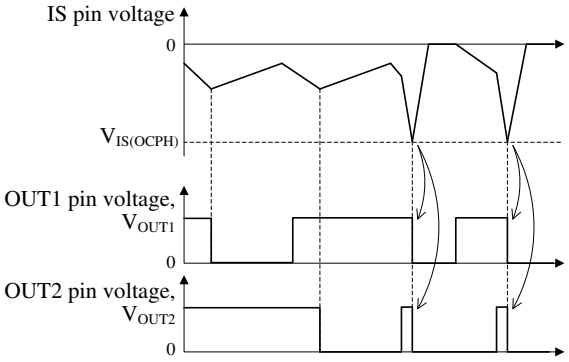


Figure 8-16 OCP operation by $V_{IS(OCPH)}$

8.7 Overvoltage Protection (OVP)

Figure 8-17 shows VFB pin peripheral circuit and Figure 8-18 shows the operational waveforms of Overvoltage Protection (OVP).

The output overvoltage is detected by using VFB pin. There are two threshold voltages, $V_{FB(SOVP)}$ for Soft Overvoltage Protection (SOVP) and $V_{FB(OVP)}$ for OVP. The operations are shown below.

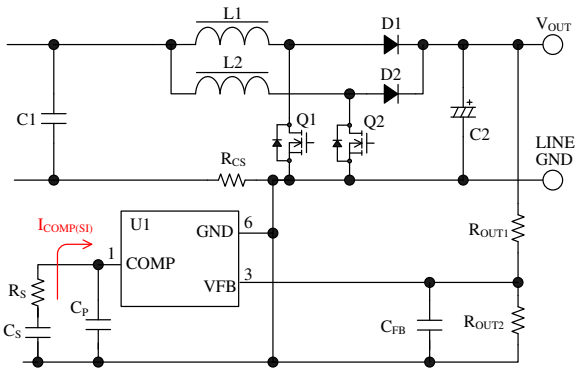


Figure 8-17 VFB pin peripheral circuit

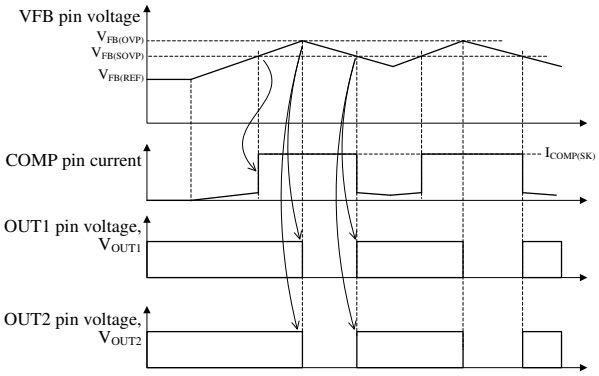


Figure 8-18 Operational waveform of OVP

- **Soft Overvoltage Protection (SOVP)**
  When VFB pin voltage increases to $V_{FB(SOVP)}$ = 3.68 V, Soft Overvoltage Protection (SOVP) is activated. Thus, COMP pin is discharged by $I_{COMP(SI)}$ = 100 µA and the output voltage is decreased.
  $V_{FB(SOVP)}$ is equivalent to about 105% of the rated output voltage. The output voltage, which operates SOVP, is calculated approximately as follows.

$$V_{OUT(SOVP)} = \frac{V_{OUT}}{V_{FB(REF)}} \times V_{FB(SOVP)} \quad (V) \qquad (8\text{-}3)$$

where,
V_{OUT} : Output voltage in normal operatioin
$V_{FB(REF)}$: Error AMP reference voltage, 3.5 V

- **Overvoltage Protection (OVP)**
  When VFB pin voltage increases to $V_{FB(OVP)}$ = 3.72 V, Overvoltage Protection (OVP) is activated. And thus both OUT1 and OUT2 are set to Low. When VFB pin voltage decreases to $V_{FB(SOVP)}$, the control circuit deactivate both OVP and SOVP, and reverts to switching operation. $V_{FB(OVP)}$ is equivalent to about 106 % of the rated output voltage. The output voltage, which operates OVP, is calculated approximately as follows.

$$V_{OUT(OVP)} = \frac{V_{OUT}}{V_{FB(REF)}} \times V_{FB(OVP)} \quad (V) \qquad (8\text{-}4)$$

where,

V_{OUT} : Output voltage in normal operatioin

$V_{FB(REF)}$: Error AMP reference voltage, 3.5 V

8.8 Open Loop Detection (OLD)

Figure 8-19 shows VFB pin peripheral circuit.

The Open Loop Detection (OLD) is activated when the output voltage detection resistor R_{OUT1} is open.

In case the R_{OUT1} becomes open in normal operation, VFB pin voltage starts to decrease. When VFB pin voltage decreases to $V_{FB(OLDL)}$ = 0.50 V, the IC stops switching operation.

When VFB pin voltage increases to $V_{FB(OLDH)}$ = 0.70 V or more, the control circuit starts switching operation. $V_{FB(OLDH)}$ is equivalent to about 20% of the rated output voltage.

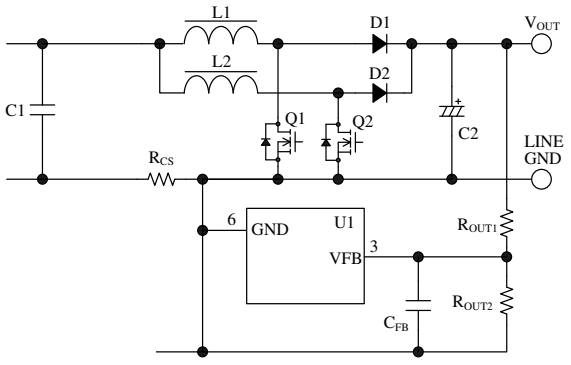


Figure 8-19 VFB pin peripheral circuit

8.9 Open Pin Protection (OPP)

VFB, IS and VIN pins have Open Pin Protection (OPP) internally.

These pins are internally connected with pull-up current sources. In case the pins are open, each pin voltage is pulled up to each internal supply voltage. The protection operations are as follows.

- VFB pin Open: VFB pin voltage increases and the Overvoltage Protection (OVP) is activated. Thus, both OUT1 and OUT2 are set to Low.
- IS pin Open: IS pin voltage increases and Overcurrent Protection (OCP) is activated. Thus, both OUT1 and OUT2 are set to Low.
- VIN pin Open: VIN pin voltage increases and the control circuit limits its operation, or stops.

8.10 Input Undervoltage Protection (UVP)

Input voltage is detected by VIN pin. When input voltage decreases due to the instantaneous power interruption etc., Input Undervoltage Protection (UVP) is activated. Figure 8-20 shows the operational waveforms.

When input voltage decrease and the VIN pin voltage decreases to $V_{IN(P)}$ = 0.3 V or more for the internal setting delay time, t_{VIN} = 14 ms or more, the High Speed Response Function (HSR) (refer to Section 8.4) is disabled, the capacitor connected to COMP pin is discharged by $I_{COMP(SI)}$ and COMP pin voltage is nearly zero.

After instantaneous power failure, input voltage increases and VIN pin voltage increase to $V_{IN(P)}$ or more, output power is increased slowly by Soft-start Function (refer to Section 8.2) in order to reduce the stress on power devices.

Since the over current is inhibited by UVP at return from instantaneous power failure, output voltage can increase again smoothly.

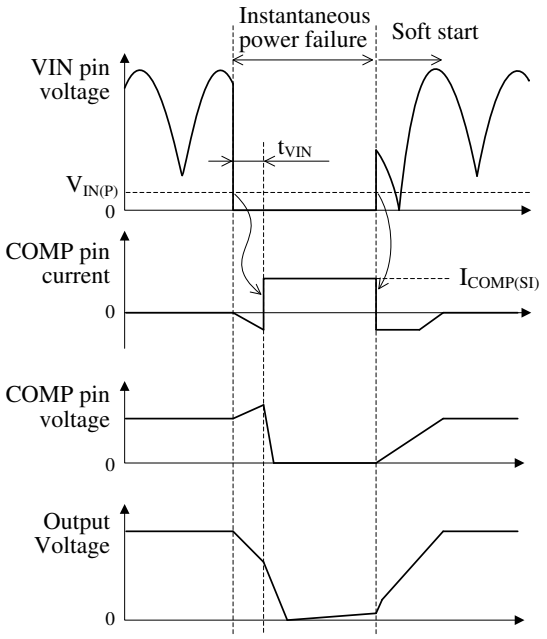


Figure 8-20 the instantaneous power failure operationwaveform

8.11 Thermal Shutdown (TSD)

When the temperature of the IC increases to T_{jTSDH} = 150 °C (min.) or more, the control circuit stops switching operation. Conversely, when that decreases to T_{jTSDL} = 140 °C (min.) or less, the control circuit starts switching operation.

9. Parameters Design

- Symbols in this section are defined as follows.
  P_O: PFC Output power per phase (W)
  η: PFC Efficiency
  t_{ON}: On time (s)
  $V_{INRMS(MIN)}$: Minimum input RMS voltage (V)
  $V_{INRMS(MAX)}$: Maximum input RMS voltage (V)
  V_{OUT}: PFC output voltage (V)
  I_{INRMS}: Input RMS current (A)

- The symbols of components are defined as shown in Figure 9-1.

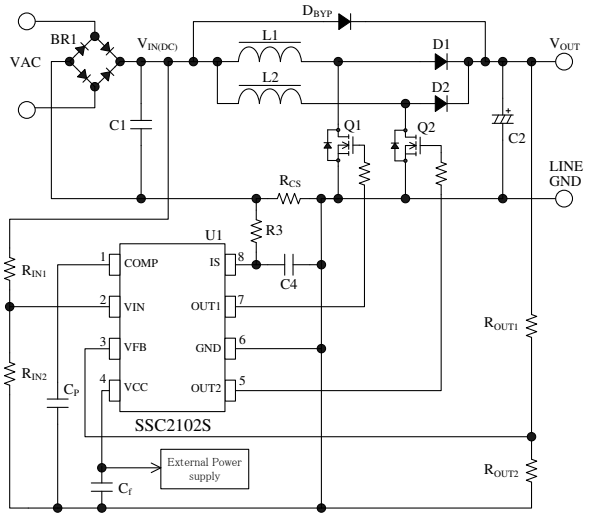


Figure 9-1 IC peripheral circuit

9.1 Inductor Design

Inductor is designed as follows.

(1) Setting of Output Voltage, V_{OUT}

At farst, output voltage of PFC should be set. Input voltage must always be lower than output voltage in a boost converter. Generally, output voltage, V_{OUT}, is set to at least 10 V higher than the peak voltage of the maximum commercial AC input voltage.

$$V_{OUT} \geq \sqrt{2} \times V_{INRMS(MAX)} + 10 \quad (V) \qquad (9\text{-}1)$$

(2) Calculation of Maximum Inductor Peak Current (per phase)

The waveform of the inductor current is triangular. The maximum peak current, $I_{LPEAK(MAX)}$, running through each inductor is calculated as follows.

- **Calculation of Maximum Input Power**
  Maximum input power, $P_{IN(MAX)}$ is calculated as follows.

$$P_{IN(MAX)} = \frac{K_{OM} \times K_{LM} \times P_O}{\eta} \quad (W) \qquad (9\text{-}2)$$

Where,
K_{OM}: Coefficient of the output power margin
K_{LM}: Coefficient of the inductor saturation margin
η: PFC Efficiency

The values of K_{OM} and K_{LM} are generally in the range of 1.2 to 1.3. η depends on the ON-resistance, $R_{DS(ON)}$, of the power MOSFET and the forward voltage, V_F of the rectifier diode. η is generally in the range of 0.90 to 0.97.

- **Calculation of Maximum Inductor Peak Current**
  Maximum inductor peak current, $I_{LPEAK(MAX)}$ is calculated using the above results and Equation (9-3).

$$I_{LPEAK(MAX)} = \frac{2\sqrt{2} \times P_{IN(MAX)}}{V_{INRMS(MIN)}} \quad (A) \qquad (9\text{-}3)$$

(3) Calculation of Maximum On Time

The IC makes both on time and off time internally using VIN pin voltage, FB pin voltage and COMP pin voltage. Maximum on time is calculated as follows.

- **Calculation of VIN pin voltage, V_{IN}**
  Defining the VIN pin voltage as V_{IN} and the voltage of C2 as $V_{IN(DC)}$, The relationship between $V_{IN(DC)}$ and input detection resistors, R_{IN1} and R_{IN2} is as follows.

$$\frac{R_{IN1} + R_{IN2}}{R_{IN2}} = \frac{V_{IN(DC)}}{V_{IN}} \qquad (9\text{-}4)$$

The relationship between output voltage, V_{OUT} and output detection resistors, R_{OUT1} and R_{OUT2} is as follows.

$$\frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}} = \frac{V_{OUT}}{V_{FB(REF)}} \qquad (9\text{-}5)$$

The values of R_{IN1} and R_{IN2} should be equal to the values of R_{OUT1} and R_{OUT2}.
From Equation (9-4) and Equation (9-5), V_{IN} is calculated as follows.

$$\frac{V_{IN(DC)}}{V_{IN}} = \frac{V_{OUT}}{V_{FB(REF)}}$$

$$\Rightarrow \quad V_{IN} = \frac{V_{IN(DC)} \times V_{FB(REF)}}{V_{OUT}} \quad (V)$$

In case of minimum AC input voltage, on time becomes maximum. V_{IN} at maximum on time is calculated as follows.

$$V_{IN} = \frac{\sqrt{2} \times V_{INRMS(MIN)} \times V_{FB(REF)}}{V_{OUT}} \quad (V) \qquad (9\text{-}6)$$

- Maximum on time
  Maximum on time depends on VIN pin voltage as shown in Figure 8-10 (Section 8.2). Maximum on time can be gotten from result of Esuation (9-6) and Figure 8-10.

(4) Calculation of Inductance value for a single phase.
The maximum inductance for a single phase, L_{MAX} is calculated as follows using the results of (2) and (3).

$$L_{MAX} = \frac{\sqrt{2} \times V_{INRMS(MIN)} \times t_{ONMAX(VIN)}}{I_{LPEAK(MAX)}} \quad (H) \qquad (9\text{-}7)$$

(5) Calculation of Inductor Turns
The turns number of inductor, N is calculated as follows using the results of (2) and (4).

$$N = \frac{I_{LPEAK(MAX)} \times L_{MAX}}{Ae \times \Delta B_{MAX}} \quad (turns) \qquad (9\text{-}8)$$

where,
Ae : the effective area of inductor core (m^2)
ΔB_{MAX} : maximum magnetic flux density (T)

< Inductor Design Example >
Inductor design examle is shown below. The specifications of power suply are as follows.
$V_{INRMS(MIN)}$ = 85V
$V_{INRMS(MAX)}$ = 265V
P_O = 150 W for each phase
(Total output power of two phase Interleaved PFC = 300 W)

(1) Setting of Output Voltage, V_{OUT}

$$V_{OUT} \geq \sqrt{2} \times V_{INRMS(MAX)} + 10$$

$$\geq \sqrt{2} \times 265 + 10 \approx 385(V)$$

hence, V_{OUT} is set to 390 V(DC)

(2) Calculation of $I_{LPEAK(MAX)}$
In case K_{OM} = 1.2, K_{LM} = 1.2, η = 0.92 and $V_{INRMS(MIN)}$ = 85 V, the maximum input power for a single phase is calculated as follows.

$$P_{IN(MAX)} = \frac{K_{OM} \times K_{LM} \times P_O}{\eta}$$

$$= \frac{1.2 \times 1.2 \times 150}{0.92} \approx 235(W)$$

Then the maximum peak inductor current for a single phase is calculated as follows.

$$I_{LPEAK(MAX)} = \frac{2\sqrt{2} \times P_{IN(MAX)}}{V_{INRMS(MIN)}}$$

$$= \frac{2\sqrt{2} \times 235}{85} \approx 7.8(A)$$

(3) Calculation of $t_{ONMAX(VIN)}$
Using $V_{FB(REF)}$ = 3.5 V(typ.) and the result of (1), V_{IN} is calculated as follows.

$$V_{IN} = \frac{\sqrt{2} \times V_{INRMS(MIN)} \times V_{FB(REF)}}{V_{OUT}}$$

$$= \frac{\sqrt{2} \times 85 \times 3.5}{390} = 1.08(V)$$

The relation in Figure 8-10 shows $t_{ONMAX(VIN)}$ at V_{IN} = 1.08 V is about 18.6 µs.

(4) Using the results of (2) and (3)

$$L_{MAX} = \frac{\sqrt{2} \times V_{INRMS(MIN)} \times t_{ONMAX(VIN)}}{I_{LPEAK(MAX)}}$$

$$= \frac{\sqrt{2} \times 85 \times 18.6 \times 10^{-6}}{7.8}$$

$$\approx 286 \times 10^{-6}(H)$$

(5) When Ae is 102 mm^2 and ΔB_{MAX} is 250 mT, N is calculated as follows using the results of (2) and (4).

$$N = \frac{I_{LPEAK(MAX)} \times L_{MAX}}{Ae \times \Delta B_{MAX}}$$

$$= \frac{7.8 \times 286 \times 10^{-6}}{102 \times 10^{-6} \times 0.25}$$

$$\approx 87(turns)$$

9.2 Overcurrent Detection Resistor, R_{CS}

Overcurrent detection resistor, R_{CS}, detects the composite inductor current of both converters.

As the peak value of composite inductor current varies by ON-duty $D_{ON(MAX)}$, the coefficient defined as K_R is calculated from its $D_{ON(MAX)}$ and R_{CS} is calculated by I_{LCMP}.

(1) Calculation of Maximum ON-duty $D_{ON(MAX)}$

$D_{ON(MAX)}$ is calculated as follows using V_{OUT} derived in Section 9.1 (1).

$$D_{ON(MAX)} = \frac{V_{OUT} - \sqrt{2} \times V_{INRMS(MIN)}}{V_{OUT}} \quad (9\text{-}9)$$

(2) Calculation of Inductor Current Coefficient, K_R

From the result of (1),

- When $D_{ON(MAX)} \geq 0.5$

$$K_R = 1 + \frac{D_{ON(MAX)} - 0.5}{D_{ON(MAX)}} \quad (9\text{-}10)$$

- When $D_{ON(MAX)} < 0.5$

$$K_R = 1 + \frac{0.5 - D_{ON(MAX)}}{1 - D_{ON(MAX)}} \quad (9\text{-}11)$$

(3) Calculation of Composite Inductor Current, $I_{LCMP(MAX)}$

Using the result of (2), $I_{LCMP(MAX)}$ is calculated as follows.

$$I_{LCMP(MAX)} = K_R \times \frac{2\sqrt{2} \times K_{OM} \times P_O}{\eta \times V_{INRMS(MIN)}} \ (A) \quad (9\text{-}12)$$

where,

K_{OM} : Output power margin coefficient

P_O : Output power for a single phase (W)

η : PFC efficiency

Generally, K_{OM} is the range of 1.2 to 1.3. η depends on the ON-resistance, $R_{DS(ON)}$, of the power MOSFET and the forward voltage, V_F of the rectifier diode. η is generally in the range of 0.90 to 0.97.

(4) Calculation of Over Current Detection Resistor, R_{CS}

Using the result of (3), R_{CS} is calculated as follows.

$$R_{CS} = \frac{|V_{IS(OCPL)}|}{I_{LCMP(MAX)}} \ (\Omega) \quad (9\text{-}13)$$

where,

$V_{IS(OCPL)}$: IS Pin Overcurrent Protection Threshold Voltage (Low) is − 0.42 V(typ.)

<R_{CS} Design Example>

R_{CS} design example is shown below. The specifications of power suply are as follows.

$V_{INRMS(MIN)}$ = 85V

$V_{INRMS(MAX)}$ = 265V

P_O = 150 W for each phase

(Total output power of two phase Interleaved PFC = 300 W)

Output Voltage: V_{OUT} = 390 V

(1) Calculation of $D_{ON(MAX)}$

$$D_{ON(MAX)} = \frac{V_{OUT} - \sqrt{2} \times V_{INRMS(MIN)}}{V_{OUT}}$$

$$= \frac{390 - \sqrt{2} \times 85}{390} \approx 0.69$$

(2) Calculation of K_R

Using the the result of (1) and Equation (9-10), K_R is calculated as follows.

$$K_R = 1 + \frac{D_{ON(MAX)} - 0.5}{D_{ON(MAX)}}$$

$$= 1 + \frac{0.69 - 0.5}{0.69} \approx 1.28$$

(3) Calculation of $I_{LCMP(MAX)}$

$$I_{LCMP(MAX)} = K_R \times \frac{2\sqrt{2} \times K_{OM} \times P_O}{\eta \times V_{INRMS(MIN)}}$$

$$= 1.28 \times \frac{2\sqrt{2} \times 1.2 \times 150}{0.92 \times 85} \approx 8.3(A)$$

(4) Calculation of R_{CS}

Using the result of (3), R_{CS} is calculated as follwos.

$$R_{CS} = \frac{|V_{IS(OCPL)}|}{I_{LCMP(MAX)}}$$

$$= \frac{|-0.42|}{8.3} \approx 0.05(\Omega)$$

10. Design Notes

10.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components. Figure 10-1 shows the IC peripheral circuit.

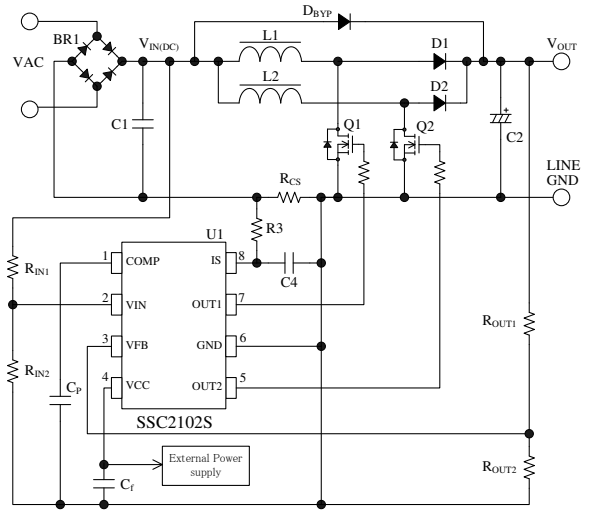


Figure 10-1 The IC peripheral circuit.

- **High Resistance and High Voltage Applied Resistor, R_{IN1} and R_{OUT1}**
  Since R_{IN1} and R_{OUT1} have applied high voltage and have high resistance value, R_{IN1} and R_{OUT1} should be selected from resistors designed against electromigration or use a combination of resistors for that.

- **Current Detection Resistor, R_{CS}**
  R_{CS} is the resistor for the current detection. A high frequency switching current flows to R_{CS}, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and high surge-tolerant type.

- **Boost Diode, D1 and D2**
  Choose a boost diode having proper margin of a peak reverse voltage V_{RSM} against output voltage V_{OUT}.
  A fast recovery diode is recommended to reduce the switching noise and loss. Please ask our staff about our lineup. The size of heat sink is chosen taking into account some loss by V_F and recovery current of boost diode.

- **Bypass Diode, D_{BYP}**
  Bypass diode protects the boost diode from a large current such as an inrush current. A high surge current tolerance diode is recommended. Please ask our staff about our lineup.

- **Output Electrolytic Capacitor, C2**
  Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

- **Inductor, L1 and L2**
  Apply proper design margin to temperature rise by core loss and copper loss.

10.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 10-2 shows the circuit design example.

(1) Main Circuit Trace Layout
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

(2) Control Ground Trace Layout
Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 10-2 as close to the R_{CS} pin as possible.

(3) R_{CS} Trace Layout
R_{CS} should be placed as close as possible to the Source pin and the IS pin.
The peripheral components of IS pin should be connected by dedicated pattern from root of R_{CS}.
The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 10-2) which is close to the base of R_{CS}.

(4) Peripheral Component of IC
The components for control connected to the IC should be placed as close as possible to the IC, and should be connected as short as possible to the each pin.

(5) Gate Resistor (R2 and R4) Trace Layout
Gate resistor should be connected as short as possible to the Source pin and Gate pin of each MOSFET.

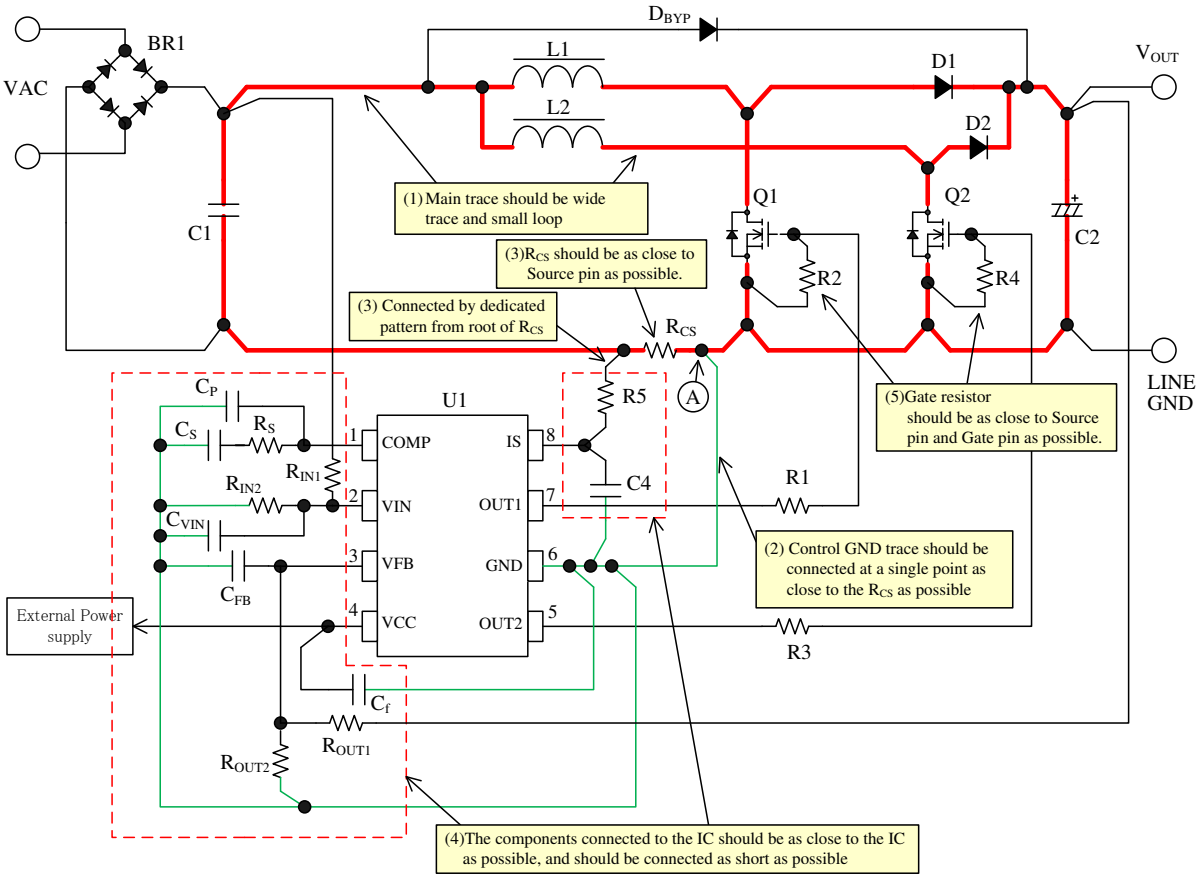


Figure 10-2 Example of connection of peripheral component

OPERATING PRECAUTIONS

In the case that you use Sanken products or design your products by using Sanken products, the reliability largely depends on the degree of derating to be made to the rated values. Derating may be interpreted as a case that an operation range is set by derating the load from each rated value or surge voltage or noise is considered for derating in order to assure or improve the reliability. In general, derating factors include electric stresses such as electric voltage, electric current, electric power etc., environmental stresses such as ambient temperature, humidity etc. and thermal stress caused due to self-heating of semiconductor products. For these stresses, instantaneous values, maximum values and minimum values must be taken into consideration. In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature affects the reliability significantly.

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5 to 35°C) and the standard relative humidity (around 40 to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of the products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between the product pins, and wrong connections. Ensure all test parameters are within the ratings specified by Sanken for the products.

Soldering

- When soldering the products, please be sure to minimize the working time, within the following limits:
  - 260 ± 5 °C 10 ± 1 s (Flow, 2 times)
  - 380 ± 10 °C 3.5 ± 0.5 s (Soldering iron, 1 time)

Electrostatic Discharge

- When handling the products, the operator must be grounded. Grounded wrist straps worn should have at least 1MΩ of resistance from the operator to ground to prevent shock hazard, and it should be placed near the operator.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in order to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in Sanken shipping containers or conductive containers, or be wrapped in aluminum foil.

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