iMOTION™

High Performance Sensorless Motor Control IC

Description

IRMCK182M is a high performance One Time Programmable ROM based motion control IC designed primarily for appliance applications which contains two computation engines integrated into one monolithic chip. One is the Flexible Motion Control Engine (MCE™) for sensorless control of permanent magnet motors or induction motors; the other is an 8-bit high-speed microcontroller (8051). The user can program a motion control algorithm by connecting these control elements using a graphic compiler. Key components of the complex sensorless control algorithms, such as the Angle Estimator, are provided as complete pre-defined control blocks. A unique analog/digital circuit and algorithm fully supports single shunt or leg shunt current reconstruction. IRMCK182M comes in a 32 pin QFN 5x5 package.

Features

- MCE™ (Flexible Motion Control Engine) - Dedicated computation engine for high efficiency sinusoidal sensorless motor control
- Built-in hardware peripheral for single or two shunt current feedback reconstruction and analog circuits
- Embedded 8-bit high speed microcontroller (8051) for flexible I/O and man-machine control
- JTAG programming port for emulation/debugger
- Serial communication interface (UART)
- Watchdog timer with independent internal clock
- Internal 32Kbyte OTP ROM
- 3.3V single supply

Product Summary

Maximum clock input (fcrystal)	60 MHz
Maximum Internal clock (SYSCLK)	128MHz
Maximum 8051 clock (8051CLK)	32MHz
MCE™ computation data range	16 bit signed
8051/MCE Data RAM	2KB
MCE Program RAM	12KB
PWM carrier frequency	20 bits/ SYSCLK
A/D input channels	4
A/D converter resolution	12 bits
A/D converter conversion speed	2 µsec
Analog output (PWM) resolution	8 bits
UART baud rate (typ)	57.6 Kbps
Number of digital I/O (max)	7
Package (lead free)	QFN32
Maximum 3.3V operating current	60mA

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRMCK182M	QFN32	Tape and Reel	3000	IRMCK182MTR
		Tray	3120	IRMCK182MTY

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1 Overview

IRMCK182M is a new generation International Rectifier integrated circuit device primarily designed as a one-chip solution for complete inverter controlled appliance motor control applications. Unlike a traditional microcontroller or DSP, the IRMCK182M provides a built-in closed loop sensorless control algorithm using the unique flexible Motion Control Engine (MCE™) for permanent magnet motors as well as induction motors. The MCE™ consists of a collection of control elements, motion peripherals; a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCK182M also employs a unique single shunt current reconstruction circuit in addition to two leg shunt current sensing circuit to eliminate additional analog/digital circuitry and enables a direct shunt resistor interface to the IC. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink™ development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging tools. Figure 1 shows a typical application schematic using the IRMCK182M.

IRMCK182M contains 32K bytes of OTP program ROM, and comes in a 32-pin QFN package.

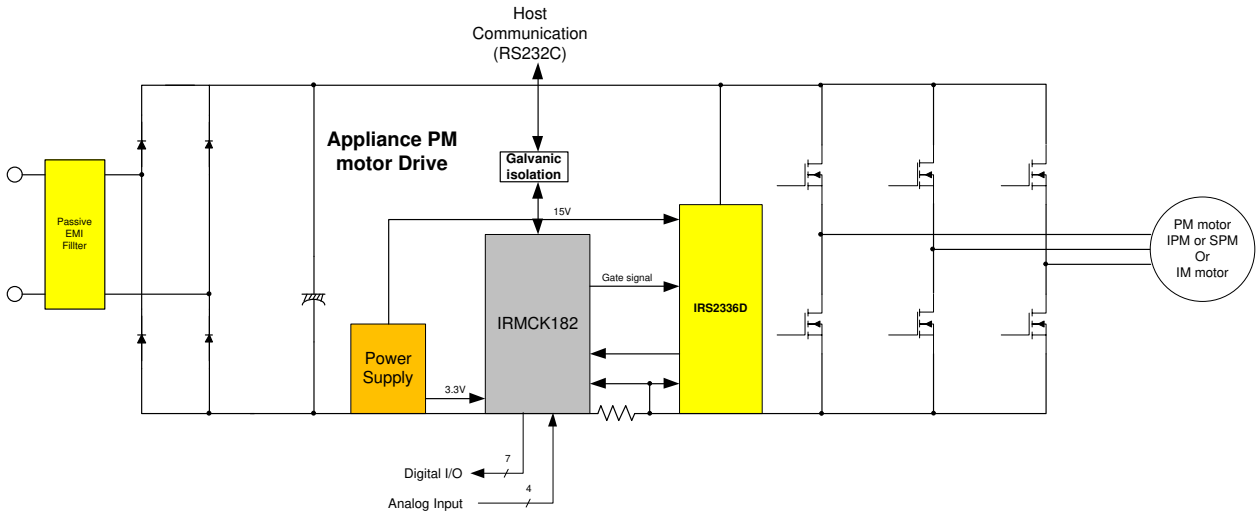


Figure 1 Typical Application Block Diagram Using IRMCK182M

2 Pinout

Pin out shown is based on QFN 5x5 32 pin package.

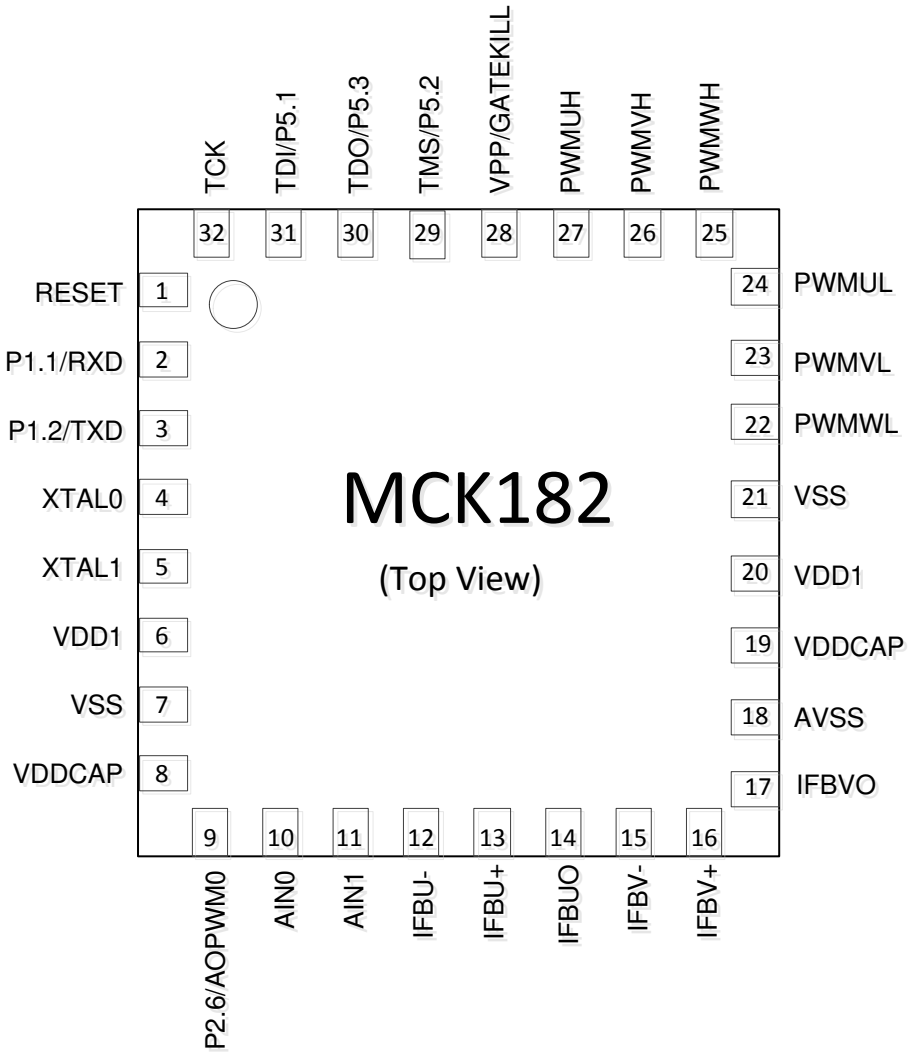


Figure 2 Pinout of IRMCK182M

3 IRMCK182M Block Diagram and Main Functions

IRMCK182M block diagram is shown in Figure 3.

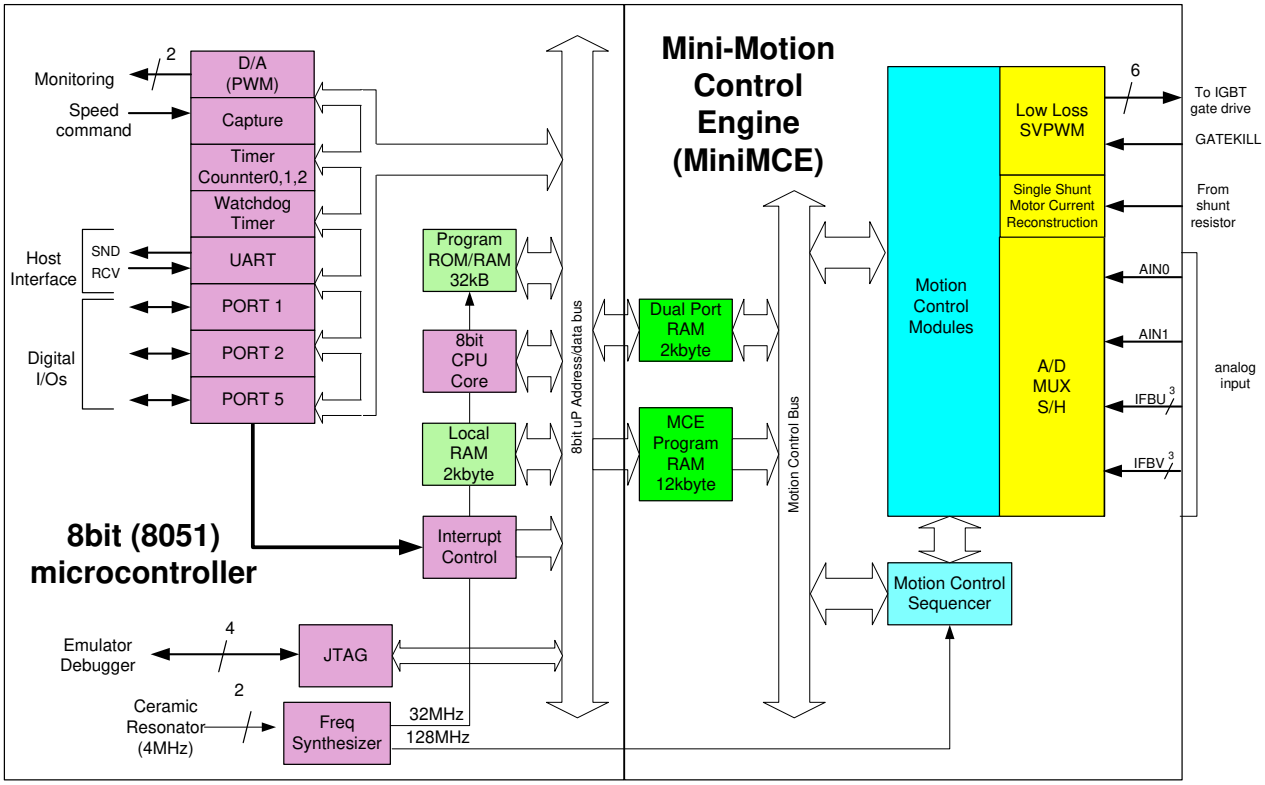


Figure 3 IRMCK182M Block Diagram

IRMCK182M contains the following functions for sensorless AC motor control applications:

- Motion Control Engine (MCE™)
  - Sensorless FOC (complete sensorless field oriented control)
  - Proportional plus Integral block
  - Low pass filter
  - Differentiator and lag (high pass filter)
  - Ramp
  - Limit
  - Angle estimate (sensorless control)
  - Inverse Clark transformation
  - Vector rotator
  - Bit latch
  - Peak detect

  - Transition
  - Multiply-divide (signed and unsigned)
  - Divide (signed and unsigned)
  - Adder
  - Subtractor
  - Comparator
  - Counter
  - Accumulator
  - Switch
  - Shift
  - ATAN (arc tangent)
  - Function block (any curve fitting, nonlinear function)
  - 16 bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)
  - MCE™ program memory and dual port RAM (max 12K+2k byte)
  - MCE™ control sequencer
- 8051 microcontroller
  - Two 16 bit timer/counters
  - One 16 bit periodic timer
  - One 16 bit watchdog timer
  - One 16 bit capture timer
  - Up to 7 discrete I/Os
  - 4 channel 12 bit A/D
    - Buffered (current sensing) two channels (0 – 1.2V input)
    - Unbuffered two channels (0 – 1.2V input)
  - JTAG port (4 pins)
  - Up to three channels of analog output (8 bit PWM)
  - UART
  - 32K byte OTP program ROM
  - 2K byte data RAM

4 Application connection and Pin function

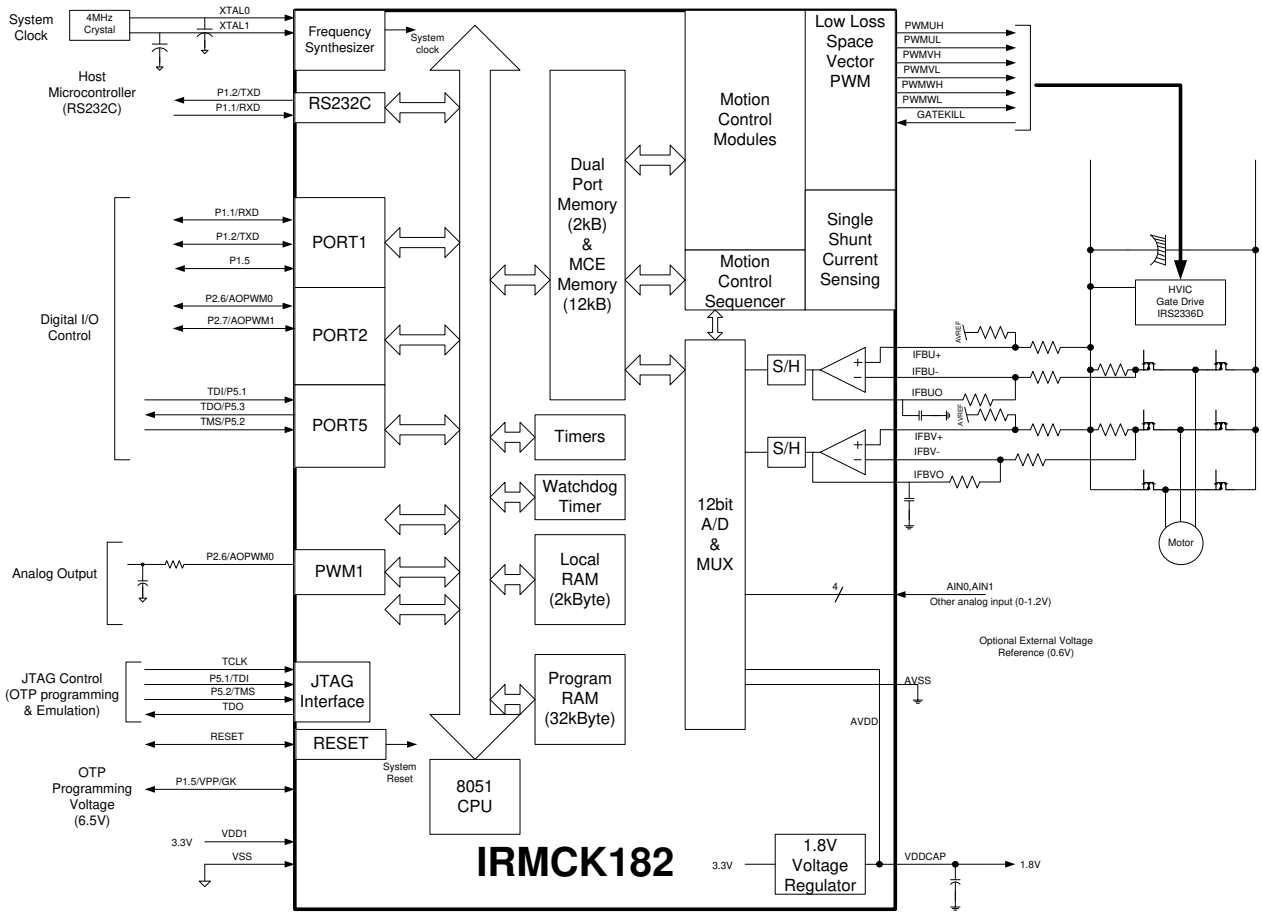


Figure 4 IRMCK182M Connection Diagram

4.1 8051 Peripheral Interface Group

UART Interface

P1.2/TXD	Output, Transmit data from IRMCK182M
P1.1/RXD	Input, Receive data to IRMCK182M

Discrete I/O Interface

P1.1/RXD	Input/output port 1.1, can be configured as RXD input
P1.2/TXD	Input/output port 1.2, can be configured as TXD output
VPP/GK	OTP programming voltage, or GATEKILL input
P2.6/AOPWM0	Input/output port 2.6, can be configured as AOPWM0 output
P2.7/AOPWM1	Input/output port 2.7, can be configured as AOPWM1 output
P5.1/TDI	Input port 5.1, configured as JTAG port by default
P5.2/TMS	Input port 5.2, configured as JTAG port by default

Analog Output Interface

P2.6/AOPWM0	Input/output, can be configured as 8-bit PWM output 0 with programmable carrier frequency
P2.7/AOPWM1	Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency

Crystal Interface

XTAL0	Input, connected to crystal
XTAL1	Output, connected to crystal

Reset Interface

RESET	Input and Output, system reset, doesn't require external RC time constant

4.2 Motion Peripheral Interface Group

PWM

PWMUH	Output, PWM phase U high side gate signal, internally pulled down by 58kΩ
PWMUL	Output, PWM phase U low side gate signal, internally pulled down by 58kΩ
PWMVH	Output, PWM phase V high side gate signal, internally pulled down by 58kΩ
PWMVL	Output, PWM phase V low side gate signal, internally pulled down by 58kΩ
PWMWH	Output, PWM phase W high side gate signal, internally pulled down by 58kΩ
PWMWL	Output, PWM phase W low side gate signal, internally pulled down by 58kΩ

Fault

GATEKILL	Input, upon assertion, this negates all six PWM signals, active low, internally pulled up by 70kΩ

4.3 Analog Interface Group

AVSS	Analog power return, (analog internal 1.8V power is shared with VDDCAP)
IFBU+	Input, Operational amplifier positive input for single or U-phase leg shunt resistor current sensing
IFBU-	Input, Operational amplifier negative input for single or U-phase leg shunt shunt resistor current sensing
IFBUO	Output, Operational amplifier output for single or U-phase leg shunt shunt resistor current sensing
IFBV+	Input, Operational amplifier positive input for V-phase leg shunt resistor current sensing
IFBV-	Input, Operational amplifier negative input for V-phase leg shunt shunt resistor current sensing
IFBVO	Output, Operational amplifier output for V-phase leg shunt shunt resistor current sensing
AIN0	Input, Analog input channel 0 (0 – 1.2V), typically configured for DC bus voltage input
AIN1	Input, Analog input channel 1 (0 – 1.2V), needs to be pulled down to AVSS if unused

4.4 Power Interface Group

VDD1	Digital power (3.3V)
VDDCAP	Internal 1.8V output, requires capacitors to the pin. Shared with analog power pad internally **Note:** The internal 1.8V supply is not designed to power any external circuits or devices. Only capacitors should be connected to this pin.
VSS	Digital common

4.5 Test Interface Group

P5.2/TMS	JTAG test mode input or input/output digital port
TDO	JTAG data output
P5.1/TDI	JTAG data input, or input/output digital port
TCK	JTAG test clock

5 DC Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	-0.3 V	-	3.6 V	Respect to VSS
V_{IA}	Analog Input Voltage	-0.3 V	-	1.98 V	Respect to AVSS
V_{ID}	Digital Input Voltage	-0.3 V	-	6.0 V	Respect to VSS
V_{PP}	OTP Programming voltage	-0.3V	-	7.0V	Respect to VSS
T_A	Ambient Temperature	-40 ˚C	-	85 ˚C	
T_S	Storage Temperature	-65 ˚C	-	150 ˚C	

Table 1 Absolute Maximum Ratings

Caution: Stresses beyond those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

5.2 System Clock Frequency and Power Consumption

C_{AREF} = 1nF, C_{MEXT}= 100nF. VDD1=3.3V, Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
SYSCLK	System Clock	32	-	128	**MHz**
P_D	Power consumption		160[1)]	200	**mW**

Table 2 System Clock Frequency

Note 1) The value is based on the condition of MCE clock=126MHz, 8051 clock 31.5MHz with a actual motor running by a typical MCE application program and 8051 code.

5.3 Digital I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	3.0 V	3.3 V	3.6 V	Recommended
V_{PP}	OTP Programming voltage	6.70V	6.75V	6.80V	Recommended
V_{IL}	Input Low Voltage	-0.3 V	-	0.8 V	Recommended
V_{IH}	Input High Voltage	2.0 V		3.6 V	Recommended
C_{IN}	Input capacitance	-	3.6 pF	-	(1)
I_L	Input leakage current		±10 nA	±1 µA	V_O = 3.3 V or 0 V
I_{OL2}(2)	Low level output current	17.9 mA	26.3 mA	33.4 mA	V_{OL} = 0.4 V (1)
I_{OH2}(2)	High level output current	24.6 mA	49.5 mA	81 mA	V_{OH} = 2.4 V (1)

Table 3 Digital I/O DC Characteristics

Note:

(1) Data guaranteed by design.

(2) Applied to all digital I/O pins.

5.4 Analog I/O (IFBU+,IFBU-,IFBUO, IFBV+,IFBV-,IFBVO) DC Characteristics

C_{AREF} = 1nF, C_{MEXT}= 100nF. VDD1=3.3V, Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
V_{OFFSET}	Input Offset Voltage	-	-	26 mV	
V_I	Input Voltage Range	0 V		1.2 V	Recommended
V_{OUTSW}	OP amp output operating range	50 mV (1)	-	1.2 V	
C_{IN}	Input capacitance	-	3.6 pF	-	(1)
R_{FDBK}	OP amp feedback resistor	5 kΩ	-	20 kΩ	Requested between IFBO and IFB-
OP $_{GAINCL}$	Operating Close loop Gain	80 db	-	-	(1)
CMRR	Common Mode Rejection Ratio	-	80 db	-	(1)
I_{SRC}	Op amp output source current	-	1 mA	-	V_{OUT} = 0.6 V (1)
I_{SNK}	Op amp output sink current	-	100 µA	-	V_{OUT} = 0.6 V (1)

Table 4 Analog I/O DC Characteristics

Note:

(1) Data guaranteed by design.

5.5 Under Voltage Lockout DC characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
UV_{CC+}	UVcc positive going Threshold	2.78 V	3.04 V	3.23 V	(1)
UV_{CC-}	UVcc negative going Threshold	2.78 V	2.97 V	3.23 V	
$UV_{CC}H$	UVcc Hysteresys	-	73 mV	-	(1)

Table 5 UVcc DC Characteristics

Note:

(1) Data guaranteed by design.

5.6 Itrip comparator DC characteristics

Unless specified, VDD1=3.3V, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
$Itrip_{+}$	Itrip positive going Threshold	-	1.22V	-	
$Itrip_{-}$	Itrip negative going Threshold	-	1.10V	-	
ItripH	Itrip Hysteresys	-	120mV	-	

Table 6 Itrip DC Characteristics

6 AC Characteristics

6.1 Digital PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
F_{CLKIN}	Crystal input frequency	3.2 MHz	4 MHz	60 MHz	(1) (see figure below)
F_{PLL}	Internal clock frequency	32 MHz	50 MHz	128 MHz	(1)
F_{LWPW}	Sleep mode output frequency	F_{CLKIN} ÷ 256	-	-	(1)
J_S	Short time jitter	-	200 psec	-	(1)
D	Duty cycle	-	50 %	-	(1)
T_{LOCK}	PLL lock time	-	-	500 µsec	(1)

Table 7 PLL AC Characteristics

Note:

(1) Data guaranteed by design.

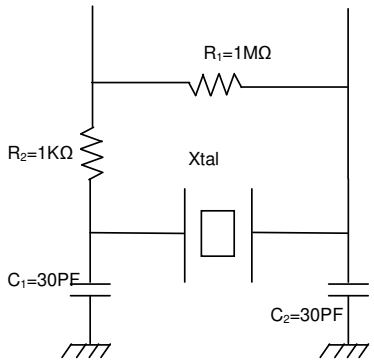


Figure 3 Crystal circuit example

6.2 Analog to Digital Converter AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
T_{CONV}	Conversion time	-	-	2.05 µsec	(1)
T_{HOLD}	Sample/Hold maximum hold time	-	-	10 µsec	Voltage droop ≤ 15 LSB (see figure below)

Table 8 A/D Converter AC Characteristics

Note:

(1) Data guaranteed by design.

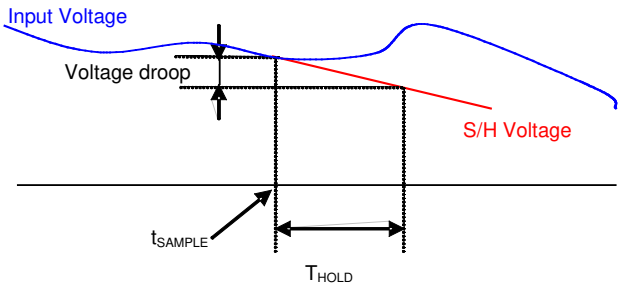


Figure 4 Voltage droop and S/H hold time

6.3 Op amp AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
OP_{SR}	OP amp slew rate	-	10 V/µsec	-	VDD1 = 3.3 V, CL = 33 pF (1)
OP_{IMP}	OP input impedance	-	10^8 Ω	-	(1) (2)
T_{SET}	Settling time	-	400 ns	-	VDD1 = 3.3 V, CL = 33 pF (1)

Table 9 Current Sensing OP Amp AC Characteristics

Note:

(1) Data guaranteed by design.

(2) To guarantee stability of the operational amplifier, it is recommended to load the output pin by a capacitor of 47pF, see Figure 5. Here only the single shunt current amplifier is show but all op amp outputs should be loaded with this capacitor.

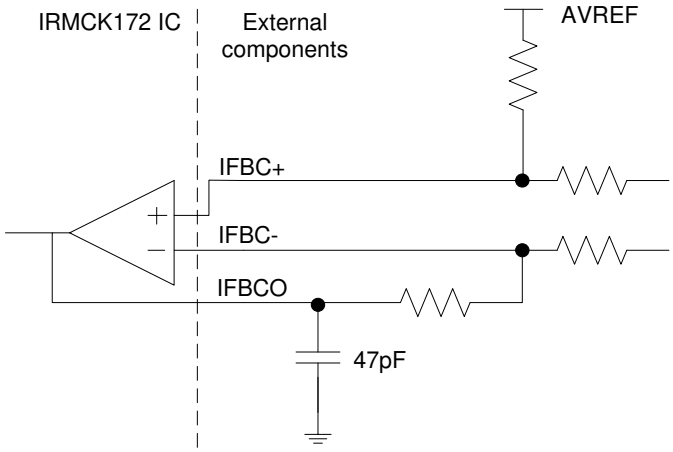


Figure 5 A capacitor of 47pF is recommended at the output pin of all op amps.

6.4 SYNC to SVPWM and A/D Conversion AC Timing

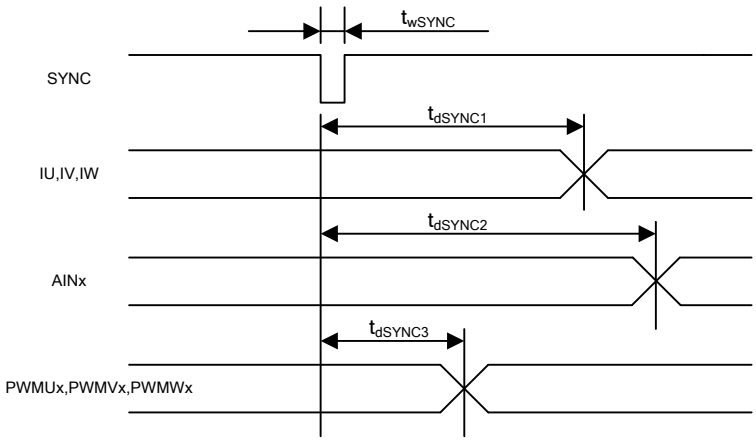


Figure 6 SYNC timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wSYNC}	SYNC pulse width	-	32	-	SYSCLK
t_{dSYNC1}	SYNC to current feedback conversion time	-	-	100	SYSCLK
t_{dSYNC2}	SYNC to AIN0-5 analog input conversion time	-	-	200	SYSCLK (1)
t_{dSYNC3}	SYNC to PWM output delay time	-	-	2	SYSCLK

Table 10 SYNC AC Characteristics

Note:

(1) AIN1 through AIN5 channels are converted once every 6 SYNC events

6.5 GATEKILL to SVPWM AC Timing

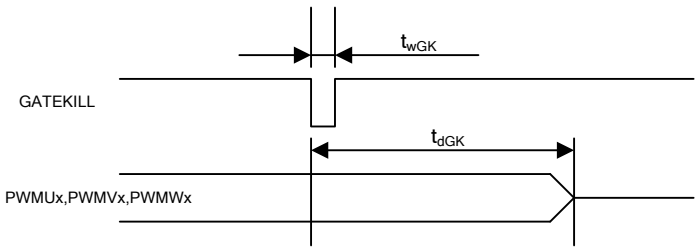


Figure 7 Gatekill timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wGK}	GATEKILL pulse width	32	-	-	SYSCLK
t_{dGK}	GATEKILL to PWM output delay	-	-	100	SYSCLK

Table 11 GATEKILL to SVPWM AC Timing

6.6 Itrip AC Timing

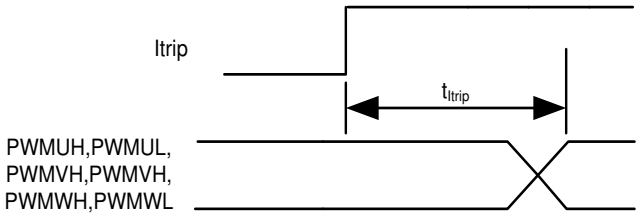


Figure 8 ITRIP timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{ITRIP}	Itrip propagation delay	-	-	100(sysclk)+1.0usec	SYSCLK+usec

Table 12 Itrip AC Timing

6.7 UART AC Timing

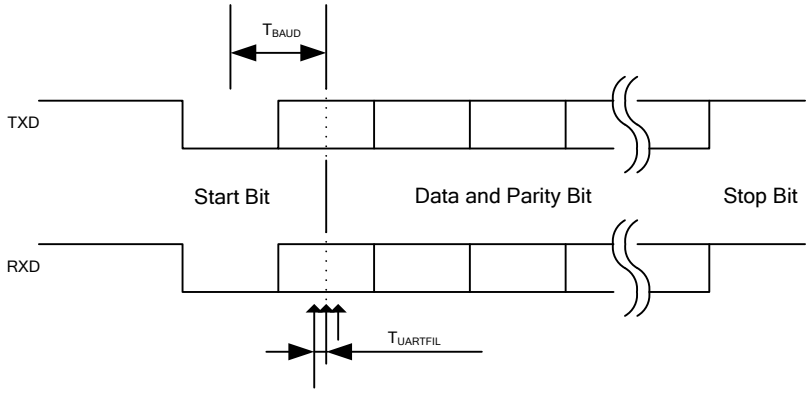


Figure 9 UART timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{BAUD}	Baud Rate Period	-	57600	-	bit/sec
$T_{UARTFIL}$	UART sampling filter period (1)	-	1/16	-	T_{BAUD}

Table 13 UART AC Timing

Note:

(1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of 1/16 T_{BAUD}. If three sampled values do not agree, then UART noise error is generated.

6.8 CAPTURE Input AC Timing

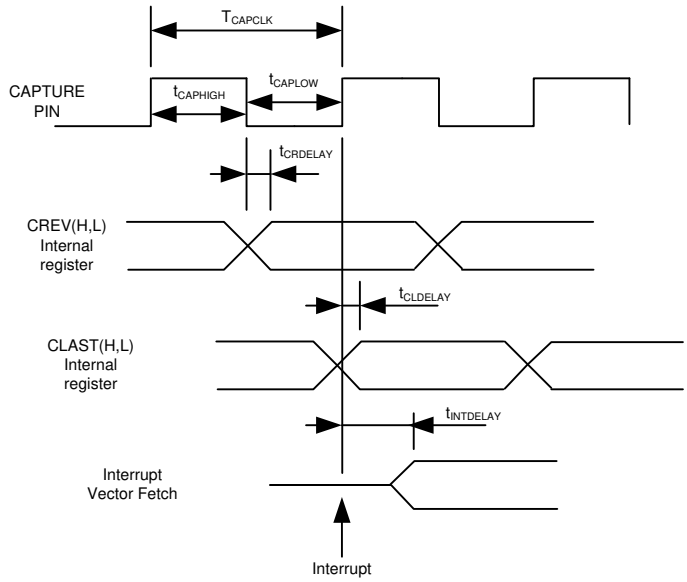


Figure 10 CAPTURE timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{CAPCLK}	CAPTURE input period	8	-	-	SYSCLK
$t_{CAPHIGH}$	CAPTURE input high time	4	-	-	SYSCLK
t_{CAPLOW}	CAPTURE input low time	4	-	-	SYSCLK
$t_{CRDELAY}$	CAPTURE falling edge to capture register latch time	-	-	4	SYSCLK
$t_{CLDELAY}$	CAPTURE rising edge to capture register latch time	-	-	4	SYSCLK
$t_{INTDELAY}$	CAPTURE input interrupt latency time	-	-	4	SYSCLK

Table 14 CAPTURE AC Timing

6.9 OTP Programming Timing

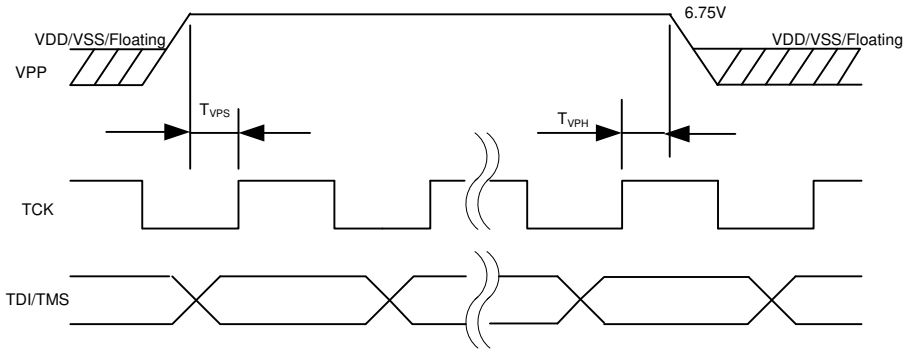


Figure 11 OTP programming timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{VPS}	VPP Setup Time	10	-	-	nsec
T_{VPH}	VPP Hold Time	15	-	-	nsec

Table 15 OTP Programming Timing

6.10 JTAG AC Timing

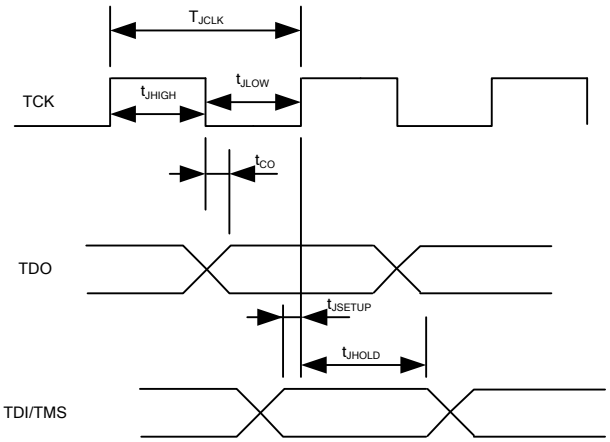


Figure 12 JTAG timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{JCLK}	TCK Period	-	-	50	MHz
t_{JHIGH}	TCK High Period	10	-	-	nsec
t_{JLOW}	TCK Low Period	10	-	-	nsec
t_{CO}	TCK to TDO propagation delay time	0	-	5	nsec
t_{JSETUP}	TDI/TMS setup time	4	-	-	nsec
t_{JHOLD}	TDI/TMS hold time	0	-	-	nsec

Table 16 JTAG AC Timing

7 I/O Structure

The following figure shows the motor PWM output (PWMUH/PWMUL/PWMVH/PWMVL/PWMWH/PWMWL)

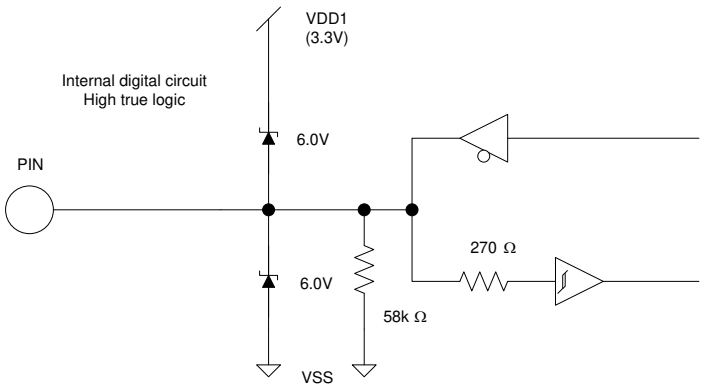


Figure 13 PWMUL/PWMUH/PWMVL/PWMVH/PWMWL/PWMWH output

The following figure shows the digital I/O structure except the motor PWM output

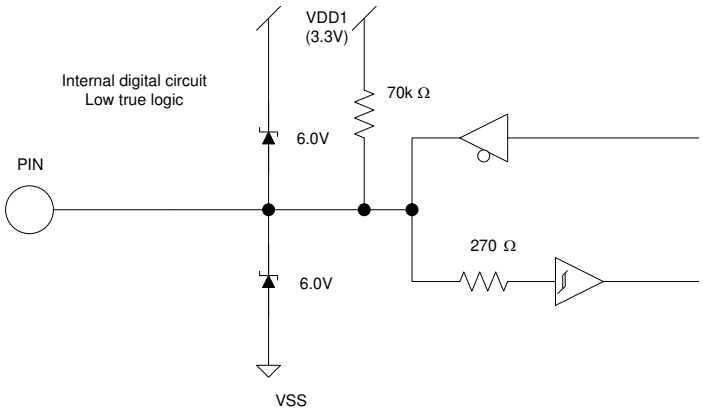


Figure 14 All digital I/O except motor PWM output

The following figure shows RESET and GATEKILL I/O structure.

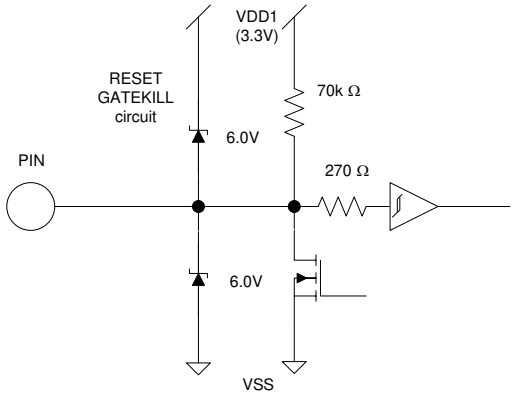


Figure 15 RESET, GATEKILL I/O

The following figure shows the analog input structure.

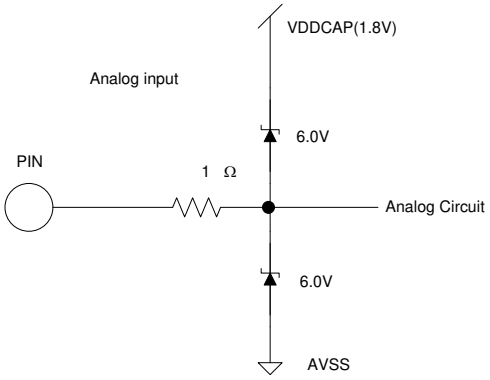


Figure 16 Analog input

The following figure shows all analog operational amplifier output pins and AREF pin I/O structure.

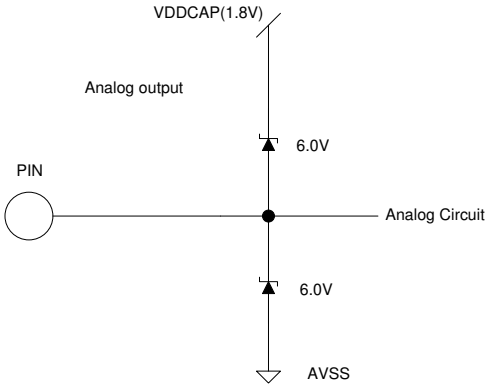


Figure 17 Analog operational amplifier output and AREF I/O structure

The following figure shows the VPP pin structure

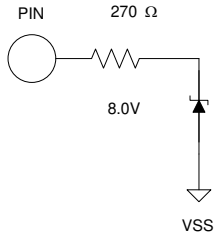


Figure 18 VPP programming pin I/O structure

The following figure shows the VSS and AVSS pins structure

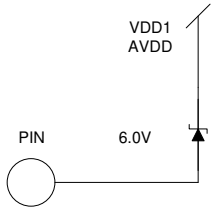


Figure 19 VSS and AVSS pin structure

The following figure shows the VDD1 and VDDCAP pin structure

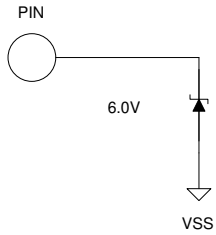


Figure 20 VDD1 and VDDCAP pin structure

The following figure shows the XTAL0 and XTAL1 pins structure

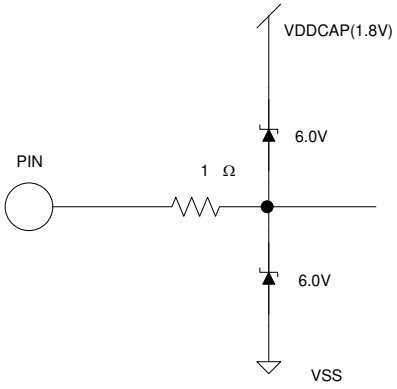


Figure 21 XTAL0/XTAL1 pins structure

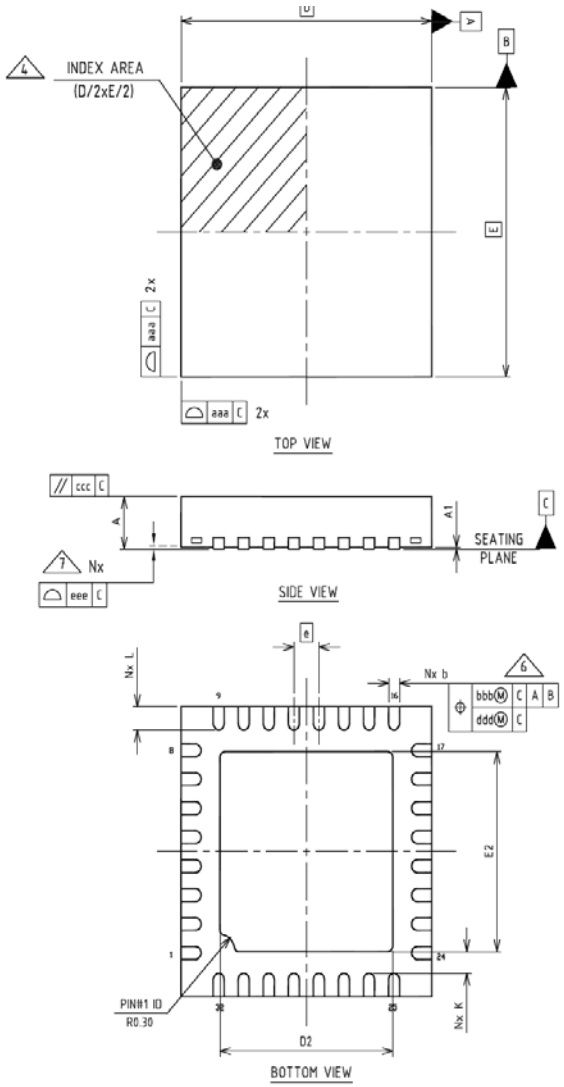
8 Pin List

Pin Number	Pin Name	Internal Pull-up /Pull-down	Pin Type	Description
1	RESET		I/O	Reset, low true, Schmitt trigger input
2	P1.1/RXD		I/O	UART receiver input or Discrete programmable I/O
3	P1.2/TXD		I/O	UART transmitter output or Discrete programmable I/O
4	XTAL0		I	Crystal input
5	XTAL1		O	Crystal output
6	VDD1		P	3.3V digital power
7	VSS		P	Digital common
8	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
9	P2.6/AOPWM0		I/O	Discrete programmable I/O or PWM 0 digital output
10	AIN0		I	Analog input channel 0, 0-1.2V range, needs to be pulled down to AVSS if unused
11	AIN1		I	Analog input channel 1, 0-1.2V range, needs to be pulled down to AVSS if unused
12	IFBU-		I	Single or U-phase leg shunt current sensing OP amp input (-)
13	IFBU+		I	Single or U-phase leg shunt current sensing OP amp input (+)
14	IFBUO		O	Single or U-phase leg shunt current sensing OP amp output
15	IFBV-		I	Single or V-phase leg shunt current sensing OP amp input (-)
16	IFBV+		I	Single or V-phase leg shunt current sensing OP amp input (+)
17	IFBVO		O	Single or V-phase leg shunt current sensing OP amp output
18	AVSS		P	Analog ground
19	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
20	VDD1		P	3.3V digital power
21	VSS		P	Digital common
22	PWMWL	58 kΩ Pull down	O	PWM gate drive for phase W low side, configurable either high or low true.
23	PWMVL	58 kΩ Pull down	O	PWM gate drive for phase V low side, configurable either high or low true
24	PWMUL	58 kΩ Pull down	O	PWM gate drive for phase U low side, configurable either high or low true
25	PWMWH	58 kΩ Pull down	O	PWM gate drive for phase W high side, configurable either high or low true
26	PWMVH	58 kΩ Pull down	O	PWM gate drive for phase V high side, configurable either high or low true

Pin Number	Pin Name	Internal Pull-up /Pull-down	Pin Type	Description
27	PWMUH	58 kΩ Pull down	O	PWM gate drive for phase U high side, configurable either high or low true
28	VPP/GK		I/O P	OTP programming power (6.5V) and PWM shutdown input
29	TMS/P5.2		I/O	JTAG test mode select or Discrete I/O
30	TDO/P5.3		O	JTAG test data output
31	TDI/P5.1		I/O	JTAG test data input or Discrete I/O
32	TCK		I	JTAG test clock

Table 17 Pin List

9 Package Dimensions

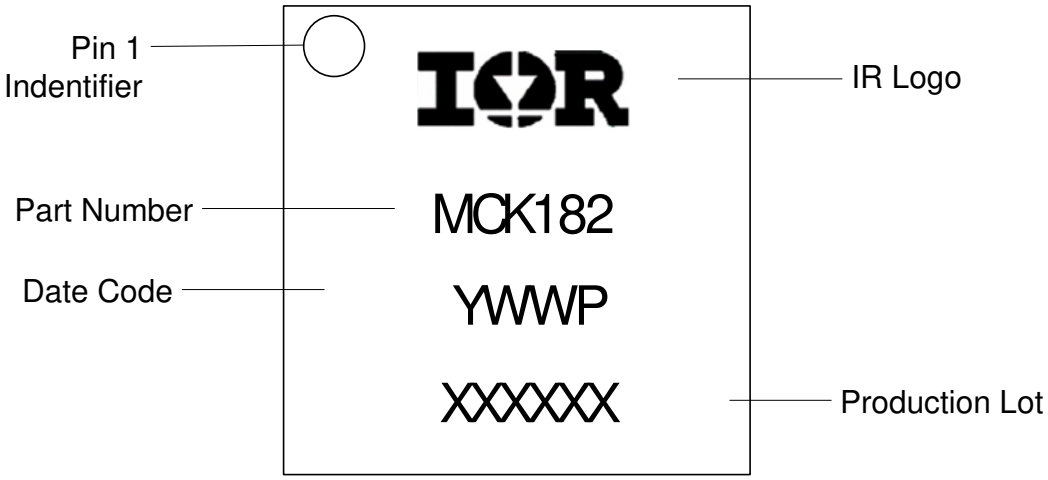


Dimension Table				
Thickness / Symbol	W : Very Very Thin			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
b	0.18	0.25	0.30	6
D		5.00 BSC		
E		5.00 BSC		
e		0.50 BSC		
D2	3.30	3.45	3.55	
E2	3.30	3.45	3.55	
K	0.20	---	---	
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		32		3
ND		8		5
NE		8		5
NOTES		1, 2		
LF PART NO.		437727		
LF DWG. NO.		CARSEM-06257		
REV.		A		

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side repectively .
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

10 Part Marking Information



11 Qualification Information

Qualification Level		Industrial[††] (per JEDEC JESD47)
Moisture Sensitivity Level		MSL2[†††] (per IPC/JEDEC J-STD-020)
ESD	**Machine Model**	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 2 (per ANSI/ESDA/JEDEC JS-001)
	Charged Device Model	Class C2 (per JEDEC standard JESD22-C101)
	Latch-Up	Class I, Level B (per JEDEC standard JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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