

## LOW INPUT OFFSET VOLTAGE C-MOS OPERATIONAL AMPLIFIER

### ■ GENERAL DESCRIPTION

The NJU7061,62 and 64 are single, dual and quad C-MOS Operational Amplifiers operated on a single-power-supply, low voltage and low operating current.

The input offset voltage is lower than 2mV, and the input bias current is as low as less than 1pA, consequently the very small signal around the ground level can be amplified.

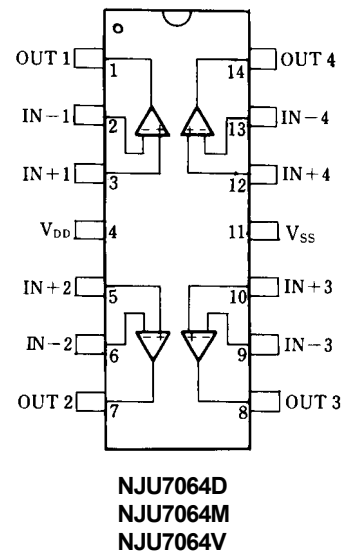
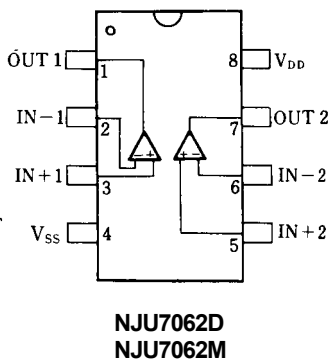
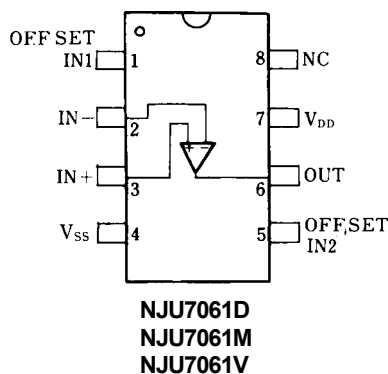
The minimum operating voltage is 3V and the output stage permits output signal to swing between both of the supply rails.

Furthermore, the operating current is also as low as 150μA (typ) per circuit, therefore it can be applied especially to battery operated items.

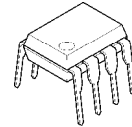
### ■ FEATURES

- Single-Power-Supply
- Low Input Offset Voltage ( $V_{IO}=2\text{mV max}$ )
- Wide Operating Voltage ( $V_{DD}=3\sim 16\text{V}$ )
- Wide Output Swing Range ( $V_{OM}=9.98\text{V typ. @ }V_{DD}=10\text{V}$ )
- Low Operating Current ( $150\mu\text{A/circuit}$ )
- Low Bias Current ( $I_B=1\text{pA typ.}$ )
- Internal Compensation Capacitor
- External Offset Null Adjustment (Only NJU7061)
- Package Outline  
 DIP/DMP/SSOP8 (NJU7061)  
 DIP/DMP8 (NJU7062)  
 DIP/DMP/SSOP14 (NJU7064)
- C-MOS Technology

### ■ PIN CONFIGURATION



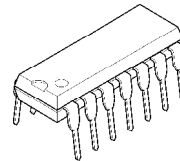
### ■ PACKAGE OUTLINE



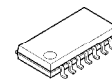
**NJU7061D  
NJU7062D**



**NJU7061M  
NJU7062M**



**NJU7064D**



**NJU7064M**



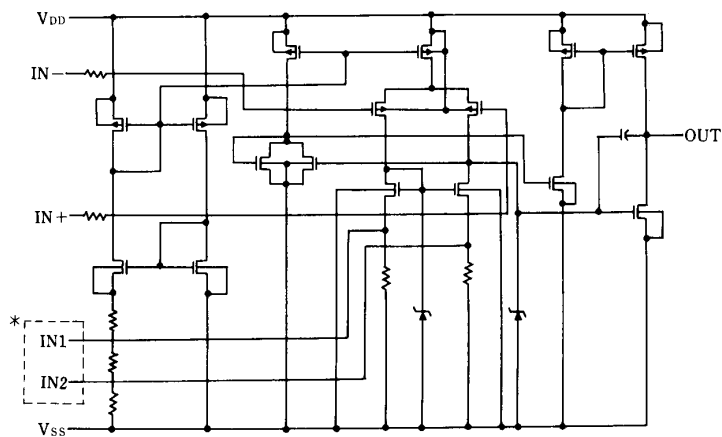
**NJU7061V**



**NJU7064V**

# NJU7061/62/64

## ■ EQUIVALENT CIRCUIT



\* IN1, IN2 are only for NJU7061 ( NJU7062/64 don't have these terminals ).

## ■ ABSOLUTE MAXIMUM RATINGS

( Ta=25°C )

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	18	V
Differential Input Voltage	$V_{ID}$	$\pm 18$ (note1)	V
Common Mode Input Voltage	$V_{IC}$	-0.3~18	V
Power Dissipation	$P_D$	( DIP14 ) 700 ( DIP8 ) 500 ( DMP8,14 ) 300 ( SSOP14 ) 300 ( SSOP8 ) 250	mW
Operating Temperature Range	$T_{opr}$	-40~+85	°C
Storage Temperature Range	$T_{stg}$	-40~+125	°C

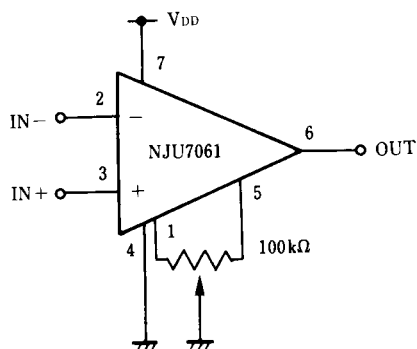
( note1 ) If the supply voltage ( $V_{DD}$ ) is less than 18V, the input voltage must not over the  $V_{DD}$  level though 18V is limit specified.

## ■ ELECTRICAL CHARACTERISTICS

( Ta=25°C,  $V_{DD}=10V, R_L=\infty$  )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$V_{IO}$	$R_S=50\Omega$	-	-	2	mV
Input Offset Current	$I_{IO}$		-	1	-	pA
Input Bias Current	$I_{IB}$		-	1	-	pA
Input Impedance	$R_{IN}$		-	1	-	TΩ
Large Signal Voltage Gain	$A_V$		80	95	-	dB
Input Common Mode Voltage Range	$V_{ICM}$		0~9	-	-	V
Maximum Output Swing Voltage	$V_{OM}$	$R_L=1M\Omega$	9.80	9.98	-	V
Common Mode Rejection Ratio	CMR		60	75	-	dB
Supply Voltage Rejection Ratio	SVR		60	75	-	dB
Operating Current/Circuit	$I_{DD}$		-	150	300	μA
Slew Rate	SR		-	0.40	-	V/μs
Unity Gain Bandwidth	$F_t$	$A_V=40dB, C_L=10pF$	-	0.4	-	MHz

## ■ OFFSET ADJUSTMENT CIRCUIT ( Only For NJU7061 )



**[CAUTION]**

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