

N-channel 1050 V, 1.4 Ω typ., 4 A MDmesh™ K5
Power MOSFETs in TO-220, IPAK and TO-247 packages

Datasheet - production data

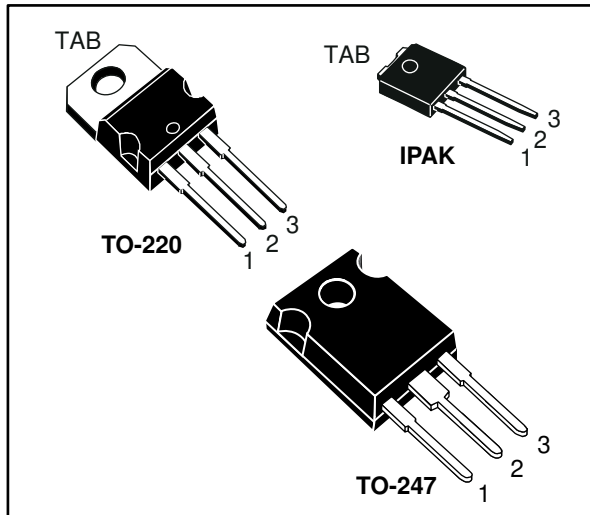
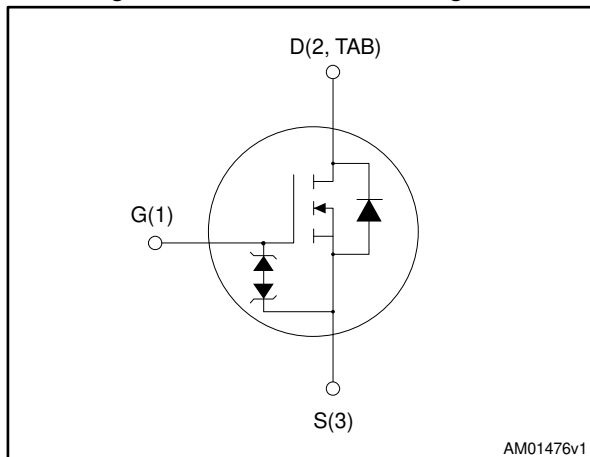


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STP7N105K5	1050 V	2 Ω	4 A	110 W
STU7N105K5				
STW7N105K5				

- Industry's lowest R_{DS(on)} X area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP7N105K5	7N105K5	TO-220	Tube
STU7N105K5		IPAK	
STW7N105K5		TO-247	

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source voltage	± 30	V
I _D	Drain current (continuous) at T _C = 25 °C	4	A
I _D	Drain current (continuous) at T _C = 100 °C	3	A
I _{DM} ⁽¹⁾	Drain current (pulsed)	16	A
P _{TOT}	Total dissipation at T _C = 25 °C	110	W
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	1.5	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D =I _{AR} , V _{DD} = 50 V)	132	mJ
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	V/ns
T _j	Operating junction temperature range	- 55 to 150	°C
T _{stg}	Storage temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾I_{SD} ≤ 4 A, di/dt ≤ 100 A/μs, V_{DS(peak)} ≤ V_{(BR)DSS} ; V_{SD} ≤ 840 V

⁽³⁾V_{DS} ≤ 840 V

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		TO-220	IPAK	TO-247	
R _{thj-case}	Thermal resistance junction-case max	1.14			°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.5	100	50	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 1 mA	1050			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 1050 V			1	μA
		V _{GS} = 0, V _{DS} = 1050 V, T _C = 125 °C ⁽¹⁾			50	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0, V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 2 A		1.4	2	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0	-	380	-	pF
C _{oss}	Output capacitance		-	40	-	pF
C _{rss}	Reverse transfer capacitance		-	0.65	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0, V _{DS} = 0 to 840 V	-	47	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	17	-	pF
R _G	Intrinsic gate resistance	f = 1MHz open drain	-	7	-	Ω
Q _g	Total gate charge	V _{DD} = 840 V, I _D = 4 A	-	11	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	2.8	-	nC
Q _{gd}	Gate-drain charge	<i>Figure 18: "Test circuit for gate charge behavior"</i>	-	5.6	-	nC

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 525V$, $I_D = 2 A$, $R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see Figure 17: "Test circuit for resistive load switching times" and Figure 22: "Switching time waveform")	-	17.5	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time		-	43	-	ns
t_f	Fall time		-	25	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
I_{SDM}	Source-drain current (pulsed)				16	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 4 A$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4 A$, $V_{DD} = 60 V$ $di/dt = 100 A/\mu s$, Figure 19: "Test circuit for inductive load switching and diode recovery times"	-	370		ns
Q_{rr}	Reverse recovery charge		-	3		μC
I_{RRM}	Reverse recovery current		-	16.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 4 A$, $V_{DD} = 60 V$ $di/dt = 100 A/\mu s$, $T_j = 150 ^\circ C$ Figure 19: "Test circuit for inductive load switching and diode recovery times"	-	600		ns
Q_{rr}	Reverse recovery charge		-	4.4		μC
I_{RRM}	Reverse recovery current		-	14.5		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 mA$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for TO-220 and TO-247

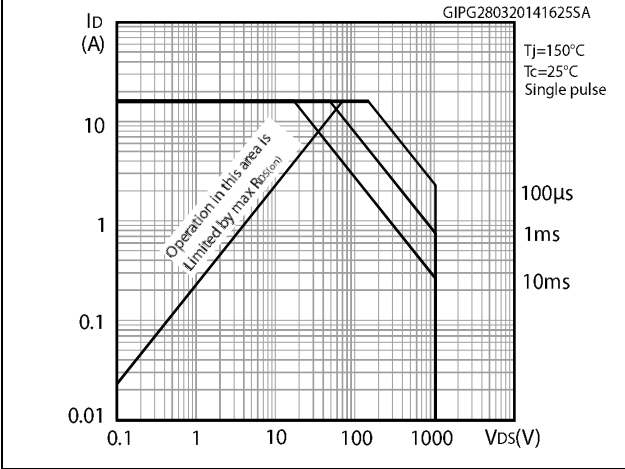


Figure 3: Thermal impedance for TO-220 and TO-247

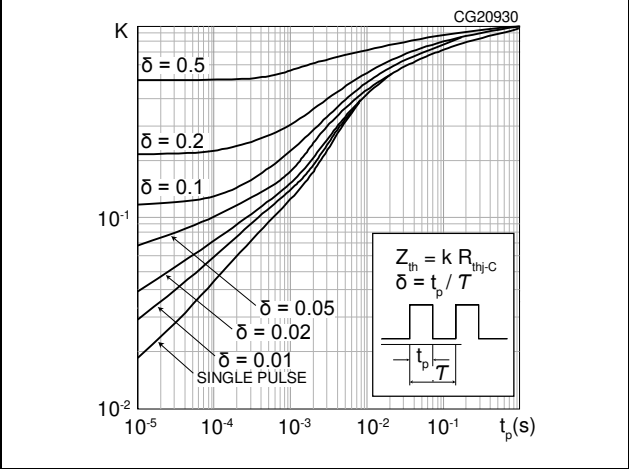


Figure 4: Safe operating area for IPAK

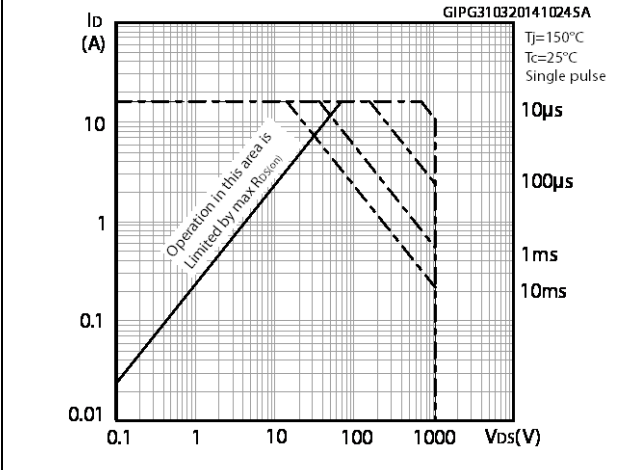


Figure 5: Thermal impedance for IPAK

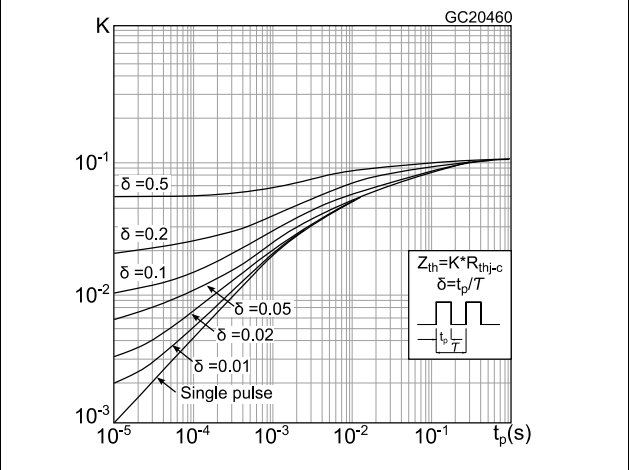


Figure 6: Output characteristics

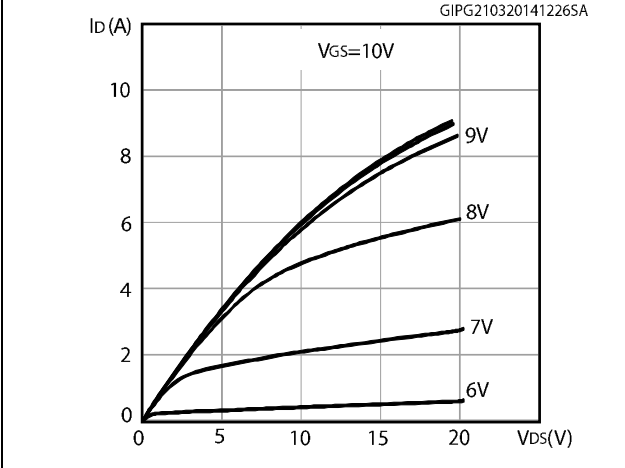


Figure 7: Transfer characteristics

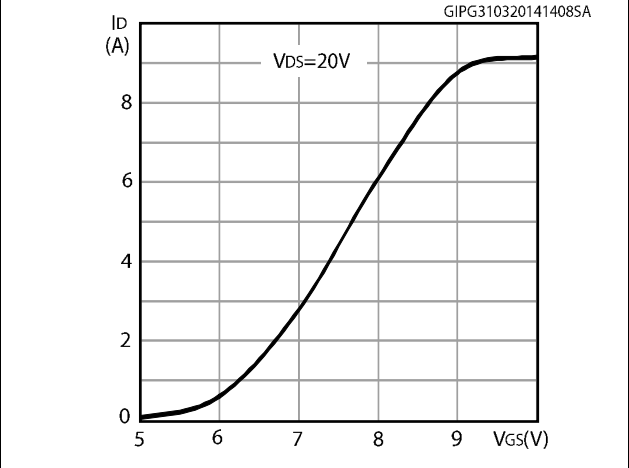


Figure 8: Gate charge vs gate-source voltage

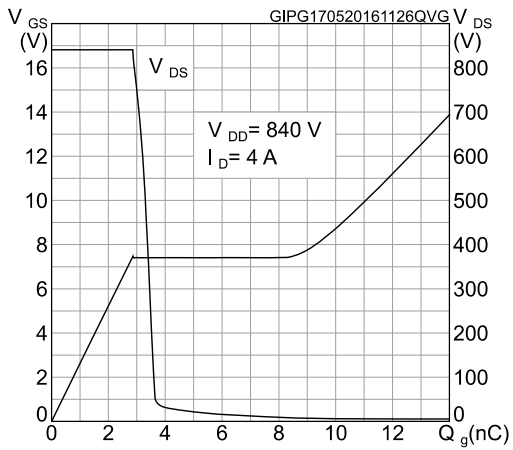


Figure 9: Static drain-source on-resistance

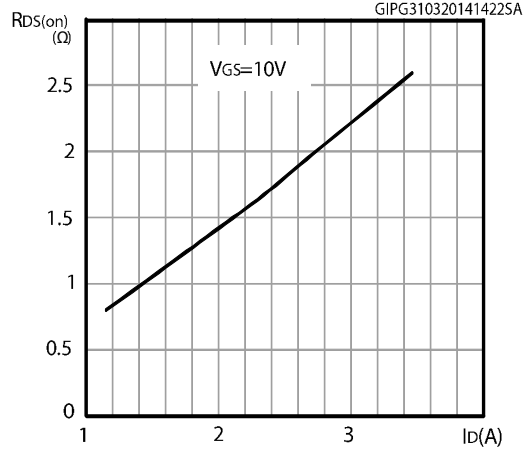


Figure 10: Capacitance variations

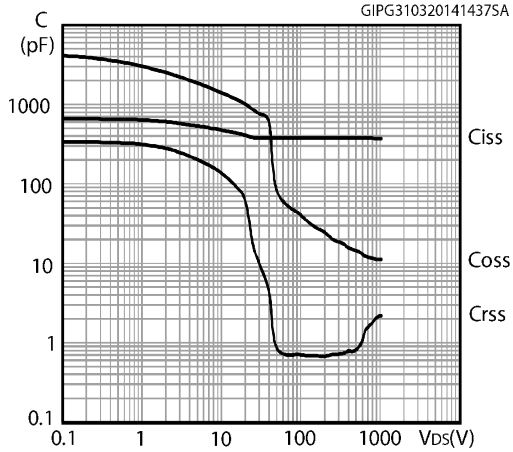


Figure 11: Source-drain diode forward characteristics

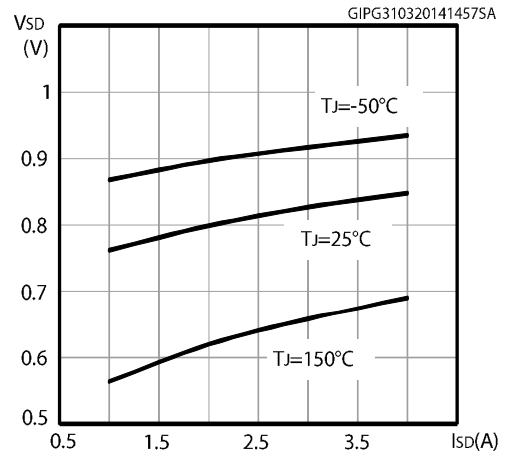


Figure 12: Normalized gate threshold voltage vs temperature

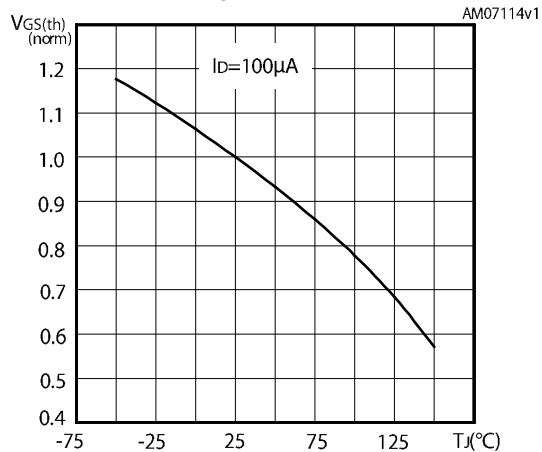
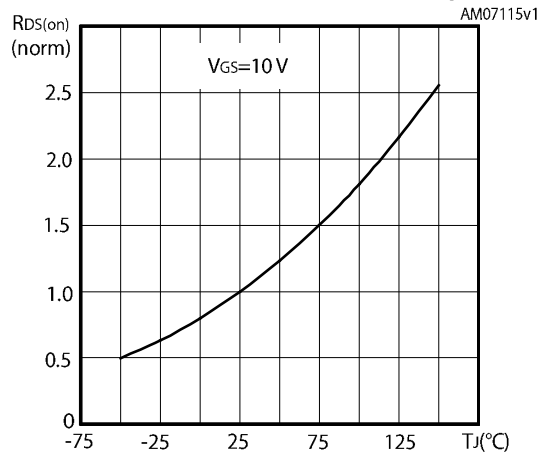


Figure 13: Normalized on-resistance vs temperature



Electrical characteristics

STP7N105K5, STU7N105K5, STW7N105K5

Figure 14: Normalized V(BR)DSS vs temperature

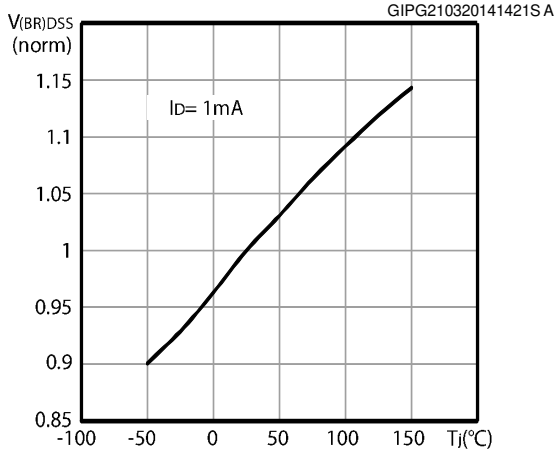


Figure 15: Maximum avalanche energy vs starting Tj

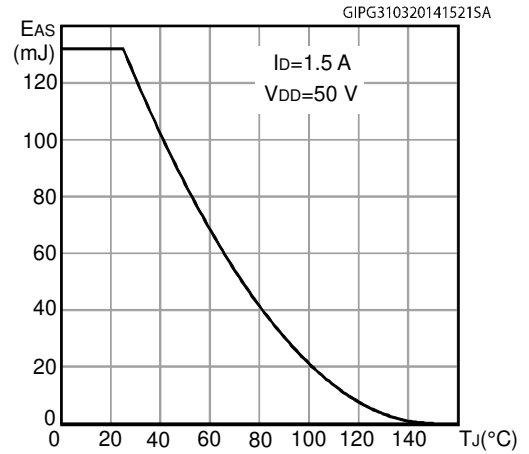
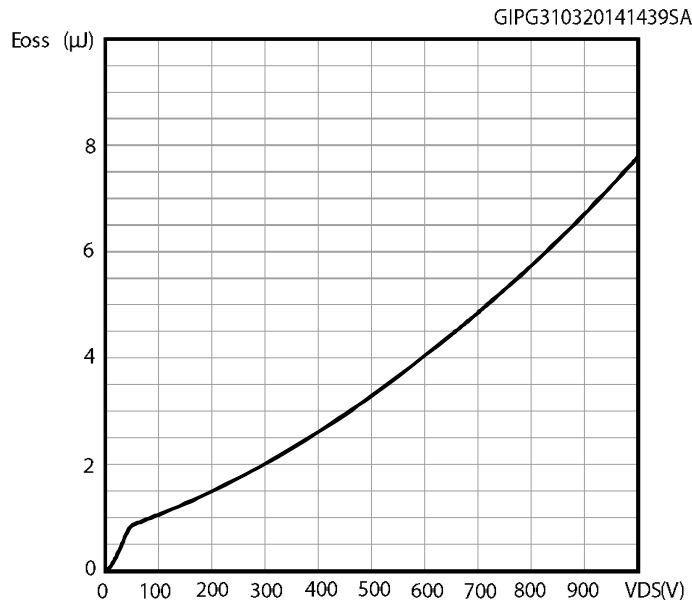
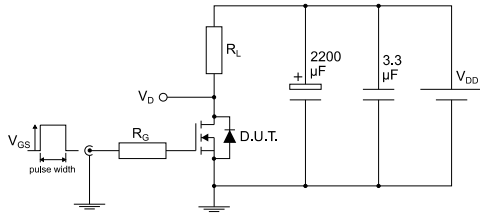


Figure 16: Output capacitance stored energy



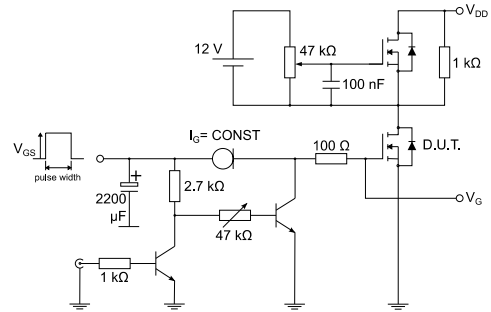
3 Test circuits

Figure 17: Test circuit for resistive load switching times



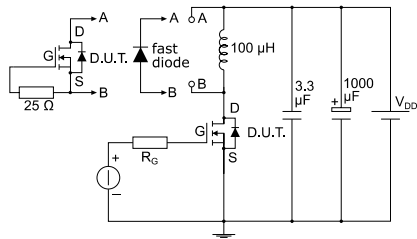
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Figure 18: Test circuit for gate charge behavior



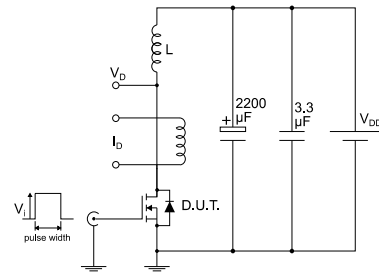
AM01469v1

Figure 19: Test circuit for inductive load switching and diode recovery times



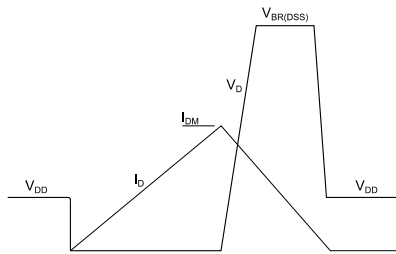
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Figure 20: Unclamped inductive load test circuit



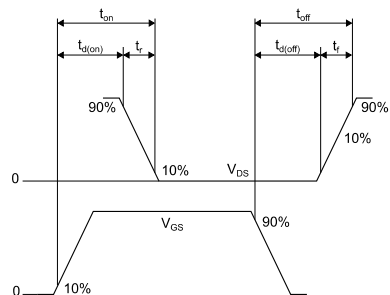
AM01471v1

Figure 21: Unclamped inductive waveform



AM01472v1

Figure 22: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220 package information

Figure 23: TO-220 type A package outline

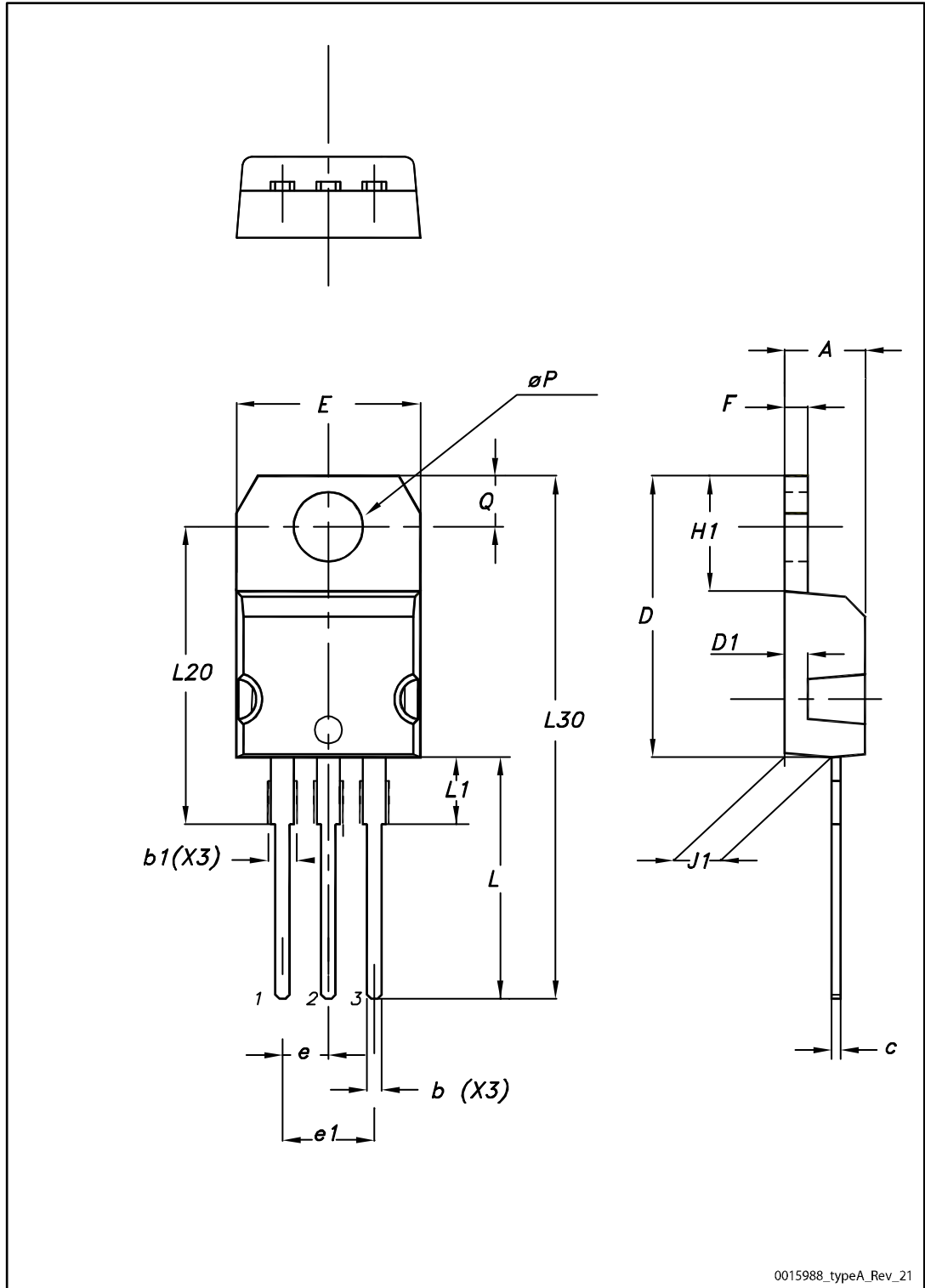


Table 9: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.2 IPAK package information

Figure 24: IPAK (TO-251) type A package outline

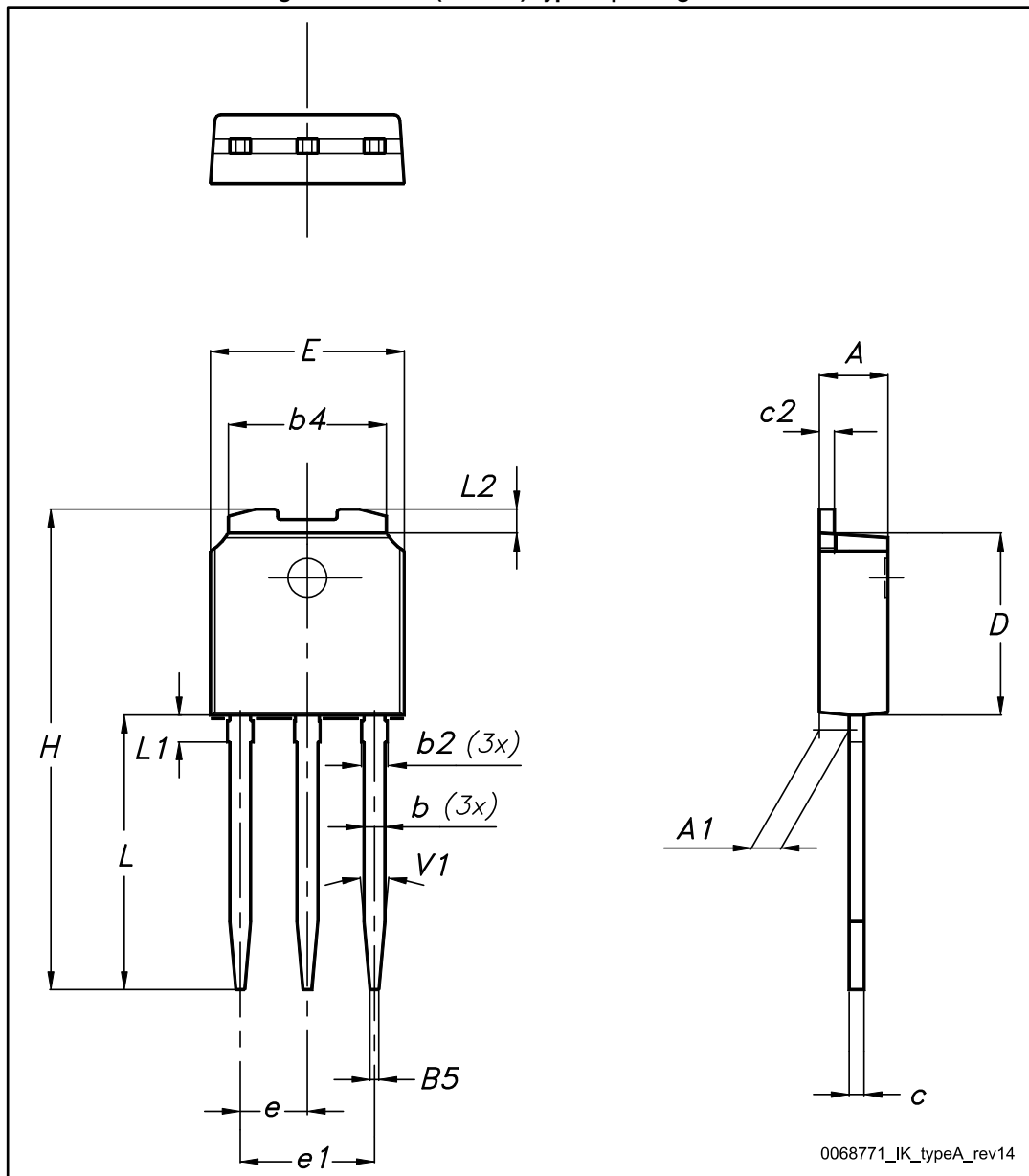
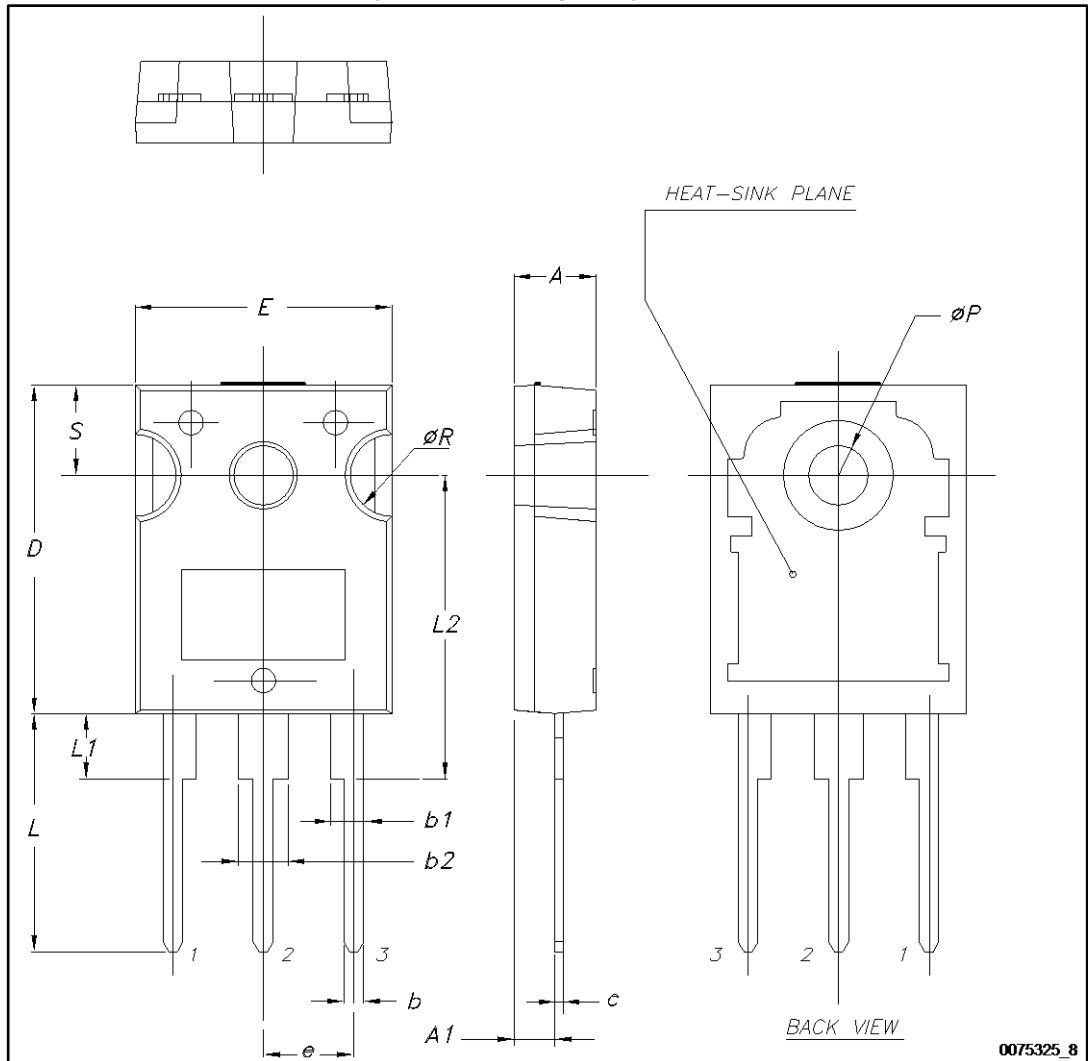


Table 10: IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.3 TO-247 package information

Figure 25: TO-247 package outline



0075325_8

Table 11: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
07-Apr-2014	1	First release.
17-Oct-2016	2	Updated <i>Figure 8: "Gate charge vs gate-source voltage"</i> and <i>Table 5: "Dynamic"</i> . Minor text changes.

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