MPQ4418A

0.6A, 36V, High-Efficiency, Low-$R_{DS(ON)}$, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4418A is a high-efficiency, synchronous, rectified, switch-mode, step-down converter with built-in internal power MOSFETs. It can achieve up to 0.6A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range (4V to 36V), with excellent load and line regulation.

Synchronous mode offers high efficiency across the entire I_{OUT} range. Current control mode provides fast transient response and improves loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MPQ4418A offers a compact solution that requires a minimal number of readily available, standard, external components, and is available in a small TSOT23-8 package.

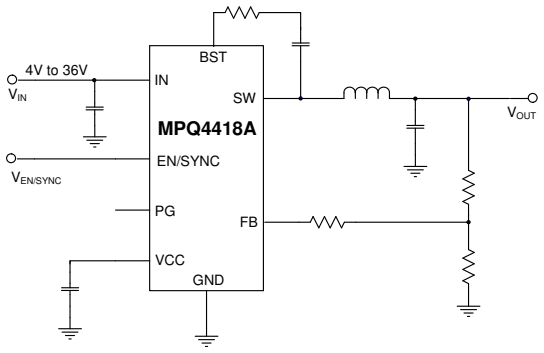
FEATURES

- Wide 4V to 36V Operating Input Voltage (V_{IN}) Range
- Configurable Output Voltage (V_{OUT}) from 0.8V
- Internal Low-$R_{DS(ON)}$ 90mΩ High-Side MOSFET (HS-FET) and 55mΩ Low-Side MOSFET (LS-FET)
- High-Efficiency Synchronous Mode Operation
- 410kHz Default Switching Frequency (f_{SW})
- 200kHz to 2.2MHz Synchronized External Clock
- High Duty Cycle for Automotive Cold Crank
- Forced Continuous Conduction Mode (FCCM)
- Internal Soft Start (SS)
- Power Good (PG)
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown
- Available in a TSOT23-8 Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

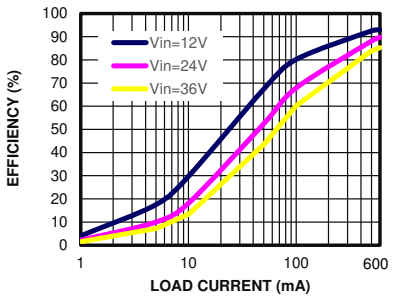
- Automotive
- Industrial Control Systems
- Distributed Power Systems

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 3.3V



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4418AGJ-AEC1	TSOT23-8	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4418AGJ-AEC1-Z).

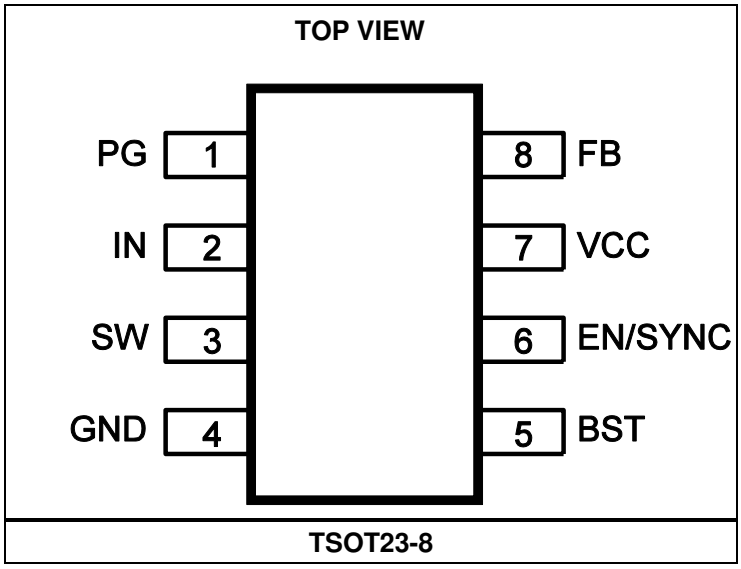
** Moisture Sensitivity Level Rating

TOP MARKING

BVMY

BVM: Product code
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good (PG) output.** The PG pin is an open-drain output. If the output voltage (V_{OUT}) exceeds 90% of the nominal voltage, this pin is pulled high.
2	IN	**Supply voltage.** The MPQ4418A operates from a 4V to 36V input rail. An input capacitor (C1) is required to decouple the input rail. To minimize switching spikes, connect C1 to GND to decouple the input rail. Place C1 as close to IN as possible.
3	SW	**Switch output.** The SW pin is the internal power switch's output.
4	GND	**Reference system ground.** The GND pin is critical to successful PCB layout. GND is the reference ground of the regulated V_{OUT}; connect the GND pin to system ground using copper traces and vias.
5	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side MOSFET (HS-FET) driver. To reduce SW voltage spikes, it is recommended to place a 20Ω resistor between SW and BST.
6	EN/SYNC	**Enable/synchronous.** To turn on the MPQ4418A, pull the EN/SYNC pin high. To configure the switching frequency (f_{SW}), apply an external clock to EN/SYNC.
7	VCC	**Bias supply.** Decouple VCC with a 0.1µF to 0.22µF capacitor, which must not exceed 0.22µF.
8	FB	**Feedback.** To set V_{OUT}, connect FB to the tap of an external resistor divider between the output and GND. When the FB voltage (V_{FB}) drops below 660mV, the frequency foldback comparator decreases the oscillator frequency to prevent current limit runaway during a short-circuit fault.

ABSOLUTE MAXIMUM RATINGS (1)

Continuous supply voltage (V_{IN}) ..... -0.3V to +40V
Switch voltage (V_{SW}) ..... -0.3V to +41V
BST voltage (V_{BST}) ..... V_{SW} + 6V
All other pins ..... -0.3V to +6V (2)
Continuous power dissipation (T_A = 25°C) (3)
TSOT23-8 ..... 1.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Continuous supply voltage (V_{IN}) ..... 4V to 36V
Output voltage (V_{OUT}) ..... 0.8V to 0.9 x V_{IN}
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
TSOT23-8	100	55	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on the EN pin's absolute maximum rating, see the Enable/Synchronous (EN/SYNC) Control section on page 11.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{SHDN}	V_{EN} = 0V			8	μA
Quiescent supply current	I_Q	V_{EN} = 2V, V_{FB} = 1V, no switching		0.6	0.8	mA
High-side (HS) on resistance	R_{ON_HS}	V_{BST_SW} = 5V		90	155	mΩ
Low-side (LS) on resistance	R_{ON_LS}	V_{CC} = 5V		55	105	mΩ
Switch leakage	I_{LKG_SW}	V_{EN} = 0V, V_{SW} = 12V			1	μA
Current limit	I_{LIMIT}	<40% duty cycle	1.3	1.7	2.1	A
Oscillator frequency	f_{SW}	V_{FB} = 750mV	320	410	500	kHz
Foldback frequency	f_{FB}	V_{FB} < 400mV	70	100	130	kHz
Maximum duty cycle	D_{MAX}	V_{FB} = 750mV, 410kHz	92	95		%
Minimum on time (5)	t_{ON_MIN}			70		ns
SYNC frequency range	f_{SYNC}		0.2		2.4	MHz
Feedback (FB) voltage	V_{FB}	T_J = 25°C	780	792	804	mV
			776		808	
FB current	I_{FB}	V_{FB} = 820mV		10	100	nA
Enable (EN) rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN falling threshold	$V_{EN\_FALLING}$		1.05	1.25	1.45	V
EN threshold hysteresis	V_{EN_HYS}			150		mV
EN input current	I_{EN}	V_{EN} = 2V		4	6	μA
		V_{EN} = 0V		0	0.2	μA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.3	3.5	3.7	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		3.1	3.3	3.5	V
V_{IN} UVLO threshold hysteresis	$V_{IN\_UVLO\_HYS}$			200		mV
VCC regulator	V_{CC}	I_{CC} = 0mA	4.6	4.9	5.2	V
VCC load regulation		I_{CC} = 5mA		1.5	4	%
Soft-start time	t_{SS}	V_{OUT} from 10% to 90%	0.55	1.45	2.45	ms
Thermal shutdown (5)			150	170		°C
Thermal hysteresis (5)				30		°C
Power good (PG) rising threshold	PG_{VTH_RISING}	As a percentage of V_{FB}	86	90	94	%
PG falling threshold	$PG_{VTH\_FALLING}$	As a percentage of V_{FB}	80	84	88	%
PG threshold hysteresis	PG_{VTH_HYS}	As a percentage of V_{FB}		6		%
PG rising deglitch time	t_{PG_RISING}		40	90	160	μs
PG falling deglitch time	$t_{PG\_FALLING}$		30	55	95	μs
PG sink current	V_{PG}	Sink 4mA		0.1	0.3	V
PG leakage current	I_{LKG_PG}			10	100	nA

Note:

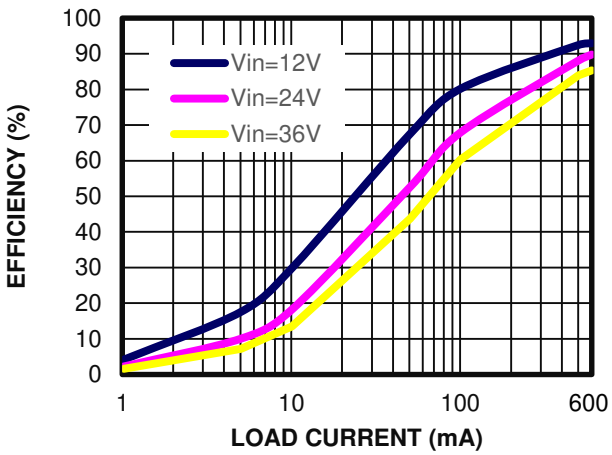
5) Guaranteed by design. Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST} = 20Ω, T_A = 25°C, unless otherwise noted.

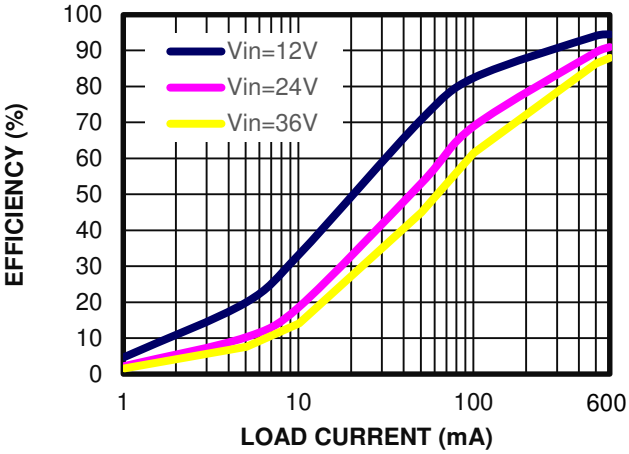
Efficiency vs. Load Current

V_{OUT} = 3.3V

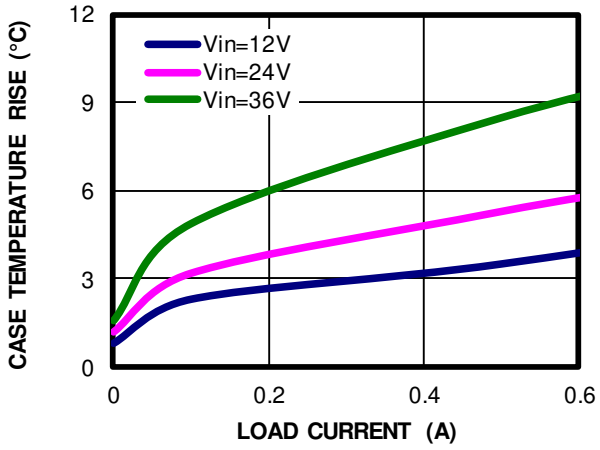


Efficiency vs. Load Current

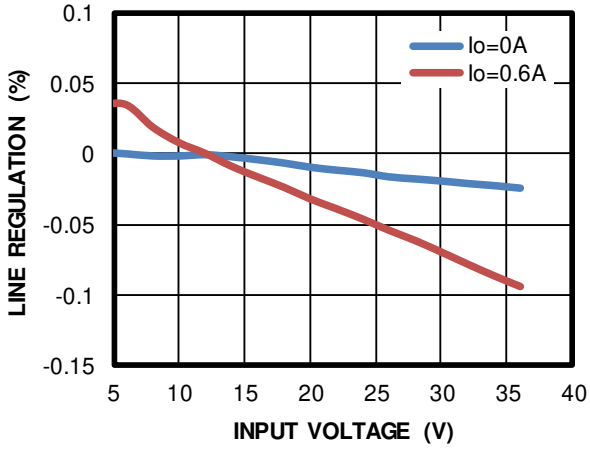
V_{OUT} = 5V



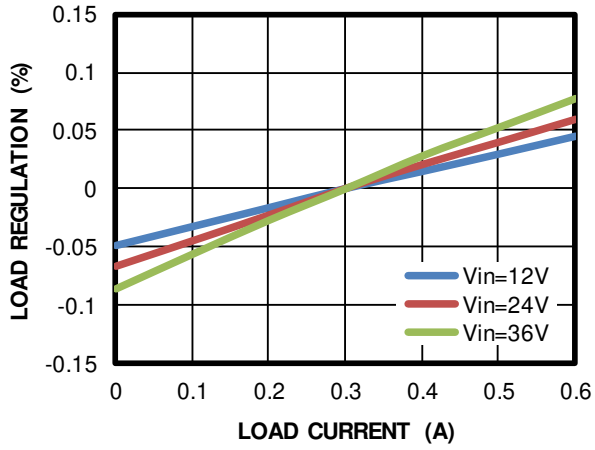
Case Temperature Rise vs. Load Current



Line Regulation



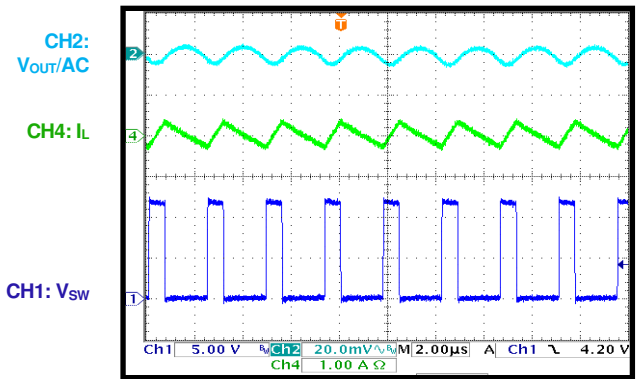
Load Regulation



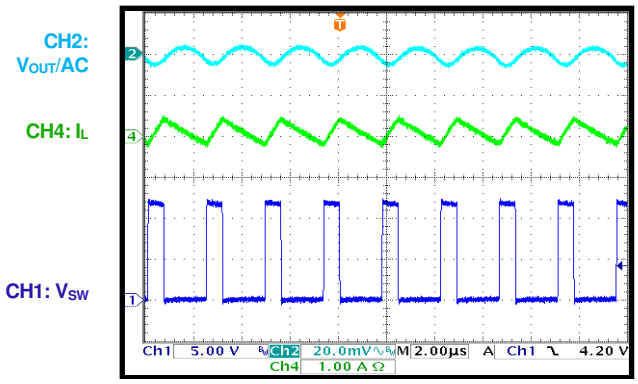
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST} = 20Ω, T_A = 25°C, unless otherwise noted.

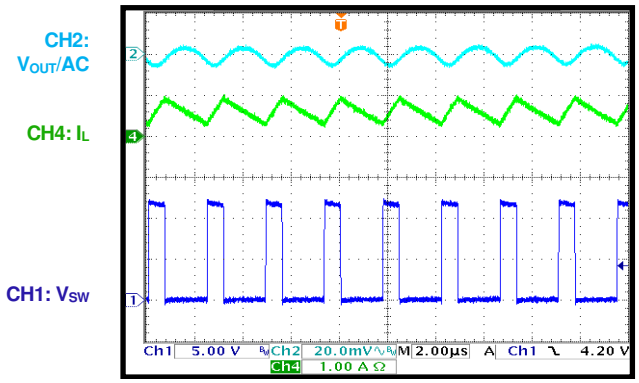
Steady State
I_{OUT} = 0A



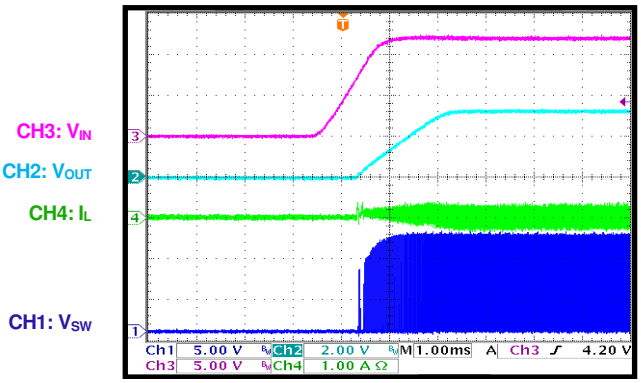
Steady State
I_{OUT} = 0.1A



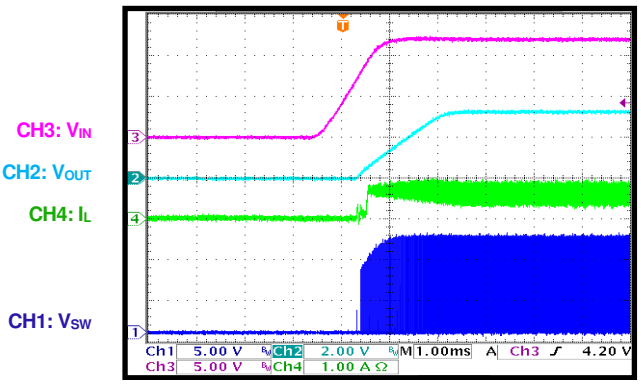
Steady State
I_{OUT} = 0.6A



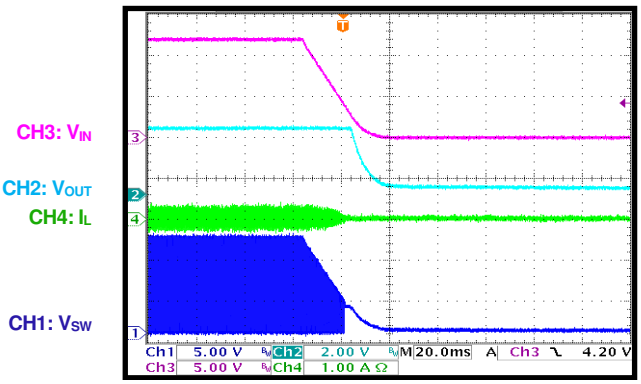
Start-Up through VIN
I_{OUT} = 0A



Start-Up through VIN
I_{OUT} = 0.6A



Shutdown through VIN
I_{OUT} = 0A

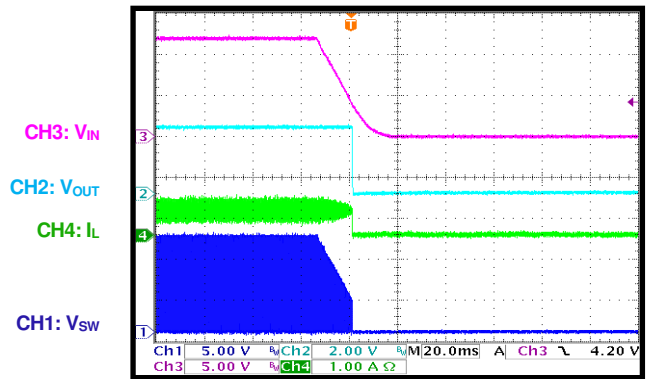


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST} = 20Ω, T_A = 25°C, unless otherwise noted.

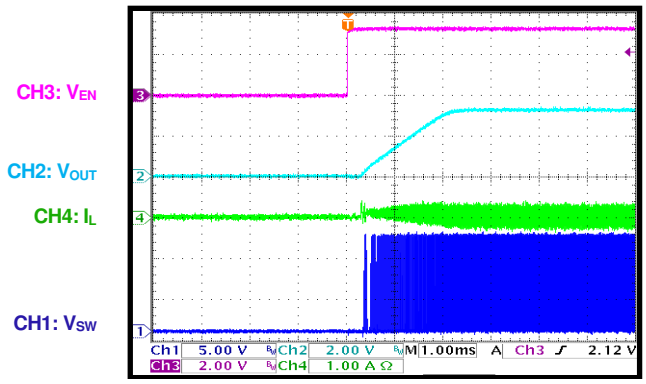
Shutdown through VIN

I_{OUT} = 0.6A



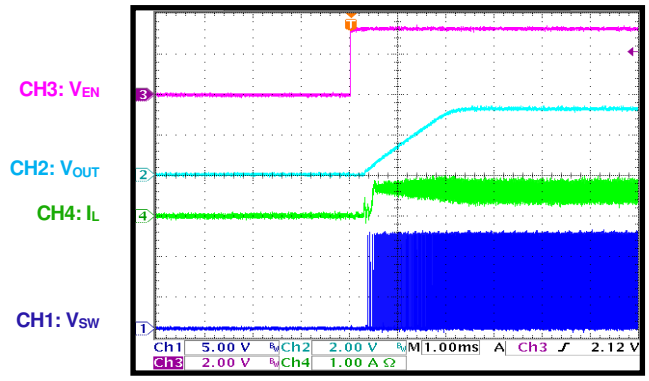
Start-Up through EN

I_{OUT} = 0A



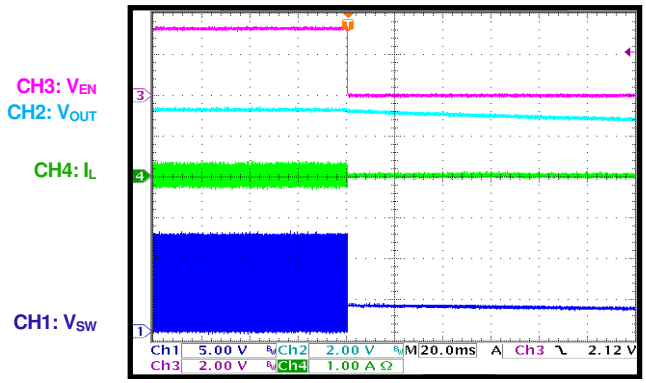
Start-Up through EN

I_{OUT} = 0.6A



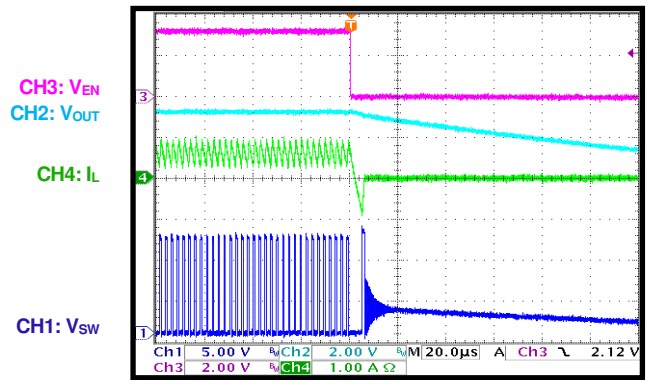
Shutdown through EN

I_{OUT} = 0A



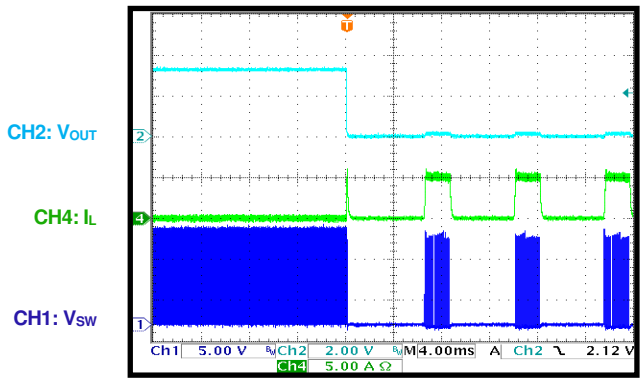
Shutdown through EN

I_{OUT} = 0.6A



SCP Entry

I_{OUT} = 0A to short circuit

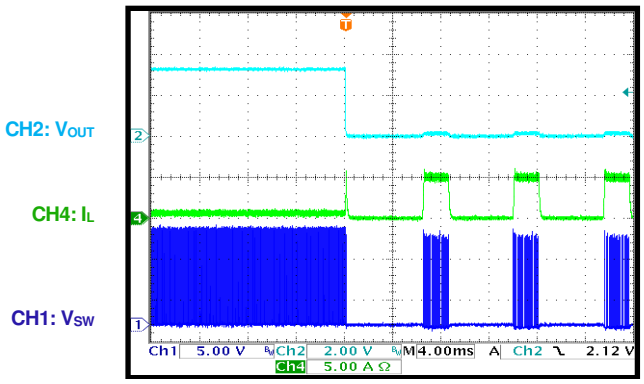


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST} = 20Ω, T_A = 25°C, unless otherwise noted.

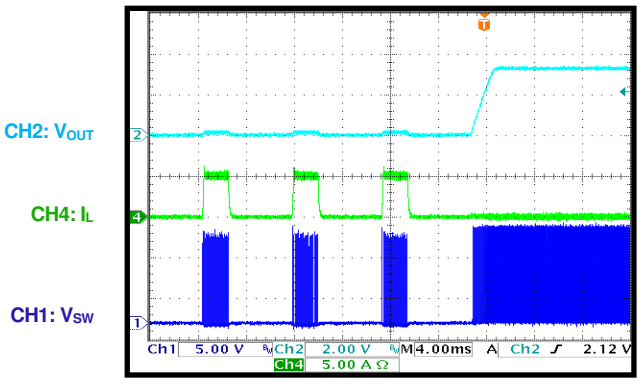
SCP Entry

I_{OUT} = 0.6A to short circuit



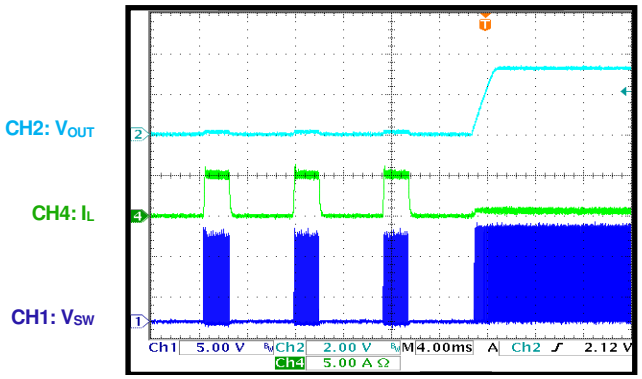
SCP Recovery

Short circuit to I_{OUT} = 0A

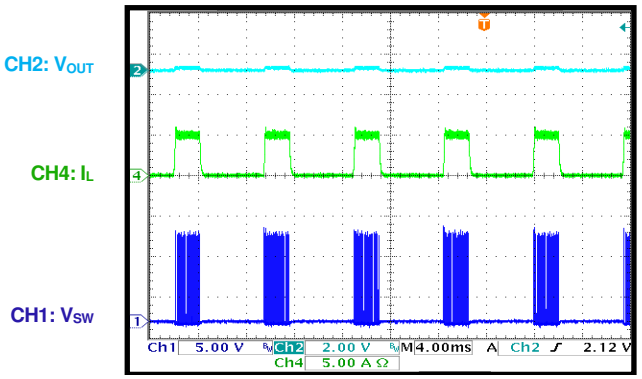


SCP Recovery

Short circuit to I_{OUT} = 0.6A

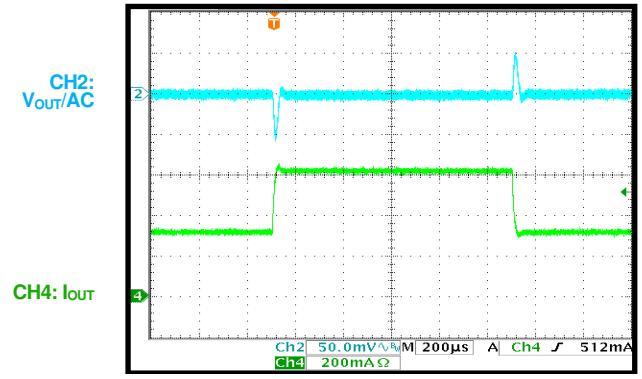


SCP Steady State



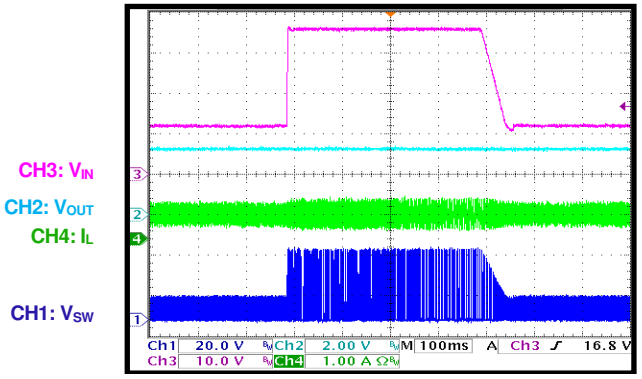
Load Transient

I_{OUT} = 0.3A to 0.6A, 1.6A/µs



Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 0.6A

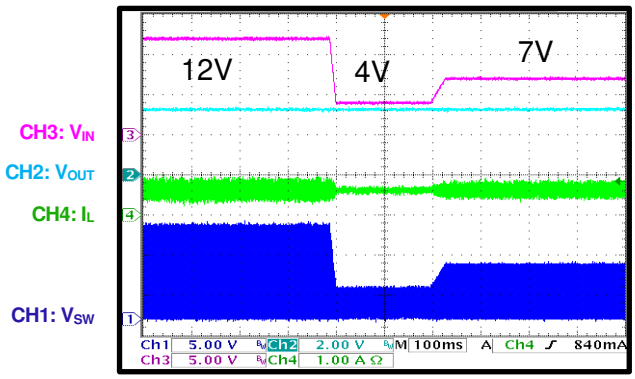


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST} = 20Ω, T_A = 25°C, unless otherwise noted.

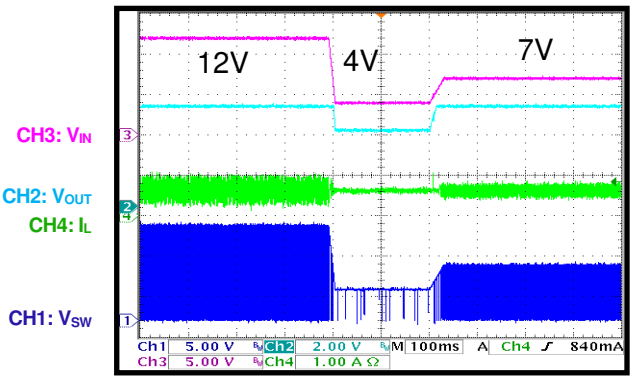
Cold Crank

V_{OUT} = 3.3V, I_{OUT} = 0.6A



Cold Crank

V_{OUT} = 5V, I_{OUT} = 0.6A



FUNCTIONAL BLOCK DIAGRAM

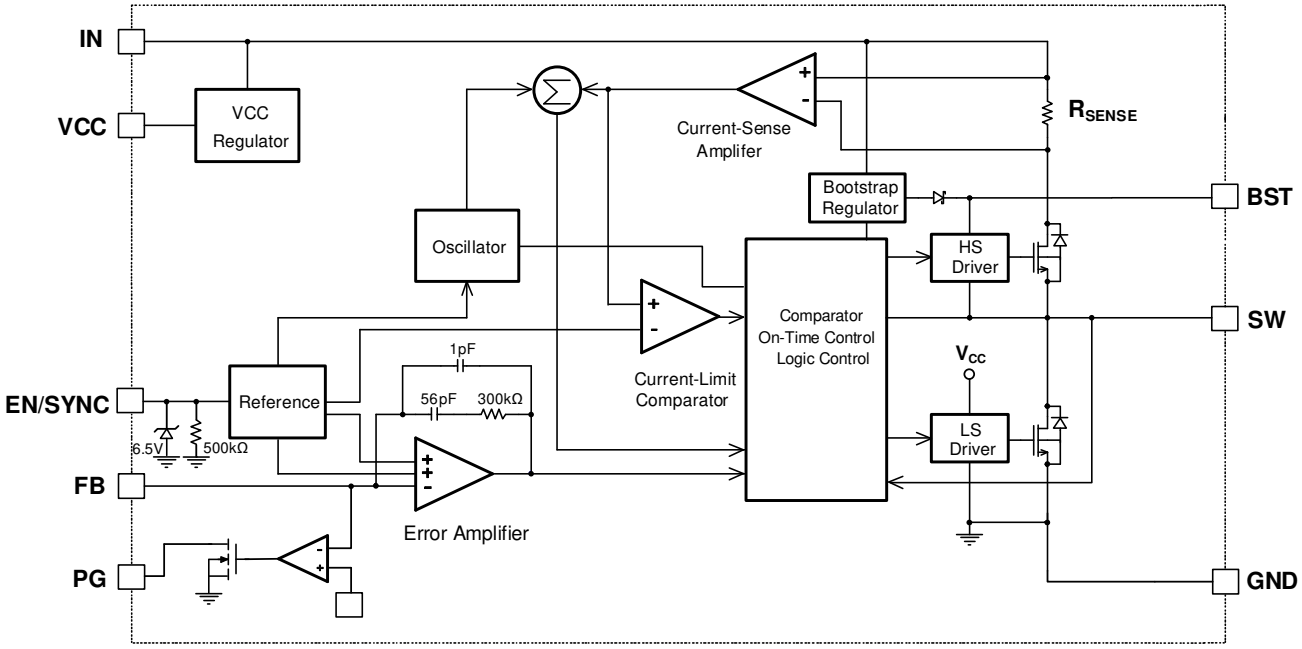


Figure 1: Functional Block Diagram

OPERATION

The MPQ4418A is a high-efficiency, synchronous, rectified, switch-mode, step-down converter with built-in internal power MOSFETs. The MPQ4418A offers a compact solution that achieves up to 0.6A of continuous output current (I_{OUT}) across a wide 4V to 36V input voltage (V_{IN}) range, with excellent load and line regulation.

To regulate the output voltage (V_{OUT}), the MPQ4418A operates in fixed-frequency, peak current control mode. An internal clock initiates the pulse-width modulation (PWM) cycle. If the high-side power MOSFET (HS-FET) turns on, it remains on until the current reaches the value set by the COMP voltage (V_{COMP}). If the HS-FET turns off, it remains off until the next clock cycle begins. If the current in the HS-FET does not reach the set V_{COMP} value within 95% of one PWM period, the HS-FET is forced to turn off.

Internal Regulator

A 5V internal regulator powers most of the internal circuitry. The regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5V, the regulator's output operates in full regulation. When V_{IN} drops below 5V, the output decreases to match V_{IN}. It is recommended to use a 0.1µF ceramic capacitor to decouple VCC.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage (V_{FB}) to the 0.8V internal reference voltage (V_{REF}), then outputs V_{COMP} to control the MOSFET current. This optimized internal compensation network minimizes the need for multiple external components and simplifies control loop design.

Enable/Synchronous (EN/SYNC) Control

EN/SYNC is a digital control pin that turns the regulator on and off. Pull EN/SYNC high to turn the regulator on; pull it low to turn the regulator off. Place a 500kΩ internal resistor from EN/SYNC to GND to float EN/SYNC, which turns off the device.

EN/SYNC is clamped internally by a 6.5V series Zener diode (see Figure 2). Connect the EN/SYNC input to any V_{IN} source via a pull-up resistor. The pull-up resistor limits EN/SYNC's input current to 150µA.

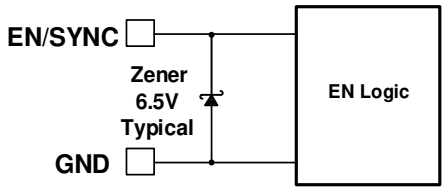


Figure 2: 6.5V Zener Diode

For example, if 12V is connected to V_{IN}, then $R_{PULLUP} \geq (12V - 6.5V) / 150\mu A = 36.7k\Omega$.

To directly connect EN/SYNC to a voltage source without a pull-up resistor, the voltage amplitude must be limited to ≤6V to prevent damage to the Zener diode.

To use the synchronous function, connect a 200kHz to 2.2MHz external clock to EN/SYNC. The external clock must be connected for a minimum of 2ms after V_{OUT} is set. If the external clock is connected, the internal clock's rising edge is synchronized to the external clock's rising edge. The external clock's pulse width signal must be below 1.7µs.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the device from operating at an insufficient supply voltage. The UVLO comparator monitors the internal regulator's V_{OUT}. The UVLO rising threshold is about 3.5V, and the UVLO falling threshold is 3.3V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the device starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1.2V. When V_{SS} drops below V_{REF}, V_{SS} overrides V_{REF}, and the EA then uses V_{SS} as its reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as its reference. The soft-start time (t_{SS}) is internally set to 1.5ms.

Over-Current Protection (OCP) with Hiccup Mode

The MPQ4418A provides cycle-by-cycle over-current protection (OCP) when the inductor's peak current exceeds the current-limit threshold. If V_{FB} drops below the UVLO

threshold (typically 84% below V_{REF}), the MPQ4418A enters hiccup mode and periodically restarts the part. OCP is useful when the output is dead-shorted to GND.

Reducing the average short-circuit current protects the regulator and reduces thermal issues. Once the over-current (OC) condition is removed, the MPQ4418A exits hiccup mode and resumes normal operation.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures. If the silicon die temperature exceeds 170°C, the MPQ4418A shuts down. Once the temperature drops below the low threshold (typically 140°C), the device starts up again and resumes normal operation.

Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor (C_{BST}) powers the floating MOSFET driver. A dedicated internal regulator charges and regulates the C_{BST} voltage at 5V.

If the voltage between the BST and SW nodes drops below the regulation voltage, a P-channel MOSFET pass transistor connected from VIN to BST turns on. The charging current path is from VIN to BST to SW. The external circuit should provide enough voltage headroom to facilitate charging. As long as V_{IN} significantly exceeds V_{SW}, C_{BST} remains charged. If the HS-FET is on, V_{IN} should be approximately equal to V_{SW}. In this scenario, C_{BST} does not charge. If the LS-FET is on, then V_{IN} - V_{SW} reaches its fast charging maximum (see Figure 3).

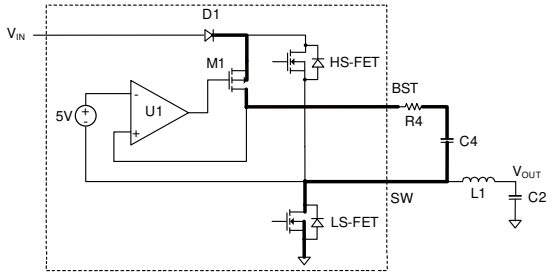


Figure 3: BST Charging Path (LS-FET On)

When the HS-FET and LS-FET are both off, V_{SW} should be equal to V_{OUT}, and the difference between V_{IN} and V_{OUT} charges C_{BST} (see Figure 4).

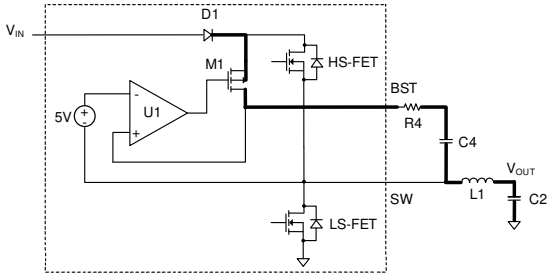


Figure 4: BST Charging Path (HS-FET and LS-FET Off)

The floating driver has its own UVLO protection: a 2.2V rising threshold and 150mV hysteresis. It is recommended to place a 20Ω resistor between SW and C_{BST} to reduce SW voltage spikes.

Start-Up and Shutdown

If both V_{IN} and EN/SYNC exceed their respective thresholds, the MPQ4418A starts up. The reference block turns on first, and generates a stable V_{REF} and current. Subsequently, the internal regulator turns on and provides a stable supply for the remaining circuitries.

Three events can shut down the device: pulling EN/SYNC low, pulling VIN low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Power Good (PG)

The MPQ4418A has a power good (PG) open-drain output. PG should be connected to VCC or another voltage source through a resistor (e.g. 100kΩ). In the presence of V_{IN}, the MOSFET turns on and PG is pulled low before SS is ready. When V_{FB} reaches 90% of V_{REF}, there is a delay (about 90µs), and then PG is pulled high. When V_{FB} drops to 84% of V_{REF}, PG is pulled low. If thermal shutdown occurs or if EN/SYNC is pulled low, then PG is also pulled low.

APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The external resistor divider sets V_{OUT} (see the Typical Application Circuit section on page 16). The feedback (FB) resistor (R1) also sets the FB loop bandwidth via the internal compensation capacitor. Set R1 at about 40kΩ. R2 can then be calculated using Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.792V} - 1} \quad (1)$$

If V_{OUT} is low, it is recommended to use a T-type network (see Figure 5).

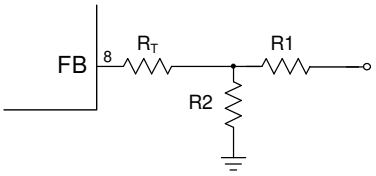


Figure 5: T-Type Network

Add R_T to R1 to set the loop bandwidth. The higher the R_T + R1 value, the lower the loop bandwidth. To ensure loop stability, limit the loop bandwidth to 40kHz (based on the 410kHz default f_{SW}). Table 1 shows the recommended T-type resistor values for common V_{OUT} values.

Table 1: Recommended Resistor Values for Common V_{OUT} Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)
3.3	41.2 (1%)	13 (1%)	100 (1%)
5	41.2 (1%)	7.68 (1%)	100 (1%)

Selecting the Inductor

Use a 1µH to 10µH inductor with a DC current rating that exceeds the maximum load current by at least 25%. For the highest efficiency, use an inductor with a small DC resistance. For most designs, the inductance (L_1) can be calculated using Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Set the inductor ripple current to be about 30% of the maximum load current. The maximum inductor peak current ($I_{L(MAX)}$) can be calculated using Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Use a larger inductor for improved efficiency under light-load conditions (below 100mA).

Input Voltage (V_{IN}) UVLO Setting

The MPQ4418A has an internal, fixed UVLO threshold. The UVLO rising threshold is 3.5V, and the UVLO falling threshold is about 3.3V. For applications that require a higher UVLO level, place an external resistor divider between EN/SYNC and IN to achieve a higher equivalent UVLO threshold (see Figure 6).

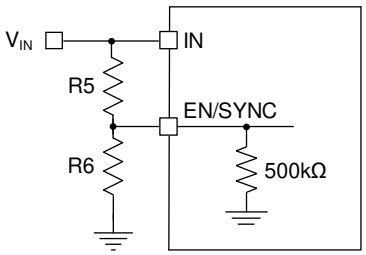


Figure 6: Configurable UVLO with EN/SYNC Divider

The UVLO rising threshold can be calculated using Equation (4):

$$V_{IN\_UVLO\_RISING} = (1 + \frac{R5}{500k\Omega // R6}) \times V_{EN\_RISING} \quad (4)$$

Where V_{EN_RISING} is 1.4V.

The UVLO falling threshold can be calculated using Equation (5):

$$V_{IN\_UVLO\_FALLING} = (1 + \frac{R5}{500k\Omega // R6}) \times V_{EN\_FALLING} \quad (5)$$

Where $V_{EN\_FALLING}$ is 1.25V.

Ensure that R5 is large enough to limit the current flowing into EN/SYNC, which is below 150µA.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while also maintaining the DC input voltage. It is recommended to use ceramic capacitors with X5R or X7R dielectrics due to their low ESR and small temperature coefficients.

For most applications, a 22µF ceramic capacitor is sufficient to maintain the DC input voltage. Use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to IN and GND as possible (see the PCB Layout Guidelines section on page 15).

An adequate ripple current rating is required because the input capacitor (C1) absorbs the input switching current. The RMS current in C1 (I_{C1}) can be estimated using Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case scenario occurs at $V_{IN} = 2 \times V_{OUT}$, which can be estimated using Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

Select a capacitor with an RMS current rating that exceeds half of the maximum load current.

C1 can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 1µF) as close to the IC as possible. Ensure that the ceramic capacitors have enough capacitance to provide sufficient charge and prevent excessive input voltage ripple (ΔV_{IN}). ΔV_{IN} is caused by the capacitance, and can be estimated using Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. It is recommended to use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to prevent excessive output voltage ripple (ΔV_{OUT}). ΔV_{OUT} can be estimated using Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (9)$$

Where L_1 is the inductor value, and R_{ESR} is the C2 equivalent series resistance (ESR) value.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency (f_{SW}) and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated using Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of C2 also affect the stability of the regulation system. The MPQ4418A can be optimized for a wide range of capacitances and ESR values.

BST Resistor and External BST Diode

It is recommended to use a 20Ω resistor in series with a BST capacitor (C_{BST}) to reduce SW voltage spikes. Using a higher resistance helps reduce SW voltage spikes, but can compromise efficiency.

An external BST diode can enhance the regulator's efficiency when the duty cycle is high (above 65%). Use a 2.5V to 5V power supply to power the external BST diode. Either V_{CC} or V_{OUT} can be used as the power supply in the circuit (see Figure 7).

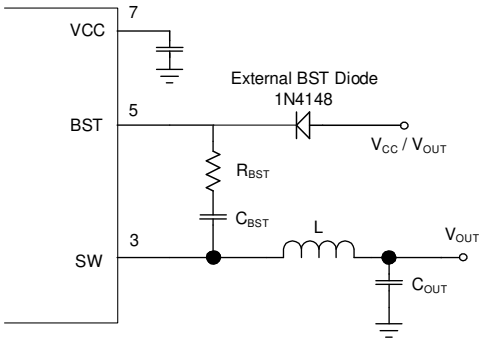


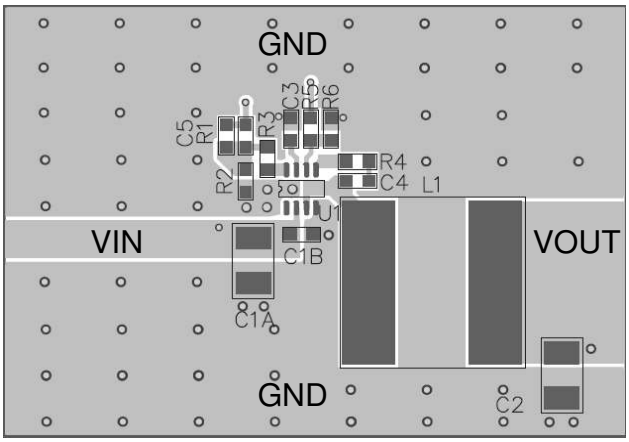
Figure 7: Optional External BST Diode for Enhanced Efficiency

It is recommended to use an IN4148 external BST diode. The recommended C_{BST} value is 0.1µF to 1µF.

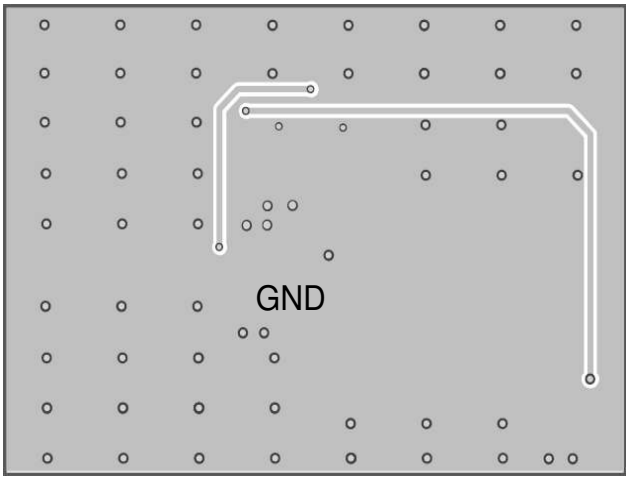
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 8 and follow the guidelines below:

1. Place C1 as close to IN and GND as possible.
2. Keep the connection between C1 and IN as short and wide as possible.
3. Place the VCC capacitor as close to VCC and GND as possible.
4. Keep the trace length from the VCC capacitor to GND as short as possible.
5. Connect a large ground plane directly to GND.
6. If the ground plane is the bottom layer, place vias around GND.
7. Route SW and BST away from sensitive analog areas, such as FB.
8. Place the T-type FB resistor close to the chip to ensure that the trace connecting to FB is as short as possible.



Top Layer



Bottom Layer

Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

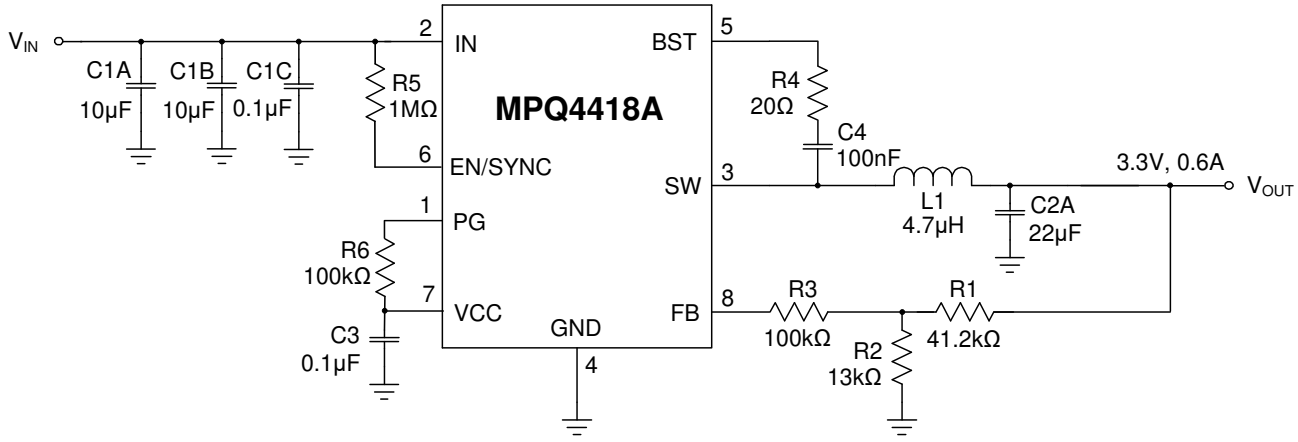
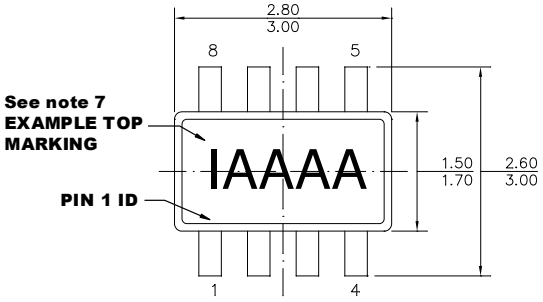


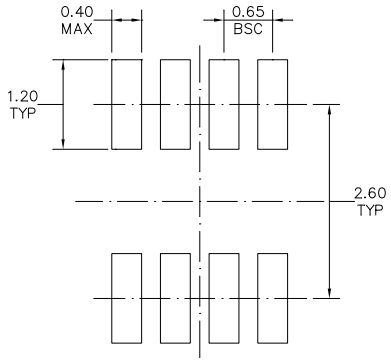
Figure 9: Typical Application Circuit (V_{OUT} = 3.3V)

PACKAGE INFORMATION

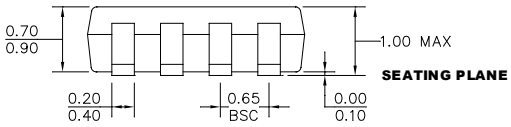
TSOT23-8



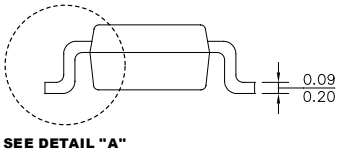
TOP VIEW



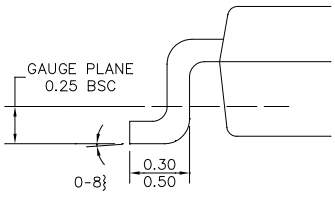
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

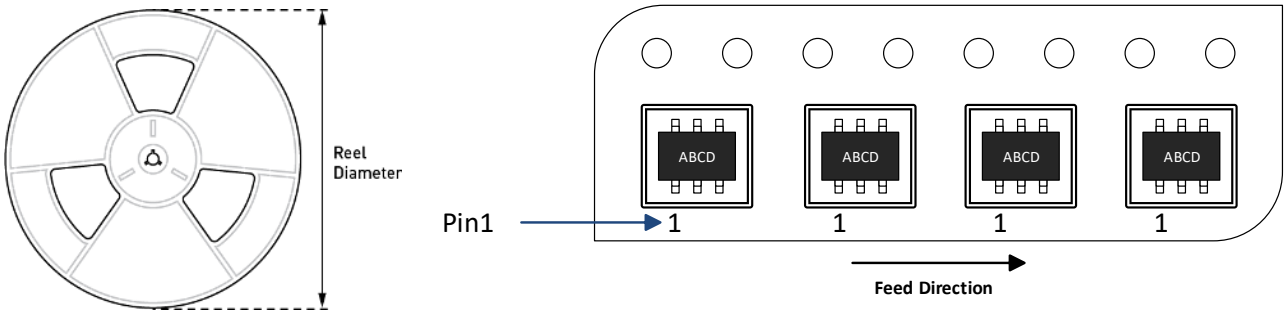


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.1 MILLIMETERS MAXIMUM.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) WHEN READING THE TOP MARKING FROM LEFT TO RIGHT, PIN 1 IS THE LOWER LEFT PIN (SEE EXAMPLE TOP MARKING).

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4418AGJ-AEC1-Z	TSOT23-8	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/09/2021	Initial Release	-