

## Evaluation Board for the Integer-N PLL Frequency Synthesizer

### FEATURES

General-purpose PLL evaluation board excluding VCO, loop filter, and TCXO

Contains **ADF4002** 400 MHz frequency synthesizer IC

Accompanying software allows complete control of synthesizer functions from a PC

### EVALUATION KIT CONTENTS

**EV-ADF4002SD1Z** board

CD that includes

Self-installing software that allows users to control the board and exercise all functions of the device

Electronic version of the **ADF4002** data sheet

Electronic version of the **UG-108** user guide

### ADDITIONAL EQUIPMENT

PC running Windows XP or more recent version

SDP-S board (system demonstration platform, serial only)

T-package VCO

0805 resistors and capacitors

Spectrum analyzer

Oscilloscope (optional)

### DOCUMENTS NEEDED

**ADF4002** data sheet

### REQUIRED SOFTWARE

Analog Devices Int-N software (Version 7 or higher)

**ADIsimPLL**

### GENERAL DESCRIPTION

This board is designed to allow the user to evaluate the performance of the **ADF4002** frequency synthesizer for phase-locked loops (PLLs). Figure 1 shows the board, which contains the footprint for an **ADF4002** synthesizer, an SMA connector for the reference input, power supplies, and an RF output. There is also a footprint for a loop filter and a VCO on board.

The evaluation kit also contains software that is compatible with Windows® XP and later versions to allow easy programming of the synthesizer.

This board requires an SDP-S (system demonstration platform-serial) board (shown in Figure 1, but not supplied with the kit). The SDP-S allows software programming of the **ADF4002** device.

### EVALUATION BOARD

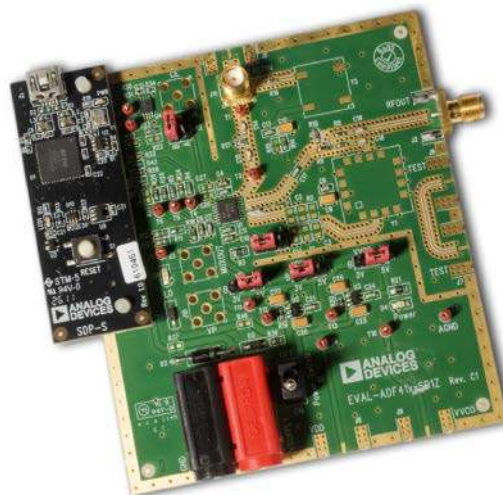


Figure 1. **EV-ADF4002SD1Z** with SDP-S

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**REVISION HISTORY**

**12/11—Rev. 0 to Rev. A**

Changes to Features and General Description Sections and Figure 1 .....

Added Evaluation Kit Contents, Additional Equipment, Documents Needed, and Required Software Sections .....

Added Quick Start Guide Section .....

Deleted Figure 3; Renumbered Sequentially.....

Replaced Hardware Description Section with Evaluation Board Hardware Section .....

Changes to Power Supplies Section and Figure 2.....

Added Input Signals Section and Output Signals Section .....

Added Default Operation and Jumper Selection Settings Section and System Demonstration Platform (SDP) Section.....

Added Table 1; Renumbered Sequentially .....

Added Evaluation Board Setup Procedure Section.....

Added Figure 3 and Figure 4; Renumbered Sequentially .....

Added Figure 5 to Figure 9.....

Added Figure 10 to Figure 14 .....

Added Figure 15 to Figure 16 .....

Replaced Software Description Section with Evaluation Board Software Section .....

Changes to Figure 17.....

Added Figure 18 .....

Added Evaluation and Test Section, Figure 19, and Figure 20 .....

Changed Schematics Heading to Evaluation Board Schematics and Artwork .....

Changes to Figure 21.....

Changes to Figure 22.....

Added Figure 23 .....

Added Figure 24 .....

Added Figure 25 .....

Added Figure 26 .....

Added Figure 27 .....

Changes to Table 2.....

**9/10—Revision 0: Initial Version**

## QUICK START GUIDE

Follow these steps to quickly evaluate the [ADF4002](#) device:

1. Solder the VCO (T-package compatible).
2. Solder the loop filter components (design with ADIsimPLL™).
3. Connect the reference frequency to J11.
4. Install the system development platform (SDP) drivers.
5. Install the Int-N software.
6. Connect the SDP-S motherboard to the PC and to the [EV-ADF4002SD1Z](#).
7. Follow the hardware driver installation procedure.
8. Connect the power supplies to banana connectors (6 V to 12 V).
9. Run the Int-N software.
10. Select the SDP board and the [ADF4002](#) device in the **Select Device and Connection** tab of the software front panel window.
11. Click the **Main Controls** tab. Update all registers.
12. Connect the spectrum analyzer to J2.
13. Measure the results.

## EVALUATION BOARD HARDWARE

The evaluation board requires the use of an SDP-S motherboard to program the device. This is not included and must be purchased separately. The [EV-ADF4002SD1Z](#) schematics are shown in Figure 21, Figure 22, and Figure 23.

### POWER SUPPLIES

The board is powered from external banana connectors. The voltage can vary between 6 V and 12 V. The power supply circuit provides 3.0 V to the [ADF4002](#)  $V_{DD}$  and allows the user to choose either 3.0 V or 5 V for the [ADF4002](#)  $V_P$ . The default settings are 3.0 V for the [ADF4002](#)  $V_{DD}$  and 5 V for the [ADF4002](#)  $V_P$ . Note that  $V_{DD}$  should never exceed 3.3 V. This can damage the device.

External power supplies can be used to directly drive the device. In this case, the user must insert SMA connectors as shown in Figure 2.

### INPUT SIGNALS

The necessary reference input can be sourced from an external generator. A low noise, high slew rate reference source is best for achieving the stated performance of the [ADF4002](#). This reference source can be connected to Connector J11. If preferred, the edge mount connector, J5, can be inserted and used instead. A third option is to solder a footprint-compatible TCXO to Footprint Y2. To use this option, connect 0  $\Omega$  links to R16 and R14.

Digital SPI signals are supplied through the SDP connector, J1. Using the SDP-S platform is recommended. The SDP\_B can also be used, but Resistor R57 must be removed on the SDP-B board. Some additional spurious low frequencies may appear if the SDP-B connector is used.

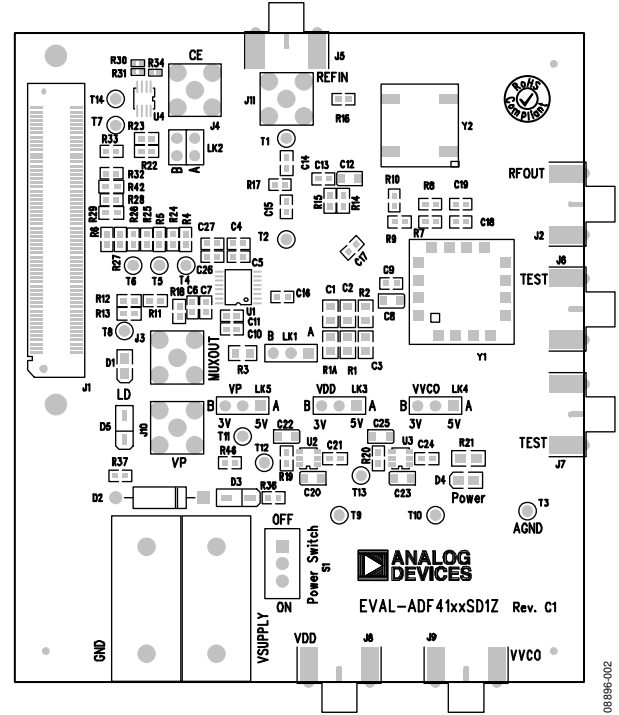


Figure 2. Evaluation Board Silkscreen

### OUTPUT SIGNALS

All components necessary for LO generation can be inserted on board. The PLL is made up of the [ADF4002](#) synthesizer, a passive loop filter, and the VCO. The package containing the VCO must be a T-package (or similar). A low-pass filter must be inserted between the charge pump output and the VCO input. In this case, the user must insert the relevant parts as shown in Figure 2. The VCO output is available at RFOUT through a standard SMA connector, J2. The MUXOUT signal can be monitored at Test Point T8 or at SMA Connector J3.

## DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This board is shipped without a TCXO, low-pass filter, or a VCO. Users must insert suitable components to complete a PLL. Link positions are outlined in Table 1.

**Table 1. Link Positions and Function**

Link	Position	Options	Description
LK1	A	R1A	Not used
	B	RSET	Normal operation
LK2	A	GND	Hardware power-down
	B	VDD	Normal operation
LK3 (V <sub>DD</sub> )	A	5V	Not used
	B	3V	Normal operation
LK4 (V <sub>VCO</sub> )	A	5V	VCO supply 5 V
	B	3V	VCO supply 3 V
LK5 (V <sub>P</sub> )	A	5V	V <sub>P</sub> supply 5 V
	B	3V	V <sub>P</sub> supply 3 V

## SYSTEM DEMONSTRATION PLATFORM (SDP)

The system demonstration platform (SDP) is a series of controller boards, interposer boards, and daughter boards that can be used for easy low cost evaluation of Analog Devices, Inc., components and reference circuits. It is a reusable platform whereby a single controller board can be reused in various daughter board evaluation systems.

Controller boards connect to the PC via USB 2.0 and provide a range of communication interfaces on a 120-pin connector.

The pinout for this connector is strictly defined. This 120-pin connector's receptacle is on all SDP daughter boards, component evaluation boards, and Circuits from the Lab™ reference circuit boards. There are two controller boards in the platform: the SDP-B, which is based on the Blackfin® [ADSP-BF527](#), and the SDP-S, which is a serial interface only controller board. The SDP-S has a subset of the SDP-B functionality.

Interposer boards route signals between the SDP 120-pin connector and a second connector. When the second connector is also a 120-pin connector, the interposer can be used for signal monitoring of the 120-pin connector signals. Alternatively, the second connector allows SDP platform elements to be integrated into a second platform, for example, the BeMicro SDK. More information on the SDP can be found at [www.analog.com/sdp](http://www.analog.com/sdp).

## EVALUATION BOARD SETUP PROCEDURE

### SOFTWARE INSTALLATION

Use the following steps to install the SDP drivers and Int-N software.

1. Install the SDP drivers by double-clicking **SDPDrivers.exe** and following the relevant installation instructions. See the [UG-291](#) for further instructions on installation of the SDP-S platform or the [UG-277](#) if the SDP-B platform is used.
2. Install the Analog Devices Int-N software by double-clicking **ADI\_Int-N\_Setup.msi**.

If you are using Windows XP, follow the instructions in the Windows XP Software Installation Guide section (see Figure 3 to Figure 7).

If you are using Windows Vista or Windows 7, follow the instructions in the Windows Vista and Windows 7 Software Installation Guide section (see Figure 8 to Figure 12).

Note that the software requires Microsoft Windows Installer and Microsoft .NET Framework 3.5 (or higher). The installer connects to the Internet and downloads Microsoft .NET Framework automatically. Alternatively, before running the **ADI\_Int-N\_Setup.msi**, both the installer and .NET Framework can be installed from the CD provided.

3. Connect your SDP board (black) or USB adapter board (green) by USB. If you are using an SDP board, the drivers install automatically, and you are ready to run the software. If you are using a USB adapter board on Windows XP, follow the steps in the Windows XP Driver Installation Guide section (see Figure 13 to Figure 16). On Windows Vista or Windows 7, the drivers install automatically.

#### Windows XP Software Installation Guide

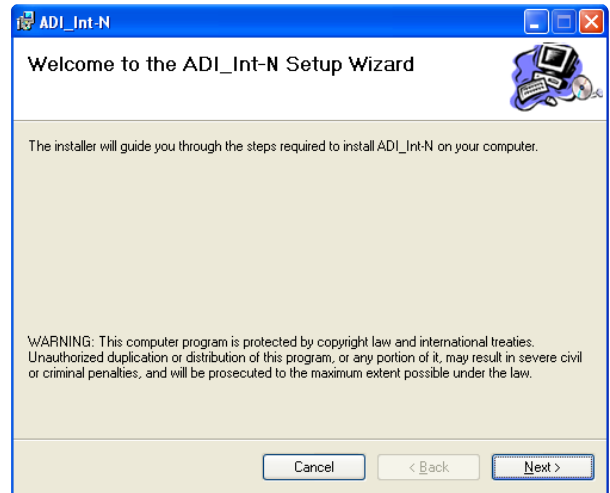


Figure 3. Windows XP Int-N Software Installation, Setup Wizard

1. Click **Next**.

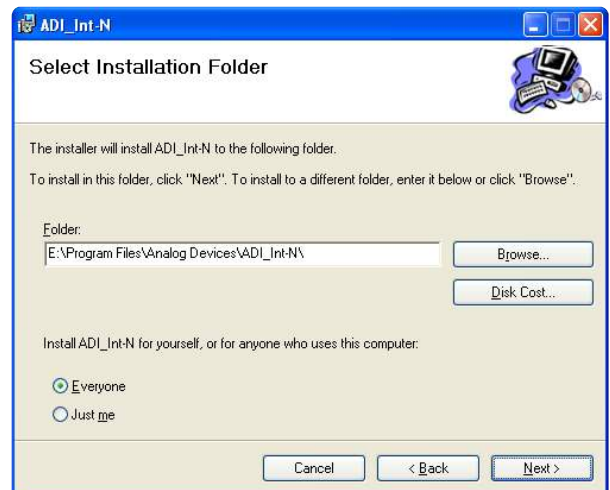


Figure 4. Windows XP Int-N Software Installation, Select Installation Folder

2. Choose an installation directory and click **Next**.

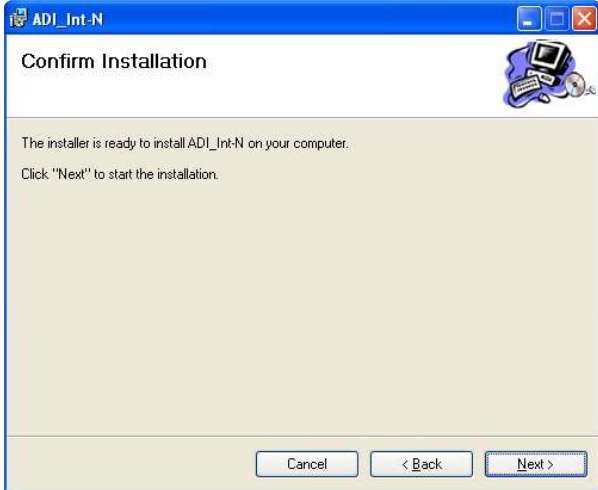


Figure 5. Windows XP Int-N Software Installation, Confirm Installation

3. Click **Next**.

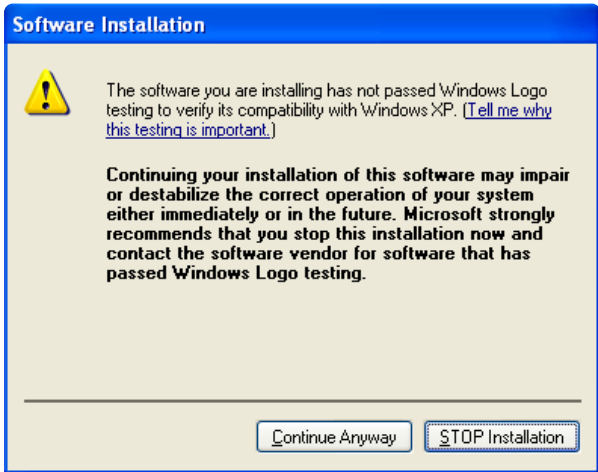


Figure 6. Windows XP Int-N Software Installation, Logo Testing

4. Click **Continue Anyway**.

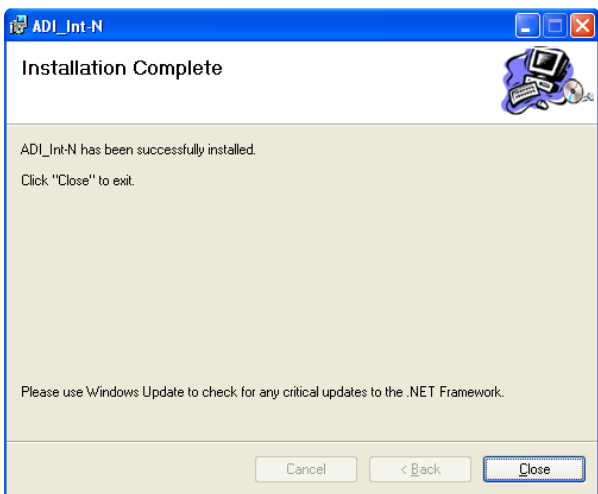


Figure 7. Windows XP Int-N Software Installation, Installation Complete

5. Click **Close**.

**Windows Vista and Windows 7 Software Installation Guide**



Figure 8. Windows Vista/7 Int-N Software Installation, Setup Wizard

1. Click **Next**.



Figure 9. Windows Vista/7 Int-N Software Installation, Select Installation Folder

2. Choose an installation directory and click **Next**.



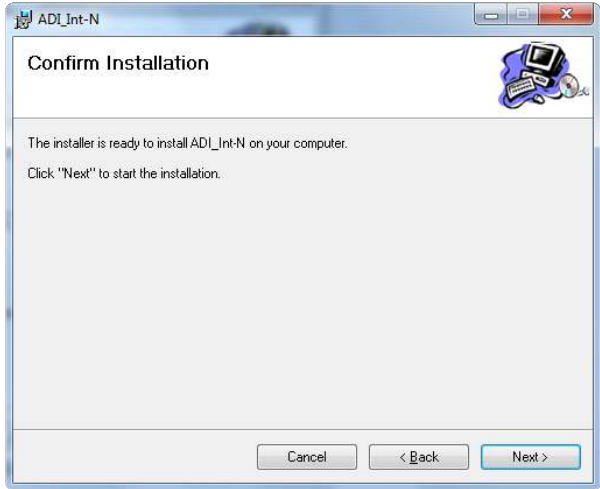


Figure 10. Windows Vista/7 Int-N Software Installation, Confirm Installation

3. Click Next.

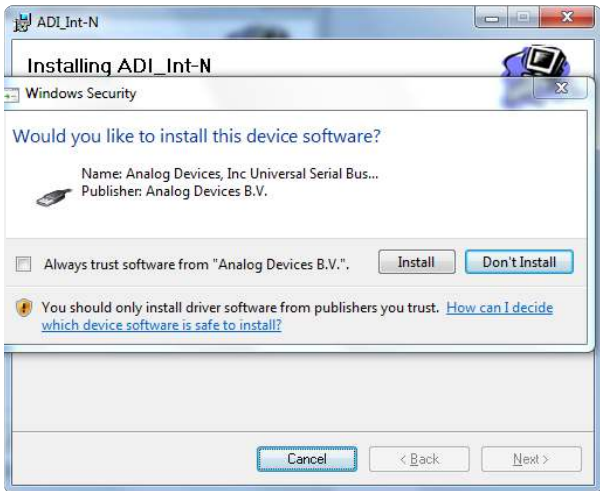


Figure 11. Windows Vista/7 Int-N Software Installation, Start Installation

4. Click Install.

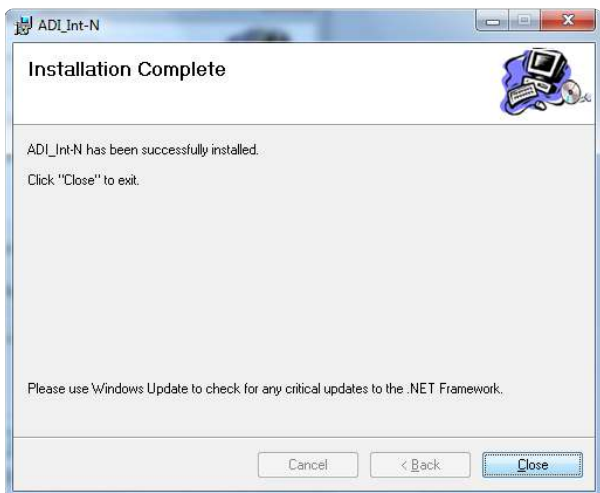


Figure 12. Windows Vista/7 Int-N Software Installation, Installation Complete

5. Click Close.

**Windows XP Driver Installation Guide**

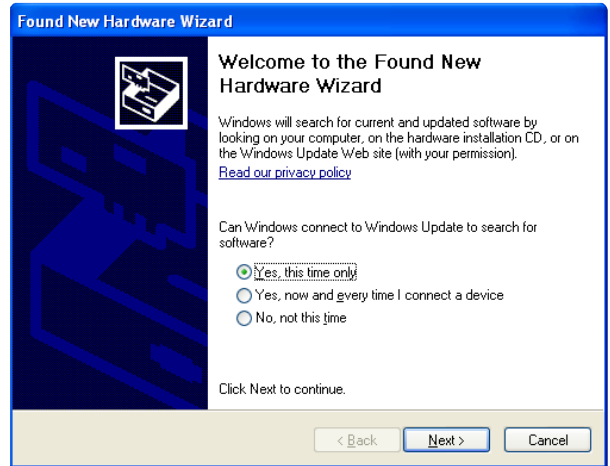


Figure 13. Windows XP USB Adapter Board Driver Installation, Found New Hardware Wizard

1. Choose Yes, this time only and click Next.

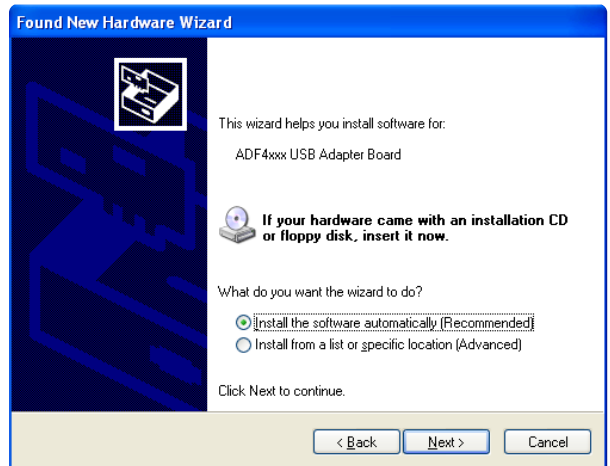
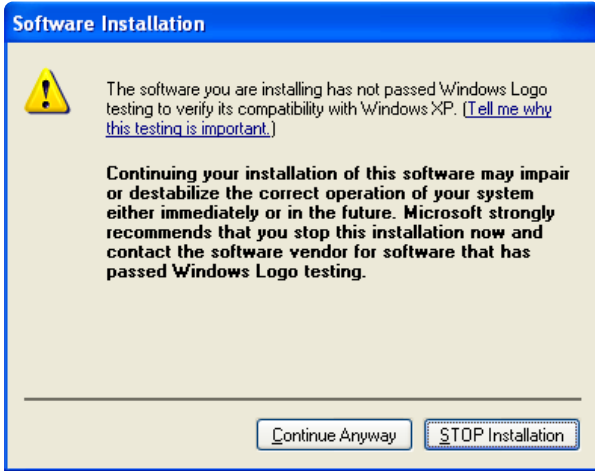


Figure 14. Windows XP USB Adapter Board Driver Installation, Installation Options

2. Click Next.

Note that Figure 14 may list **Analog Devices RFG.L Eval Board** instead of **ADF4xxx USB Adapter Board**.

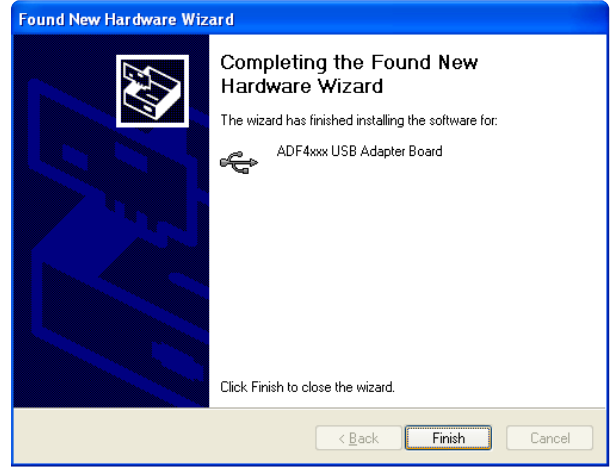




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Figure 15. Windows XP USB Adapter Board Driver Installation, Logo Testing

3. Click **Continue Anyway**.



08896-016

Figure 16. Windows XP USB Adapter Board Driver Installation, Complete Installation

4. Click **Finish**.

## EVALUATION BOARD SOFTWARE

The control software for the [EV-ADF4002SD1Z](#) accompanies the [EV-ADF4002SD1Z](#) on a CD. To install the software, see the Software Installation section.

To run the software, click the **ADI PLL Int-N** file on the desktop or in the **Start** menu.

On the **Select Device and Connection** tab, choose your device and your connection method, and click **Connect**.

Confirm that **SDP board connected, ADF4xxx USB Adapter Board connected,** or **Analog Devices RFG.L Eval Board**

**connected** is displayed at the bottom left of the window (see Figure 17). Otherwise, the software has no connection to the evaluation board.

Note that, when connecting the board, it takes about 5 sec to 10 sec for the status label to change.

Under the **File** menu, the current settings can be saved to, and loaded from, a text file.

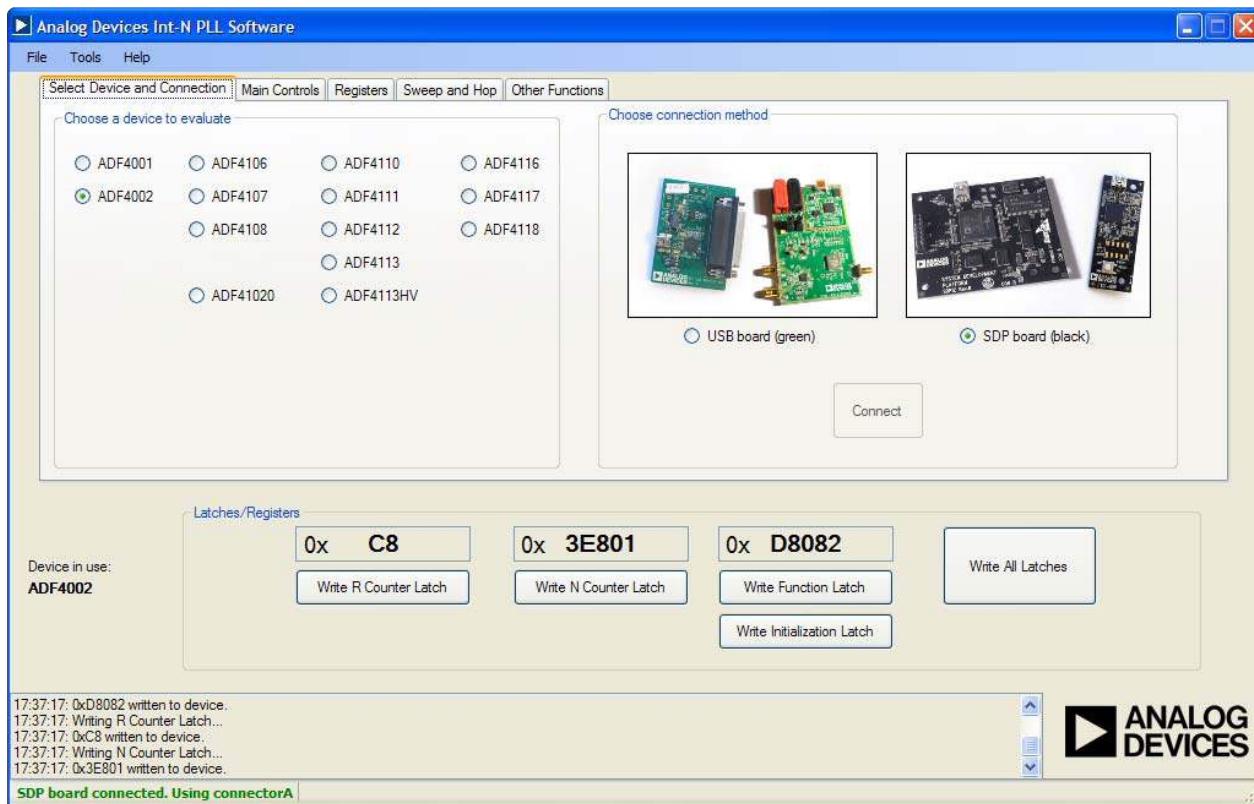


Figure 17. Software Front Panel Display—Select Device and Connection

The **Main Controls** tab controls the PLL settings (see Figure 18).

Use the **Reference Frequency** text box to set the correct reference frequency and the reference frequency divider. The default reference on the software window is at 10 MHz.

Use the **RF Settings** section to control the output frequency. You can type the desired output frequency in the **RF VCO Output Frequency** text box (in megahertz).

In the **Registers** tab, you can manually input the desired value to be written to the registers.

In the **Sweep and Hop** tab, you can make the device sweep a range of frequencies or hop between two set frequencies.

In the **Latches/Registers** section at the bottom of the window, the values to be written to each register are displayed. If the background on the text box is green, the value displayed is different from the value actually on the device. Click **Write R Counter Latch** or **Write N Counter Latch** to write that value to the device.

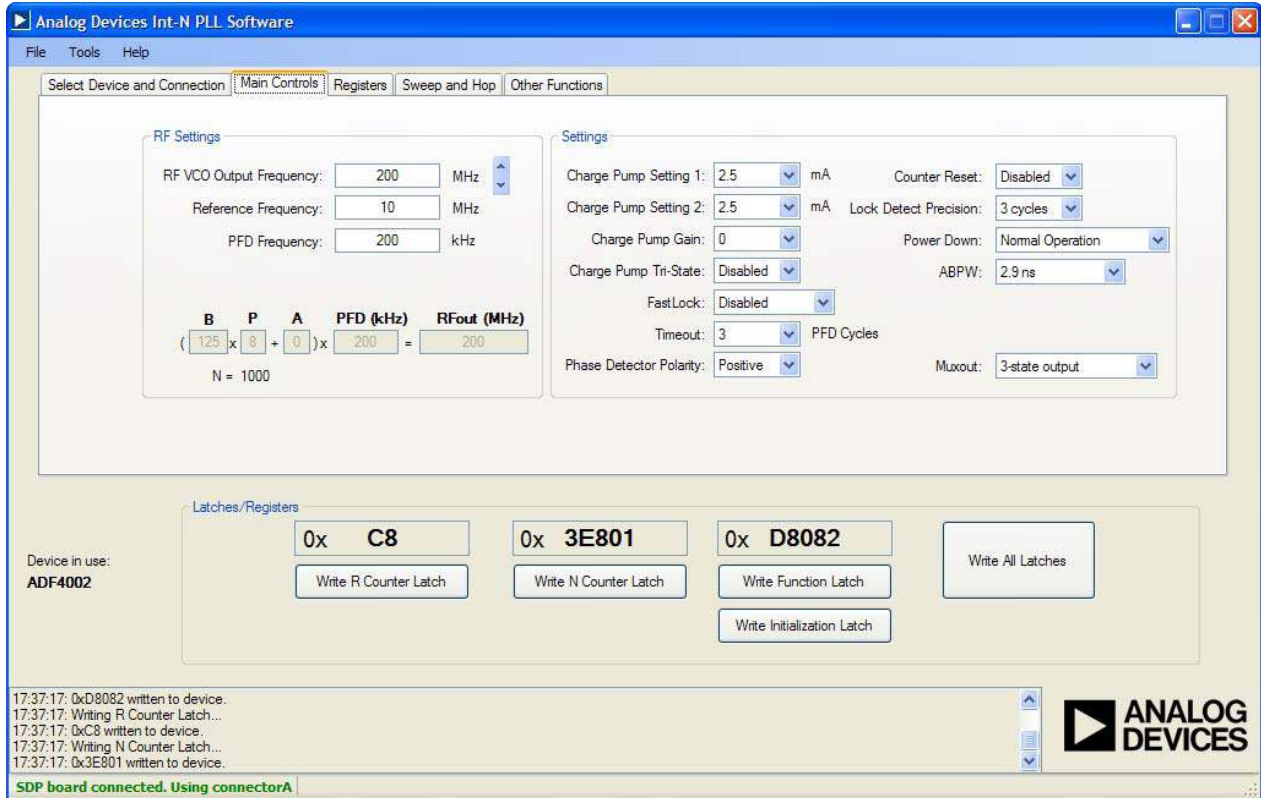


Figure 18. Software Front Panel Display—Main Controls

## EVALUATION AND TEST

To evaluate and test the performance of the ADF4002, use the following procedure:

1. Ensure that a VCO and loop filter are inserted on the board. Use ADIsimPLL to generate the loop filter component values.
2. Install the SDP-S software drivers. Connect the evaluation board to a PC using the supplied USB cable. Follow the hardware driver installation procedure that appears.
3. Connect the SDP-S connector to the [EV-ADF4002SD1Z](#).
4. Connect a reference signal to J11 (or J5, if an edge mount connector is inserted).
5. Connect a spectrum analyzer to Connector J2.
6. Run the Int-N software.
7. Select the SDP board and the [ADF4002](#) device in the **Select Device and Connection** tab of the software front panel window.
8. In the software window, set the VCO center frequency (Figure 19 uses a 400 MHz VCO). Set the PFD frequency as defined in ADIsimPLL, and program the reference frequency to equal that supplied to Connector J11 (or the TCXO). See Figure 20 for the suggested setup.

9. Measure the output spectrum. Figure 19 shows a 400 MHz output.

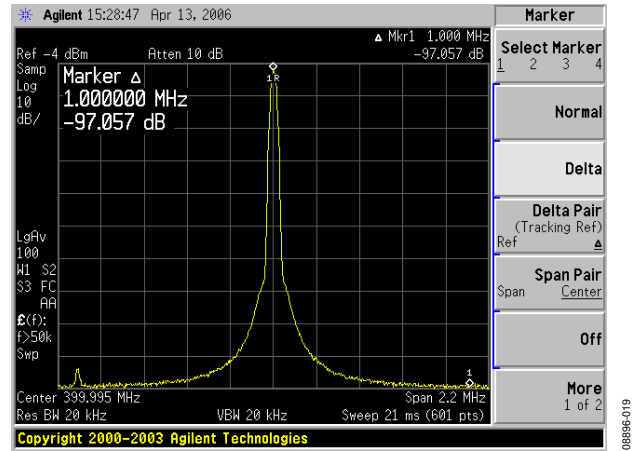


Figure 19. Spectrum Analyzer Display

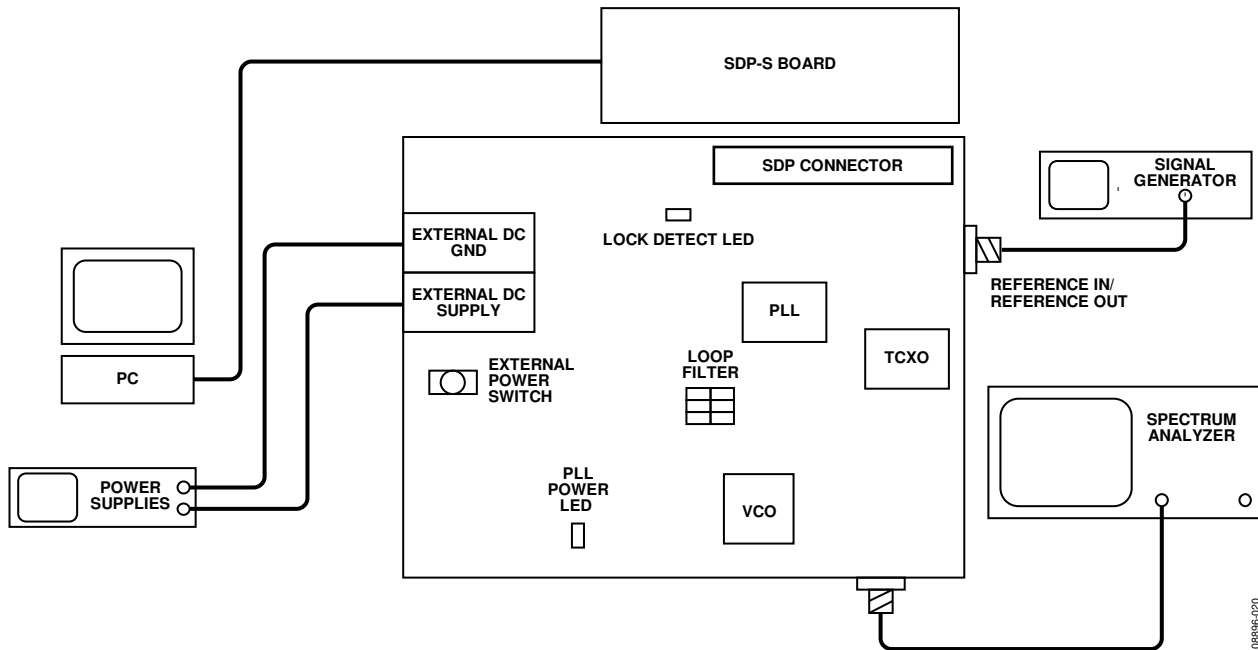


Figure 20. Typical Evaluation Setup

EVALUATION BOARD SCHEMATICS AND ARTWORK

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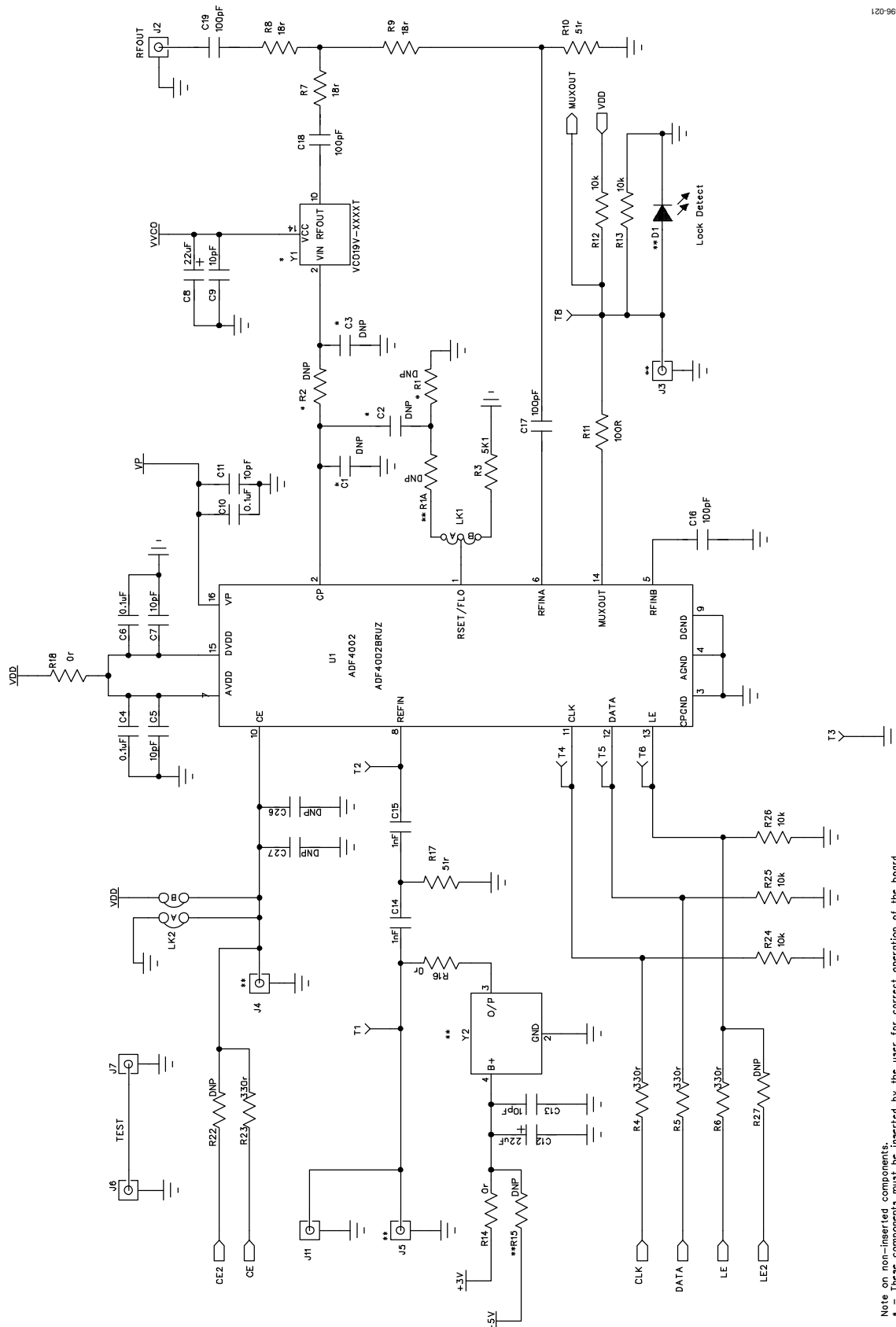


Figure 21. Evaluation Board Schematic (Page 1)

Note on non-inserted components:  
 \* - These components are not inserted by the user for correct operation of the board.  
 \*\* - These components can be inserted by the user for expansion purposes.



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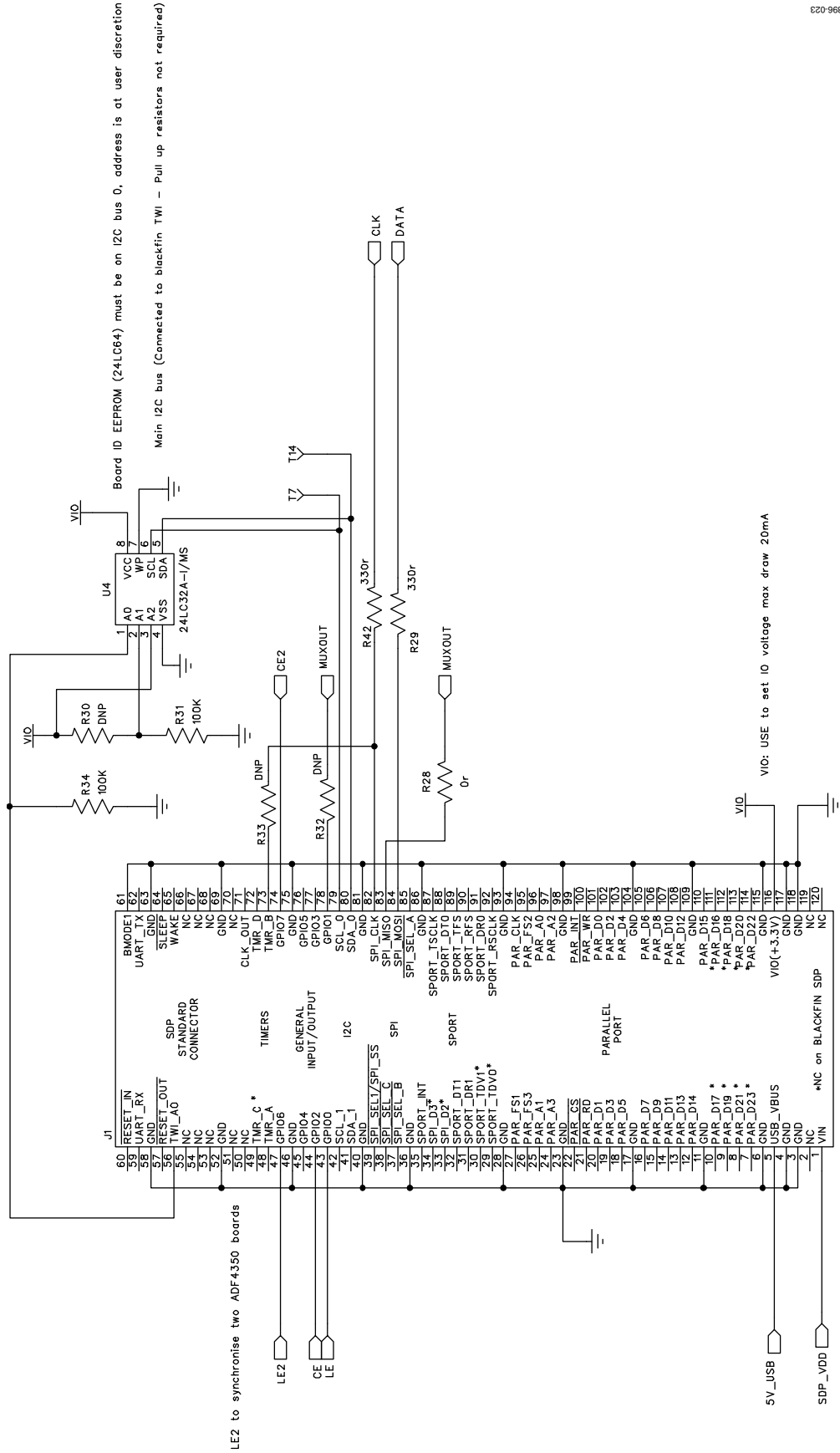


Figure 23. Evaluation Board Schematic (Page 3)



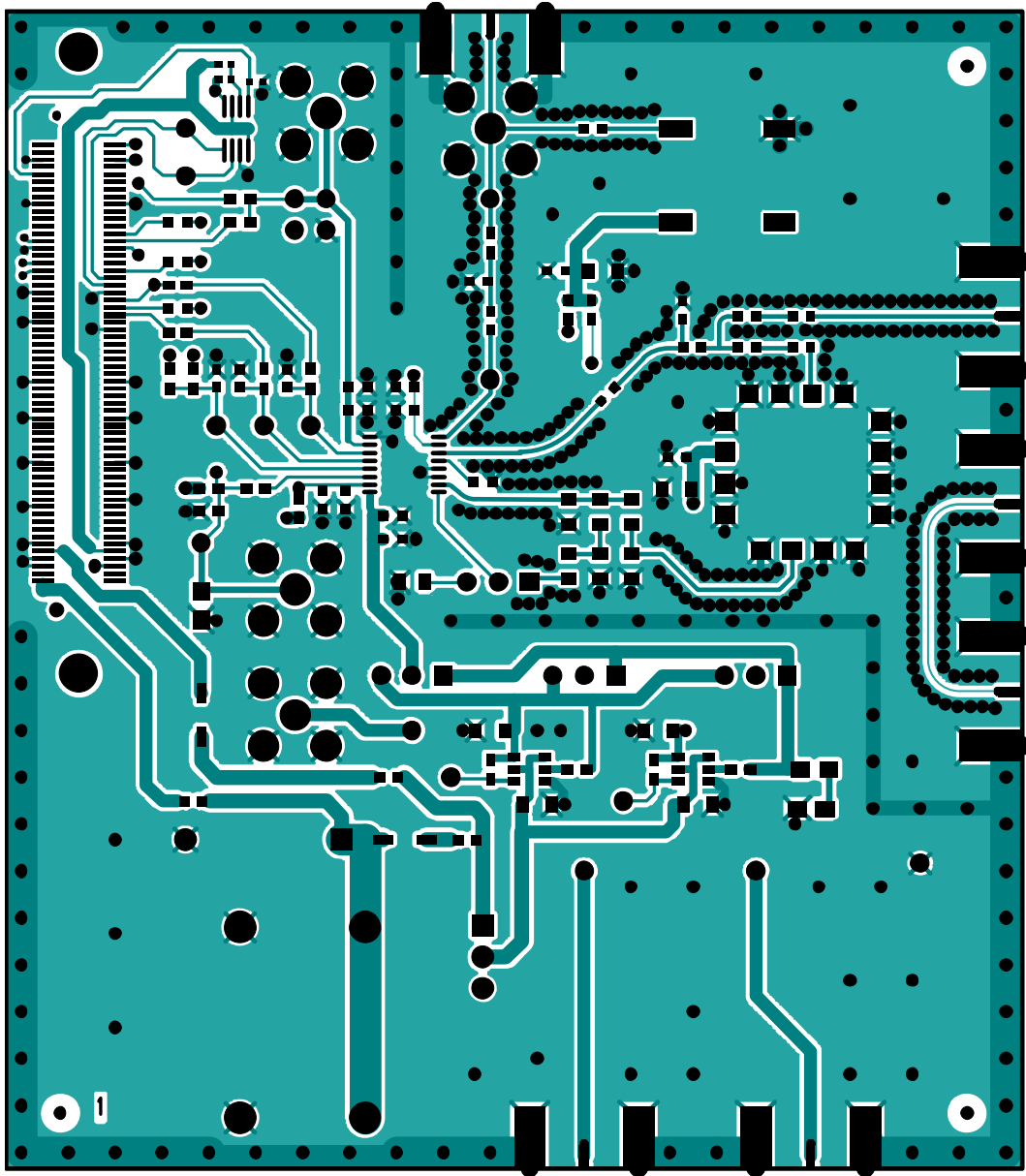


Figure 24. Layer 1 (Component Side)

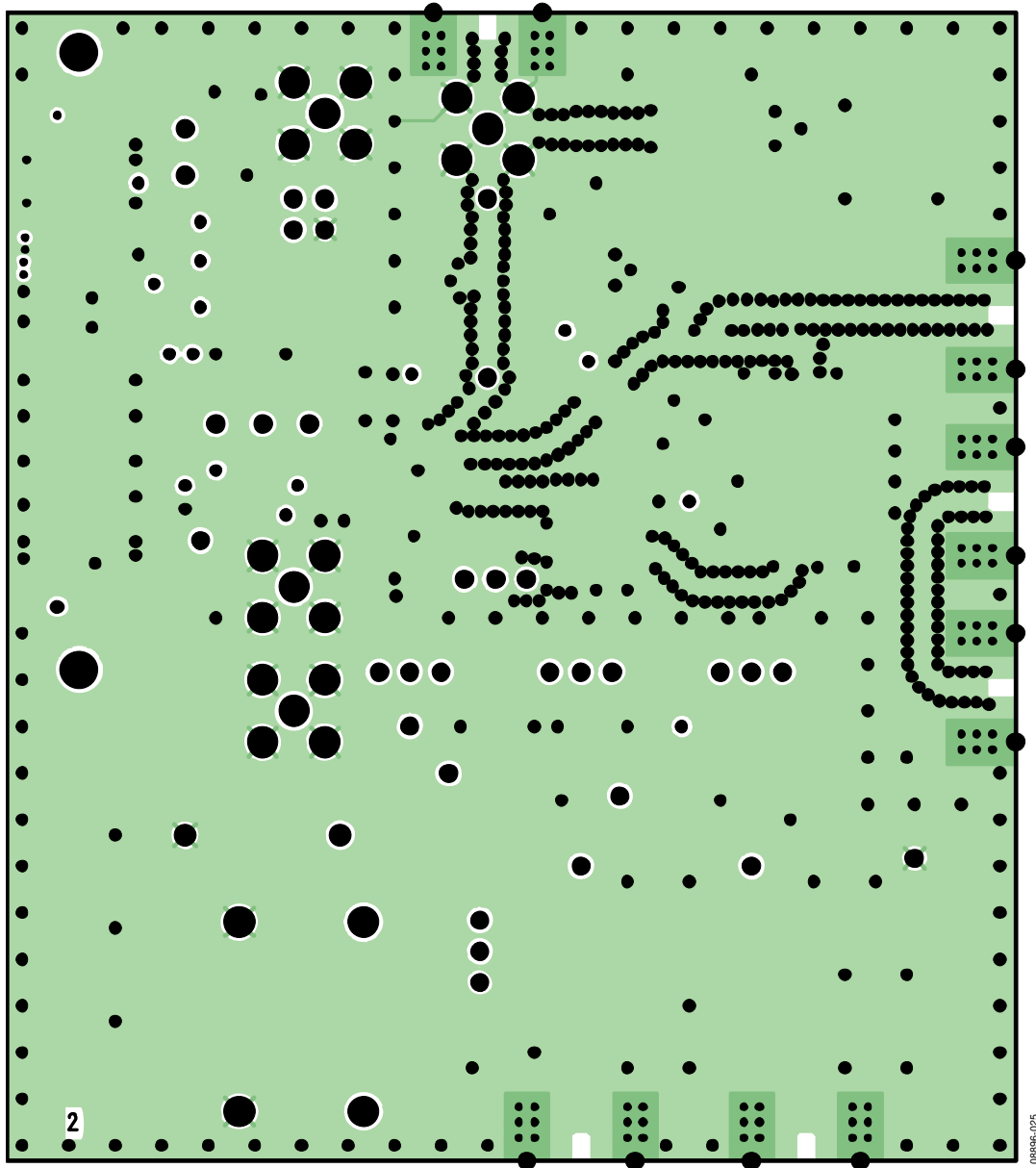


Figure 25. Layer 2 (Ground Plane)

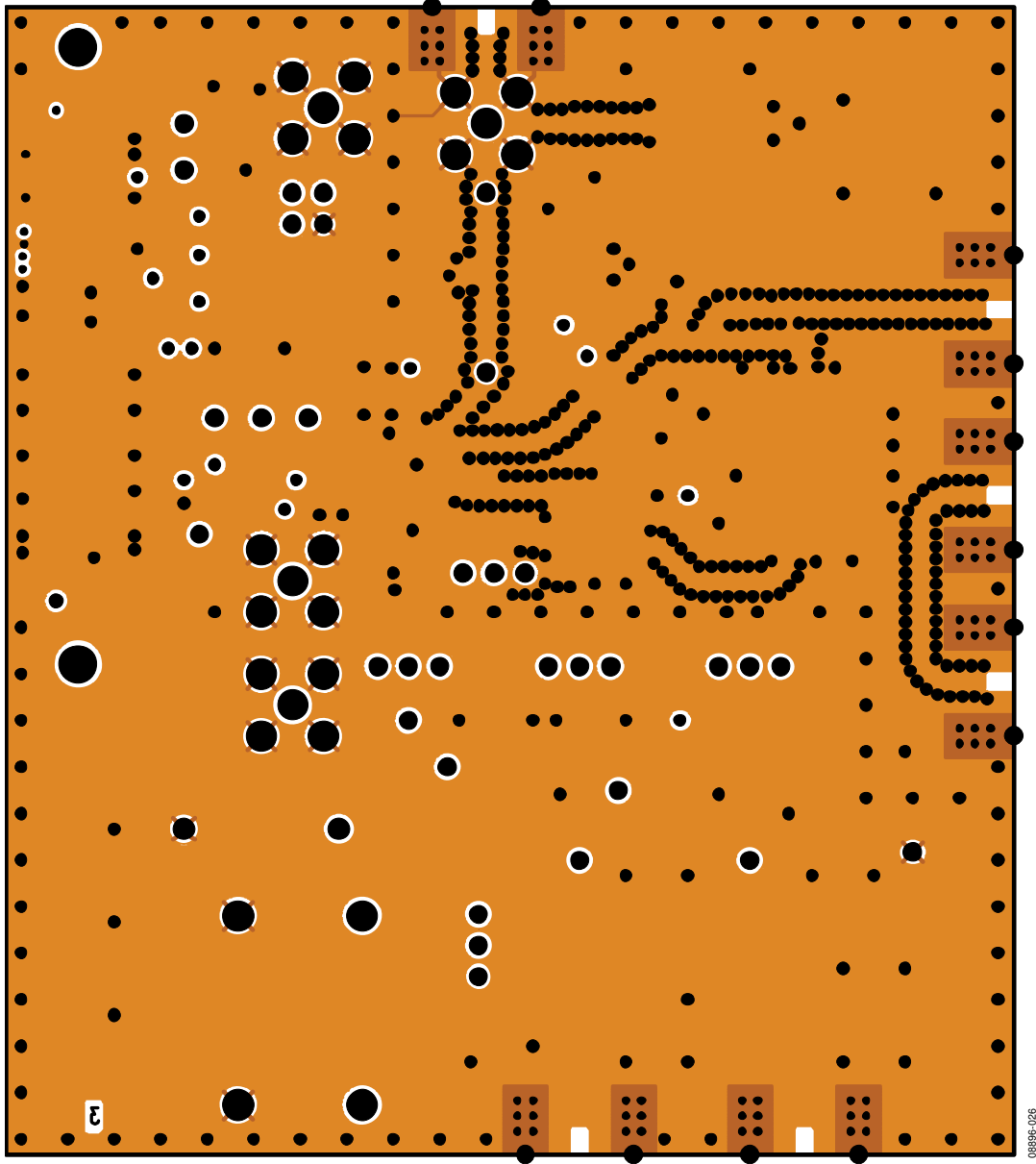


Figure 26. Layer 3 (Power Plane)

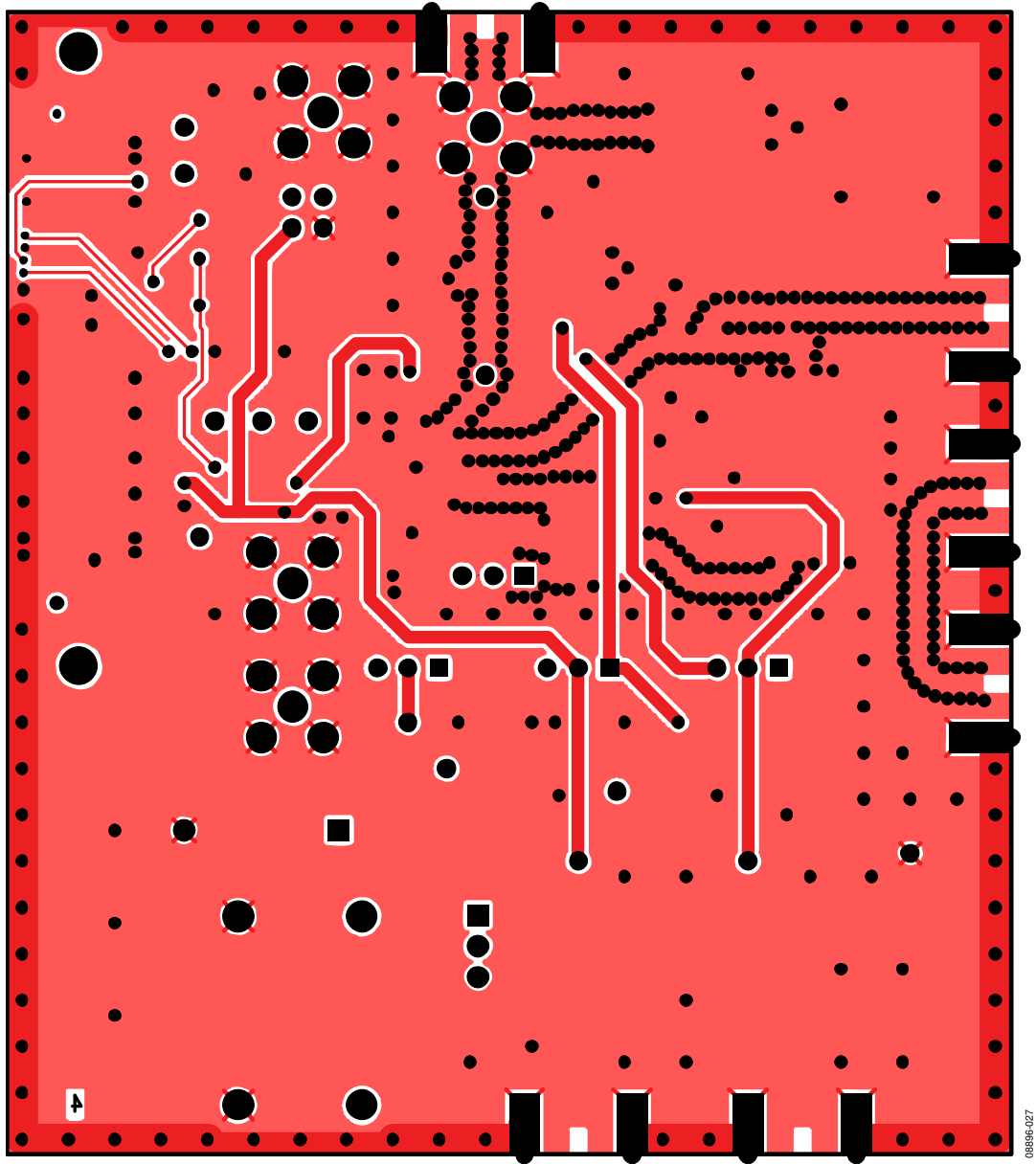


Figure 27. Layer 4 (Solder Side)

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## ORDERING INFORMATION

## BILL OF MATERIALS

Table 2.

Reference Designator	Part Description	Manufacturer/Part No.
C1, C2, C3	Capacitor, 0805	User supplied
C4, C6, C10	Capacitor, 0402, 0.1 $\mu$ F, 16 V	AVX CM105X7R104K16AT
C5, C7, C9, C11, C13	Capacitor, 0603, 10 pF, 50 V, SMD	AVX 06035A100JAT2A
C8, C12	Capacitor, Case A, 22 $\mu$ F, 6.3 V	AVX TAJA226K006R
C14, C15	Capacitor, 0603, 1 nF, 50 V	AVX 06035A102JAT2A
C16, C17, C18, C19	Capacitor, 0603, 100 pF, 50 V	AVX 06035A101JAT2A
C20, C23	Capacitor, Case A, 1 $\mu$ F, 16 V	AVX TAJA105K016R
C21, C24	Capacitor, 0603, 10 nF, 50 V	AVX 06035C103JAT2A
C22, C25	Capacitor, Case A, 4.7 $\mu$ F, 10 V	AVX TAJA475K010R
C26, C27	Capacitor, 0603, 10 nF, 50 V	Not inserted
D1	LED, green	OSRAM LGR971-Z
D2	Diode, DO41, 1 A, 50 V	Multicomp 1N4001
D3, D5	SD103C, 6.2 V	ON Semiconductor MBR0520LT1G
D4	LED, red	Avago HSMS-C170
J1	120-way connector, 0.6 mm pitch	Hirose FX8-120S-SV(21)
J2	Jack, SMA, SMA_EDGE	Johnson Components 142-0701-851
J3, J4, J10	Jack, SMA, receptacle straight PCB	Not inserted
J5, J6, J7, J8, J9	Jack, SMA, SMA_EDGE	Not inserted
J11	Jack, SMA, receptacle straight PCB	Pomona 72963
LK1, LK3, LK4, LK5	Jumper-2\SIP3, Link-3P	Harwin M20-9990345 and M7566-05
LK2	Jumper-2	Harwin M20-9990245 and M7566-05
GND	Black 4 mm banana socket	Deltron 571-0100-01
VSUPPLY	Red 4 mm banana socket	Deltron 571-0500-01
R1A	Resistor, 0805	User supplied
R1	Resistor, 0805	User supplied
R2	Resistor, 0805	User supplied
R3	Resistor, 0805, 5.1 k $\Omega$ , $\pm$ 1%, 0.1 W	Multicomp MC 0.1 0805 1% 5K1
R4, R5, R6, R23, R29, R42	Resistor, 0603, 330 $\Omega$	Multicomp MC 0.063W 0603 1% 330R
R7, R8, R9	Resistor, 0603, 18 $\Omega$	Multicomp MC 0.063W 0603 1% 18R
R10, R17	Resistor, 0603, 51 $\Omega$	Multicomp MC 0.063W 0603 1% 51R
R11	Resistor, 0603 100 $\Omega$	Multicomp MC 0.0625W 0402 1% 100R
R12, R13, R24, R25, R26	Resistor, 0603, 10 k $\Omega$	Multicomp MC 0.063W 0603 1% 10K
R14, R16, R18, R28, R36	Resistor, 0603, 0 $\Omega$	Multicomp MC 0.063W 0603 1% 0R
R15, R22, R27, R32, R33, R37, R46	Resistor, 0603, 0 $\Omega$	Not inserted
R19, R20	Resistor, 0603, 330 k $\Omega$ , $\pm$ 1%, 0.063 W	Multicomp MC 0.063W 0603 1% 330K
R21	Resistor, 0603, 4.7 k $\Omega$ , $\pm$ 1%, 0.063 W	Multicomp MC 0.063W 0603 1% 4K7
R30	Resistor, 0402	Not inserted
R31, R34	Resistor, RC31 0402 100 k $\Omega$	YAGEO (Phycomp) RC0402JR-07100KL
S1	Switch, PCB, SPDT, 20 V	APEM TL36P0050
T1 to T14	Test point, PCB, red PK_100	Vero 20-313137
U1	ADF4002, TSSOP-16	ADF4002BRUZ
U3	ADP3300, SOT23-6	ADP3300ART-5
U2	ADP3300, SOT23-6	ADP3300ART-3
U4	32k I <sup>2</sup> C serial EEPROM, MSOP8	Microchip 24LC32A-I/MS
Y1	VCO19V-XXXXT	Not inserted
Y2	Low profile/temperature compensated crystal oscillator, OSC_TCXO, 10 W	Not inserted

**RELATED LINKS**

<b>Resource</b>	<b>Description</b>
<a href="#">ADF4002</a>	Product Page, Phase Detector / PLL Frequency Synthesizer
<a href="#">ADP3300</a>	Product Page, High Accuracy anyCAP® 50 mA Low Dropout Linear Regulator

**NOTES**



**NOTES**

## NOTES

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Legal Terms and Conditions**

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.