DDC11xEVM-PDK User's Guide

Figure 1. DDC11xEVM-PDK Photo

The DDC11xEVM-PDK is an evaluation kit for evaluating the DDC112 (dual channel) and DDC114 (quad channel) current input 20-bit analog-to-digital (A/D) converters. The kit consists of a motherboard (DDCMB) for interfacing to a PC, one DDC112 device board (DDC112EVM), and one DDC114 device board (DDC114EVM). Easy-to-use software for the Microsoft Windows® operating system is included that allows performance evaluation of either device. Complete circuit descriptions, schematic diagrams, and bills of material are included in this user's guide.

The following related documents are available through the Texas Instruments web site at www.ti.com.

EVM-Compatible Device Data Sheets

Device	Literature Number	Device	Literature Number
DDC112U	SBAS085	SN74LVC07	SCES337
DDC114	SBAS255	REG113	SBVS031
OPA350	SBOS099	TPS75233	SLVS242
SN74LVC2T45	SCES516	SN105125	SLVS418
SN74LVC4245A	SCAS375	LM4040A41	SLOS456
REG104	SBVS025		

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1 Introduction

The DDC11xEVM-PDK provides an easy-to-use platform for evaluating the DDC112 or DDC114 charge-digitizing A/D converters. A PC interface board (DDCMB) and daughterboards for the DDC112 or DDC114 are included along with software that makes analysis and testing of these devices simple.

2 DDC112

The DDC112 is a dual input, precision, wide dynamic range, charge-digitizing A/D converter with 20-bit resolution. The functional block diagram is shown in Figure 2. Low-level current output devices, such as photo sensors, can be directly connected to the DDC112 input. The most stringent accuracy requirements of many unipolar output sensor applications occur at low signal levels. The DDC112 combines the functions of current-to-voltage conversion, integration, programmable full-scale, A/D conversion, and digital filtering to produce precision, wide dynamic range results. Oversampling and digital filtering reduce system noise dramatically. Correlated double sampling captures and eliminates steady state and conversion cycle-dependent offset and switching errors that conventional analog circuits do not eliminate.

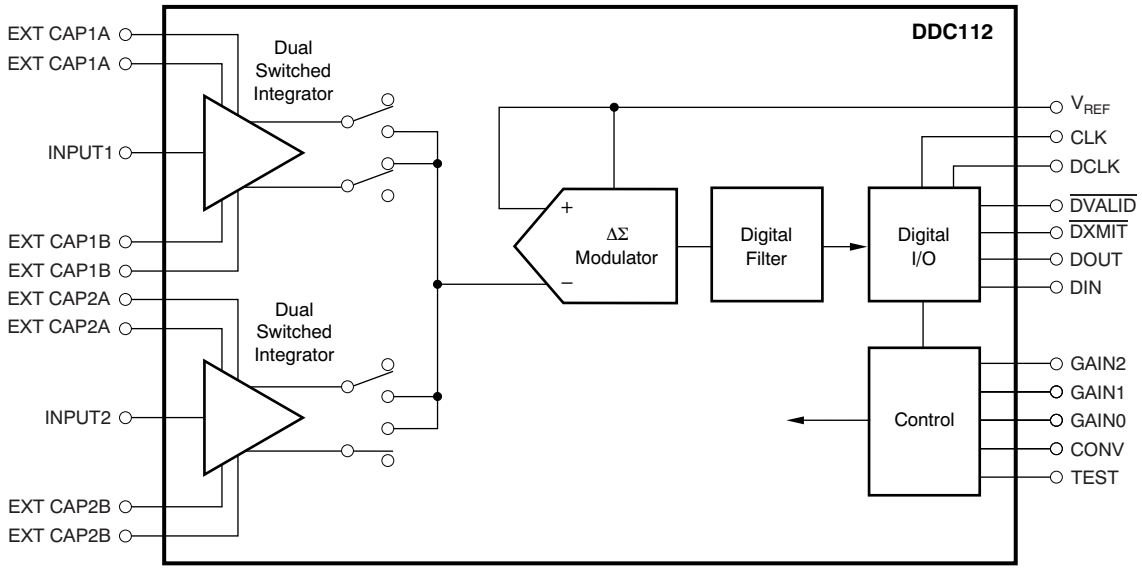


Figure 2. DDC112 Functional Block Diagram

The DDC112 continuously integrates the input signal by incorporating one dual integrator (A and B) per input channel. The output of the dual integrators are multiplexed into the A/D converter. In operation, one side of each input integrates the input charge, while the other side is being converted by the delta-sigma A/D converter and then reset. Figure 3 illustrates this operation. Another unique feature of the DDC112 is the option of external integrating capacitors. This option allows a user-programmable full-scale range. On the DDC112EVM evaluation fixture, sockets are provided on the device under test (DUT) board (P_{13} to P_{20}) to allow for easy insertion of these optional capacitors.

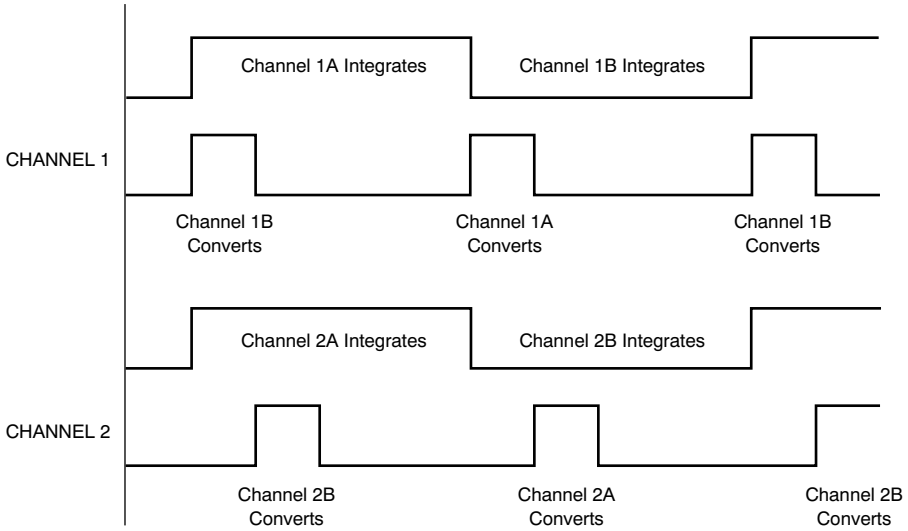


Figure 3. Integration/Conversion Timing of a Dual DDC112 A/D Converter

The gain of the DDC112 can be programmed to seven predetermined values through the software. Likewise, a user can install four external capacitors (C10, C11, C12, and C13) and design in a custom gain setting. Table 1 summarizes the available gain options.

Table 1. Input Ranges vs Gain Settings for the DDC112[(1)]

Input Range Q_{IN} Range (pC)	Integration Capacitor (Nominal) C_{INT} (pF)
–0.2 to 50	12.5 (internal)
–0.4 to 100	25.0 (internal)
–0.6 to 150	37.5 (internal)
–0.8 to 200	50.0 (internal)
–1.0 to 250	62.5 (internal)
–1.2 to 300	75.0 (internal)
–1.4 to 350	87.5 (internal)
–4.0 to 1000	250 (external)

(1) In this example, the integration time is 1 ms.

Assuming a 10MHz system clock (pin 10 of the DUT), the relationship between the integration time, input current, and input charge is summarized in Equation 1 through Equation 3.

$$T_{INT} = \frac{Q_{IN}}{I_{IN(max)}} \tag{1}$$

$$\left(\frac{T_{INT}}{C_{INT}}\right) = \left(\frac{V_{REF}}{I_{IN(max)}}\right) \tag{2}$$

$$C_{INT} = \left(\frac{Q_{IN}}{V_{REF} - 0.1V}\right) \tag{3}$$

where

- T_{INT} = integration time in ms
- Q_{IN} = input charge in coloumbs
- I_{IN} = input current in amperes

The dual switched integrators of the A/D converter use a differential input topology, with the noninverting input internally tied to VREF. This architecture allows the digitizer to operate from a single supply. Before the beginning of each integration, the integrator is reset to VREF. Additionally, the offset, offset drift, noise, and kT/C errors are corrected at that time. A low-noise voltage reference of 4.096V (nominal) provides the best performance from the DDC112. The reference that is designed for the DDC112EVM DUT board is implemented with a LM4040 (4.1V reference), a low-pass R/C filter, and a single-supply operational amplifier (U3). The operational amplifier is loaded with multiple capacitors in an effort to further reduce reference noise and ripple.

A digital filter in the DDC112 passes a low-noise, high-resolution digital output to the serial I/O register. Because the serial I/O register is independent of the DDC112 conversion process, the output of multiple DDC112 units can be connected together in series to minimize interconnections.

The DDC112 integrates on one side of the dual switched integrator while it digitizes the other side (as illustrated in Figure 3). In the event that the integration time is less than the amount of time required to digitize Channel 1 and Channel 2, the DDC112 changes to a non-continuous mode. In this mode, the integration is not continuous and the device appears to skip integrations. The limiting factor in these situations is the time required to digitize the signals (Channel 1 and Channel 2).

3 DDC112EVM Hardware Description

The DDC112EVM is a device-under-test (DUT) board that contains one DDC112 device to be tested, data buffers, 4.1V reference, decoupling capacitors, sockets for optional input circuits, sockets for optional external gain configurations, and an analog breadboard area (see Figure 25 for layout artwork and appended schematic).

The PC interface board (DDCMB) and the DUT board are separate to minimize digital noise effects on the DDC112 unit being tested, as well as to allow for other DUT boards to be used (for example, a board with multiple converters). Digital buffers are installed at both ends of the interface to improve the isolation between the boards.

The DDC112EVM DUT board is carefully laid out to ensure low-noise evaluations. Note that all the digital pins are located on one end of the DDC112U with the analog pins on the other. Be careful to keep the digital activity as far away from the analog pins as possible. In particular, pins 9 through 17 of the DDC112U have higher digital activity than the others, and should be shielded from the analog functions. The digital return lines are carefully separated on the DDC112EVM DUT board. The additional ground plane shields on the top and bottom of the DDC112EVM DUT board are installed with the board to ensure that low-noise tests are possible. During operation, the lid of the DDC112EVM DUT board should be closed.

Proper grounding and shielding practices should be taken into consideration when designing the circuit layout for the DDC112. In the event that the application cannot tolerate the additional shields of the DDC112EVM DUT board, an alternative layout is shown in Figure 4, where a PC ground plane is placed around the inputs of the DDC112 (pins 1 and 28). This shield helps minimize coupled noise into the input pins. Additionally, the pins that are used for the external integration capacitors (pins 3, 4, 5, 6, 23, 24, 25, and 26) should be guarded by a ground plane when the external capacitors are used.

The digital and analog planes are not separate on this demonstration fixture because of the low level of digital activity on the board. Regardless of the power-supply strategy, the bypass capacitors should be as close to the device as possible.

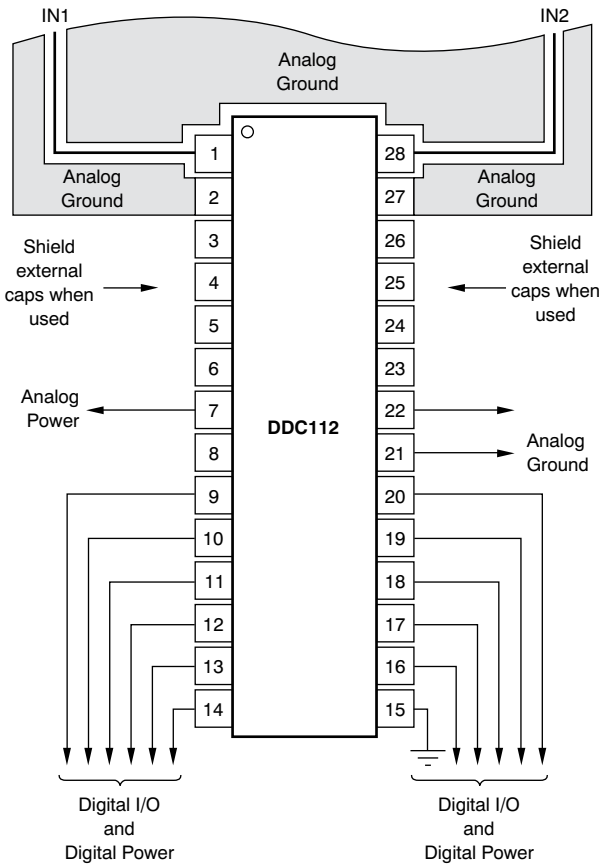


Figure 4. Recommended Shield for DDC112 Layout Design

3.1 Reference Circuit

The 4.096V reference that has been installed on the DDC112EVM DUT board has been carefully selected because of its low-noise performance. The LM4040-4.1 provides a 4.096V (nominal) reference. At the reference output, a single pole (3.157Hz) low-pass filter is inserted in the reference signal path. This filter is then followed by an amplifier configured as a buffer. The output of the amplifier has been loaded with 20.1μF of capacitance. This value of capacitance was derived through experimentation. The voltage reference circuit described above has been found to enable the DDC112U to perform optimally.

To evaluate alternative reference circuits, use jumper JP1 to connect an external reference source through the BNC connector, J5, or a user-designed reference circuit from the breadboard. Table 2 shows the jumper settings for JP1.

Table 2. Jumper Setting Definitions for JP1 for the Voltage Reference Source for the DDC112

Jumper Setting	Jumper Setting Function
Position A	Connects the 4.096V onboard reference to the DUT.
Position B	Connects the EXT VREF connector, J5, to the DUT.
Position C	Connects the breadboard VREF bus to the DUT.

3.2 Optional Component Sockets

Resistor and capacitor socket locations are included on the DDC112EVM DUT board to allow for optional input circuits and easy insertion of the optional external gain capacitors.

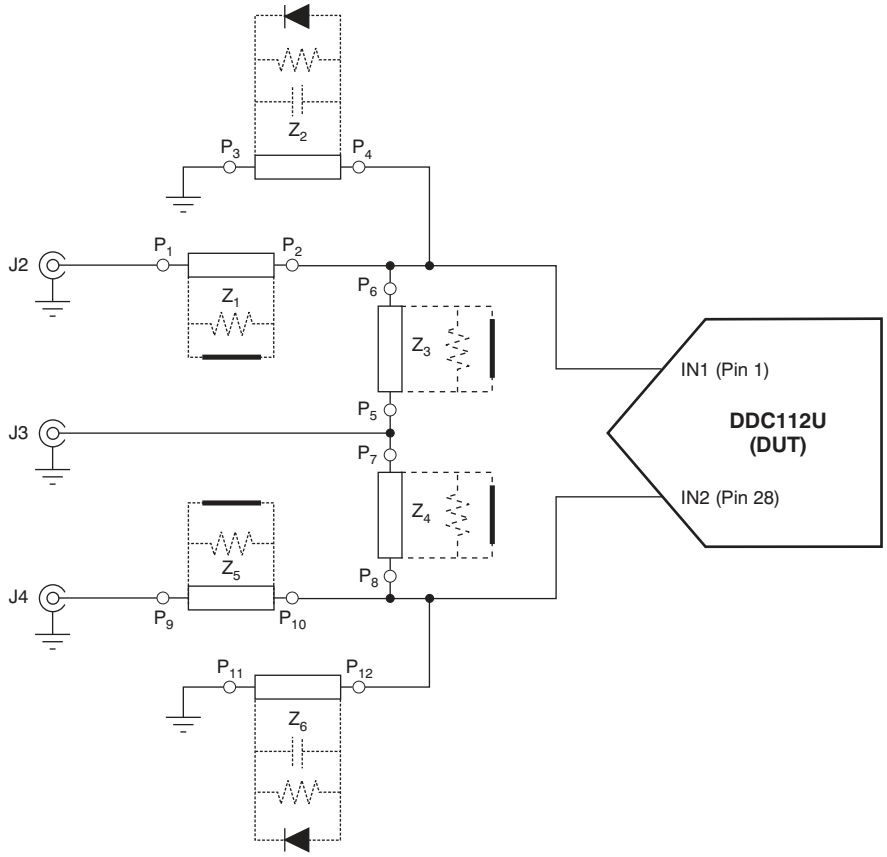


Figure 5. Input Structure on the DDC112EVM DUT Board

Figure 5 shows the topology of the input socket options and BNC connectors. For this input structure to work as shown, jumpers JP2 and JP3 must be removed from the DDC112 DUT board so that R6 and R7 have no effect at the input. To simplify the diagram JP2, JP3, R6, and R7 are not shown. Using this arrangement, several different input configurations can be implemented on the DDC112 DUT board. For example, a photosensor can be installed for the IN1 (pin 1 of the DUT) using the P_3 and P_4 sockets. Alternatively, a voltage source could be used to excite the input of the converter by using J2 with a resistor installed in the Z_1 position (P_1 and P_2) sockets. Both of these configurations can be implemented on the IN2 (pin 28) input as well. A dc offset current can be injected into the input through J3. A resistor in the Z_3 position should be inserted if the source from J3 is voltage. A short should be inserted if the source is a current. It can be quickly seen that a variety of configurations can be implemented with this input circuitry configuration. The factory setting for this circuit is all input sockets open. The default inputs to the DDC112 connect to R6 and R7, which are 10MΩ resistors. The input to the resistors can be selected using the jumpers JP2 and JP3. JP2 is used as an input selection for IN1 of the DDC112, and can be selected to receive an input from J2 or J3. JP3 is used to select the input for IN2 of the DDC112 and can receive an input from J3 or J4. The factory default setting for JP2 and JP3 is J3 (INPUT CM).

External capacitors can be inserted in the C10, C11, C12, and C13 positions, as shown in Figure 6. These external capacitors can be used to set the gain of the DDC112U (DUT) to user specifications instead of the seven internal gains available. Refer to the DDC112 portion of this user guide for more details concerning the appropriate value of these external capacitors. For further detailed information, also refer to the DDC112 product data sheet. For best performance, the leads of the capacitors should be as short as possible on C10 to C11 and C12 to C13.

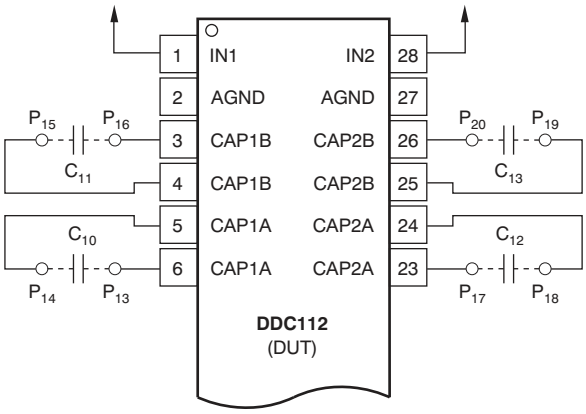


Figure 6. External Gain Capacitor Socket Configuration for the DUT Board

4 DDC114

The DDC114 is a 20-bit, quad channel, current-input A/D converter (as shown in Figure 7). It combines both current-to-voltage and A/D conversion so that four low-level current output devices, such as photodiodes, can be directly connected to its inputs and digitized.

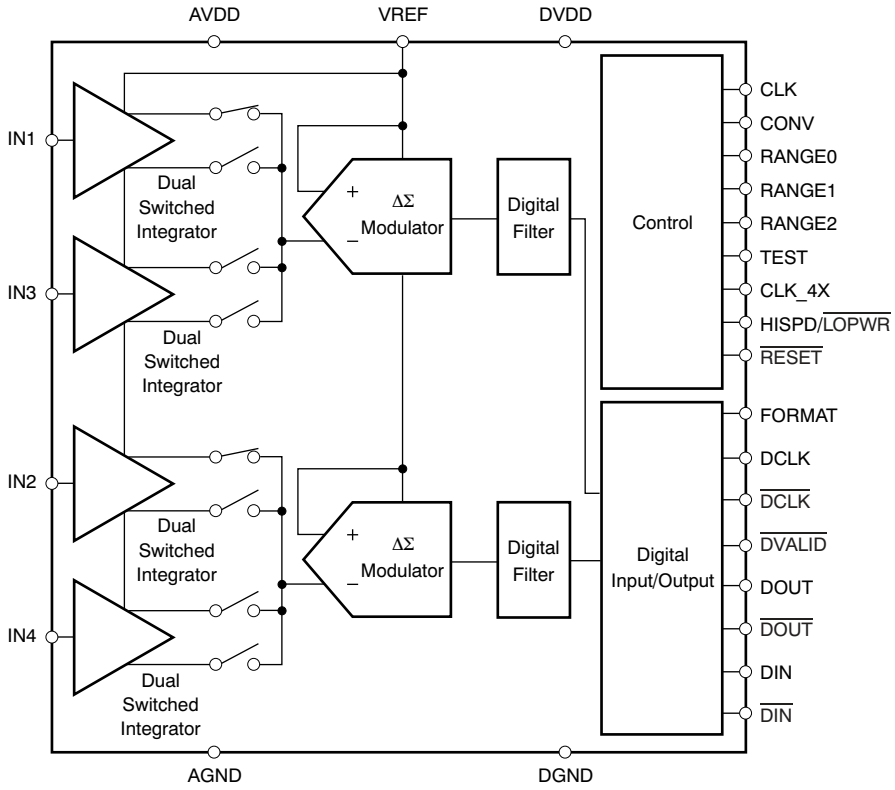


Figure 7. DDC114 Block Diagram

For each of the four inputs, the DDC114 provides a dual-switched integrator front-end. This design allows for continuous current integration: while one integrator is being digitized by the onboard A/D converter, the other is integrating the input current. Adjustable full-scale ranges from 12pC to 350pC and adjustable integration times from 50μs to 1s allow currents from fAs to μAs to be measured with outstanding precision. Low-level linearity is ±0.5ppm of the full-scale range and noise is 5.2ppm of the full-scale range.

In many ways, the DDC114 can be viewed as a dual DDC112; the difference between the devices is that the DDC112 offers the option of using external integrating capacitors, giving it the possibility for extended input ranges.

There are eight different capacitors available on-chip for both sides of every channel in the DDC114. These internal capacitors are trimmed in production to achieve the specified performance for range error of the DDC114. The range control pins (RANGE0–RANGE2) change the capacitor value for all four integrators. Consequently, all inputs and both sides of each input have the same full-scale range. Table 3 shows the capacitor value selected for each range selection.

Table 3. Range Selection of the DDC114

RANGE2	RANGE1	RANGE0	C_F (pF, typ)	Input Range (pC, typ)
0	0	0	3	–0.048 to 12
0	0	1	12.5	–0.2 to 50
0	1	0	25	–0.4 to 100
0	1	1	37.5	–0.6 to 150
1	0	0	50	–0.8 to 200
1	0	1	62.5	–0.1 to 250
1	1	0	75	–1.2 to 300
1	1	1	87.5	–1.4 to 350

5 DDC114EVM Hardware Description

The DDC114EVM is a device-under-test (DUT) board with a DDC114 device, data buffers, and a 4.1V reference (see Figure 28 for layout artwork and appended schematic). The interface and the appropriate circuit options for this device are similar to those available on the DUT board for the DDC112.

Three power-supply connections are provided on this DUT board: 5V, DVDD, and AVDD. The 5V supply is regulated on the DUT board to provide a 3.3V supply for the interface buffers. DVDD is the digital supply for the DDC114 and can range from 2.7V to 5.5V; AVDD is the analog supply to the DDC114 and must be between 4.75V and 5.25V. Jumpers JP1 and JP2 allow the board 5V and AVDD supplies to be tied to DVDD, if a single 5V supply is used. Table 4 summarizes the powering options of this board.

Table 4. Power Option Jumpers for DDC114 DUT Board

Jumper	Description
JP1	When installed, 5V is connected to DVDD (J3). When not installed, 5V must be supplied through J2.
JP2	When installed, AVDD is connected to DVDD (J3). When not installed, AVDD must be supplied through J4.

The inputs to the DDC114 device can be provided individually on the J6–J9 (AIN1 to AIN4) BNC connectors. For testing purposes, all four channels can be driven with the same signal if it is provided on J5 (AINCOM). Each of the four input channels connect to a jumper (JP4–JP7) for selecting whether the input is common (AINCOM), or if each input is individually connected through the BNC connectors (J6–J9). Each jumper is connected to a 10MΩ resistor (R16–R19), which in turn goes to one of the input channels (AIN1–AIN4). The default configuration is to have each jumper connect to J5 (AINCOM) so that one signal feeds all four channels through an individual 10MΩresistor per channel. Pin socket locations are also provided at each BNC connector to allow a resistor or jumper to connect the BNC to the actual input channel. Refer to the appended schematic for details. The factory setting is all pin sockets open.

6 DDCMB Hardware Description

The PC interface board, or motherboard, is called the DDCMB. This board has a USB interface for connecting to a PC; the USB interfaces to a small microcontroller that controls the functions of a Xilinx Spartan™-3 FPGA. The FPGA generates all the timing signals that are sent to the DUT and handles communication of data between the DUT and the PC.

The DDCMB is designed to be extremely flexible and therefore has many configurable settings. These settings are described in the following subsections. When using the board with this evaluation kit, the default settings should be used. Refer to the appended schematic and the layout diagram in Figure 31.

6.1 Motherboard Connectors

The USB interface to a personal computer is provided on J1. The connection to a DUT daughtercard is made using the J4 50-pin socket.

One connector is only provided for use in manufacturing the DDCMB. J2 is a JTAG header used for the configuration of the FPGA and downloading firmware to the EEPROM.

Power is supplied to the DDCMB in one of several ways. One way is directly through the screw terminal block J3. This input should be +5VDC. Another way is through connector J5. This connector accepts a 6V–9V DC voltage from an ac/dc wall adapter supply. AC adapters must be tip-positive/sleeve-negative, with an inner size of 2.5mm and outer size of 5.5mm. A third option is to power the board using the voltage supplied from the USB connection. Jumper JP3 allows selection of the USB supply or one of the two external supply options. The factory default settings for JP3 is the USB connection.

6.2 Motherboard Jumpers

Refer to Figure 31 for location of jumpers on the DDCMB.

6.2.1 Clock Options

Two clocks are used on the DDCMB: a clock for the USB microcontroller, and a clock for the FPGA. The FPGA generates all clocking signals for the DUT daughtercards. The USB microprocessor uses a 24MHz crystal (X1), while the FPGA (U7) uses an 80MHz crystal oscillator (U8).

6.2.2 Power Supplies

JP1 provides 3.3V while JP2 provides 5V to the daughtercard via the 50-pin connector; if these options are used, assure that the daughtercard is not also supplying 3.3V or 5V locally. The factory default setting for JP1 and JP2 is installed.

6.3 Motherboard Switches

S1, RESET_USB, resets the USB controller. Pushing this switch may be necessary if the DDCMB is not recognized by your PC when connecting it to the DDCMB.

S2, RESET_FPGA, resets the FPGA. Normally, it should not be necessary to use this switch.

6.4 Hardware LEDs on the Motherboard

A number of LED indicators are on the DDCMB. These indicators allow ease of monitoring the state the motherboard is in. Refer to Table 5 for a summary of these indicators.

Table 5. DDCMB LED Indicator Functions

LED	Function Indicator
D1	USB bus power detected.
D6	FPGA configuration is done.
D5	The motherboard is powered on with 5V available.
D7	3.3V power to motherboard available.
D8	2.5V power to motherboard available.
D9	1.2V power to motherboard available.
D3	3.3V motherboard to daughterboard power is connected.
D4	5V motherboard to daughterboard power is connected

7 DDC11xEVM-PDK Kit Operation

This section provides information on using the DDC11xEVM-PDK, including setup, program installation, and program usage.

7.1 Minimum Requirements

Before installing the software please verify that the PC meets the following minimum requirements:

- Microsoft ® Windows XP® operating system with Service Pack 2 (SP2) installed
- 1024 x 768 screen resolution
- USB 2.0 compatible port

Other configurations may work; however, they are not tested. Users should be advised that when capturing larger data sets, PCs equipped with the faster processors and ample memory tend to perform best.

7.2 Installing the Software

Application software can be downloaded from the DDC11xEVM-PDK product folder. Unzip the downloaded file into a known location.

Before installing the DDC11xEVM-PDK application software, the USB drivers must be installed. This step is best accomplished by letting Windows find the drivers when the hardware connects. The drivers are located in the driver directory. To begin, connect a power supply to the DDCMB. If the wizard has trouble finding the driver files, point to the location where the application software was unzipped. Connect a USB cable from the computer to the DDCMB through J1.

Use the Windows *Found New Hardware* Wizard to install the drivers. The DDCMB requires a boot driver and an application driver; therefore, new setups require going through the Found New Hardware Wizard twice. Figure 8 through Figure 13 show the first driver screens that appear.

Figure 8. Initial Found New Hardware Wizard Screen

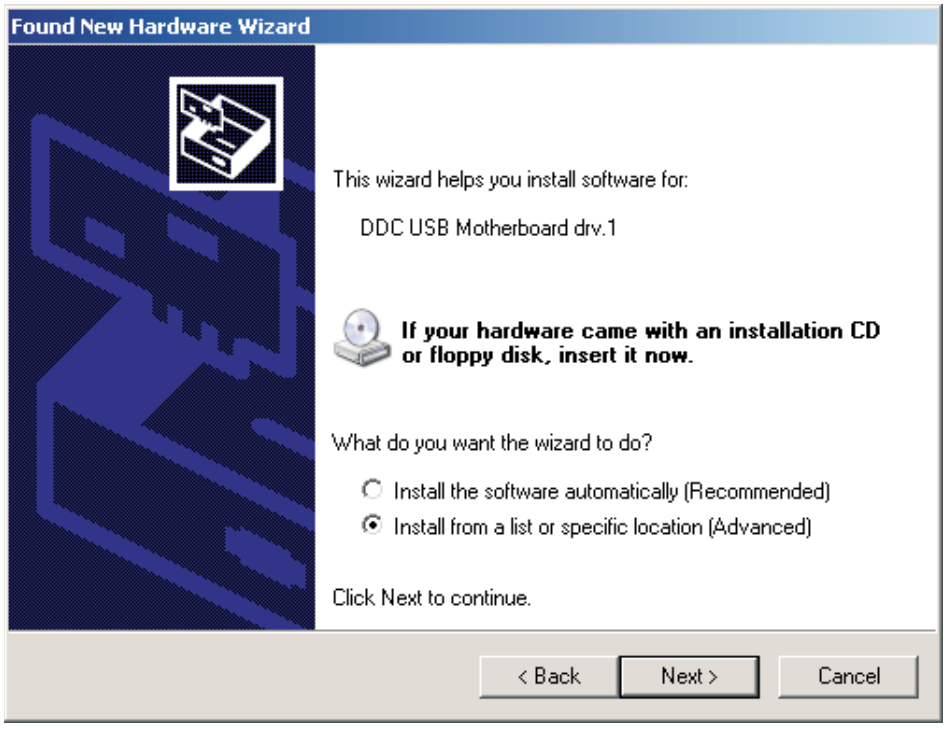


Figure 9. Driver Selection for DDC USB Motherboard drv.1

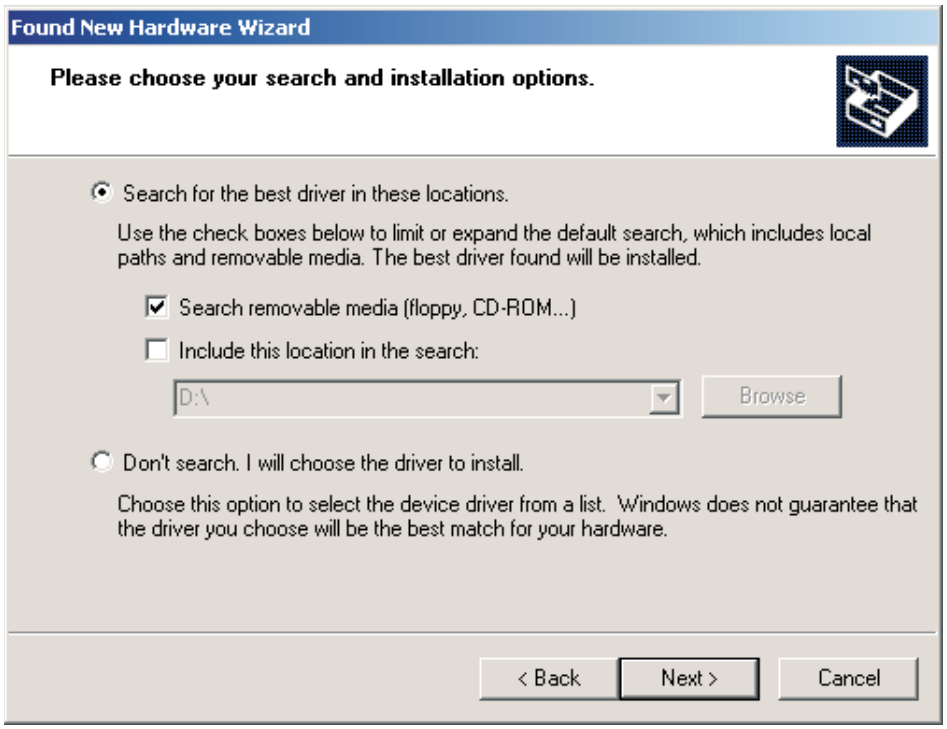


Figure 10. Select to Search Removable Media to Find Drivers on CD

NOTE: You may see notices (Figure 11) that the drivers are not digitally signed, and given the option to accept the drivers anyway. Choose *Continue Anyway*.

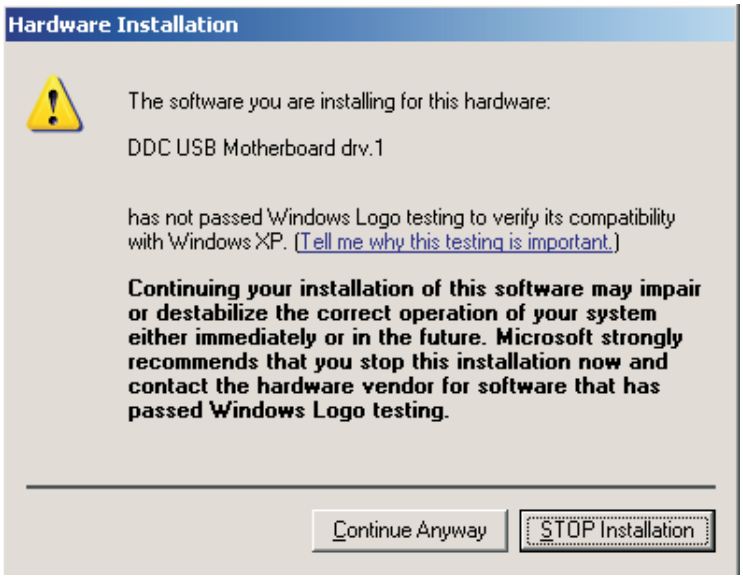


Figure 11. Driver Not Signed Notification—Choose Continue Anyway

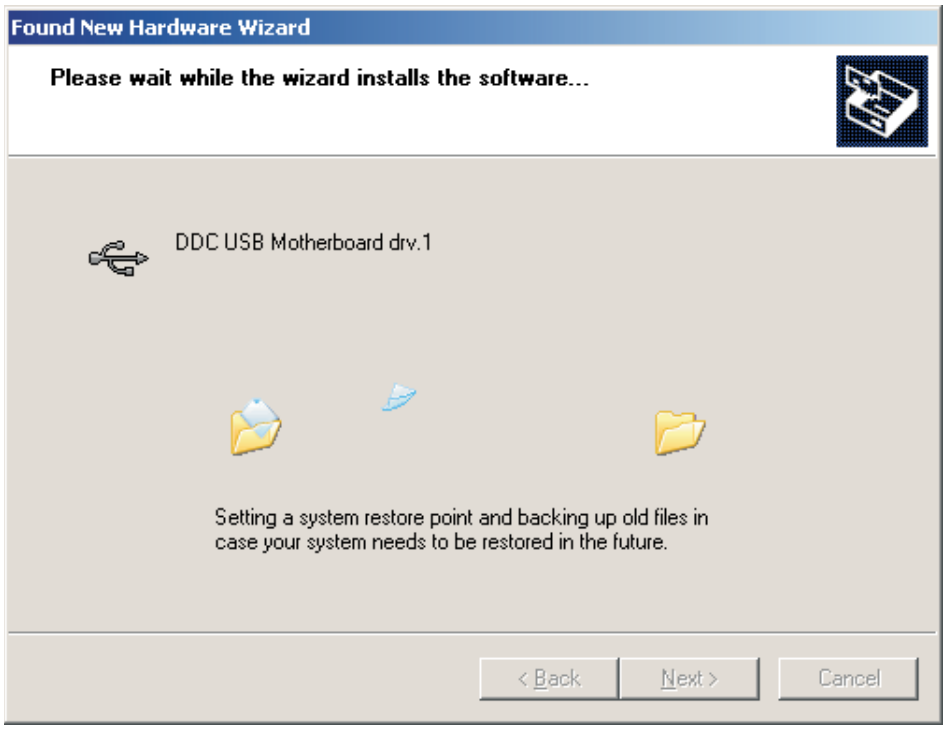


Figure 12. Copying Driver Files

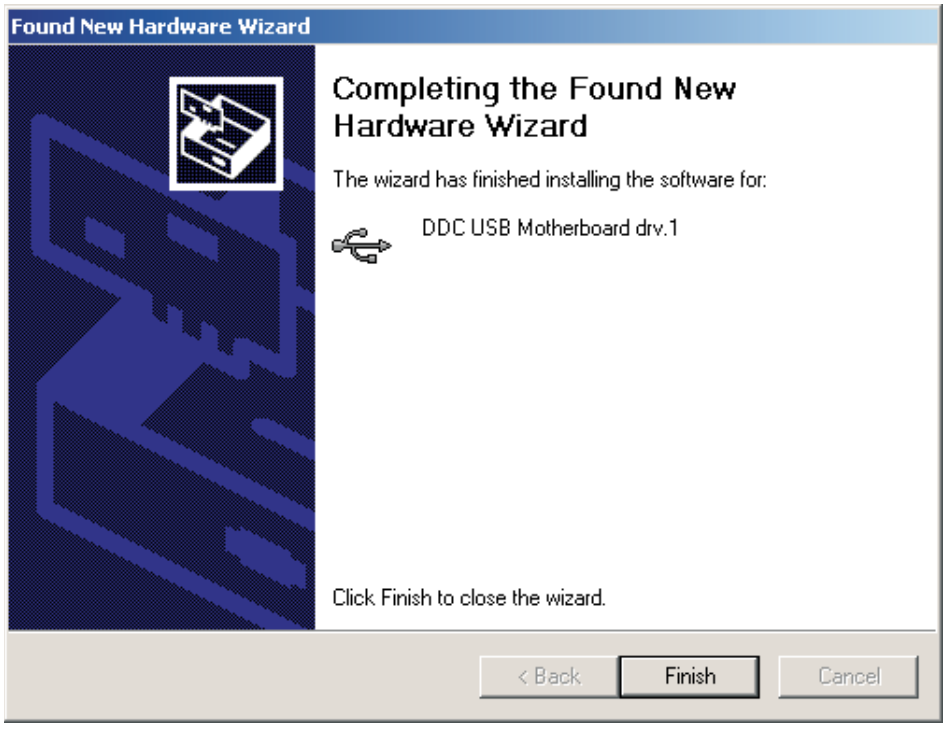


Figure 13. First Driver Installation Complete

After the first driver is installed, disconnect and reconnect the USB cable to the DDCMB, or press the RESET_USB button on the DDCMB. This step causes the second driver to be installed. You will then see screens similar to those in Figure 14 through Figure 16.

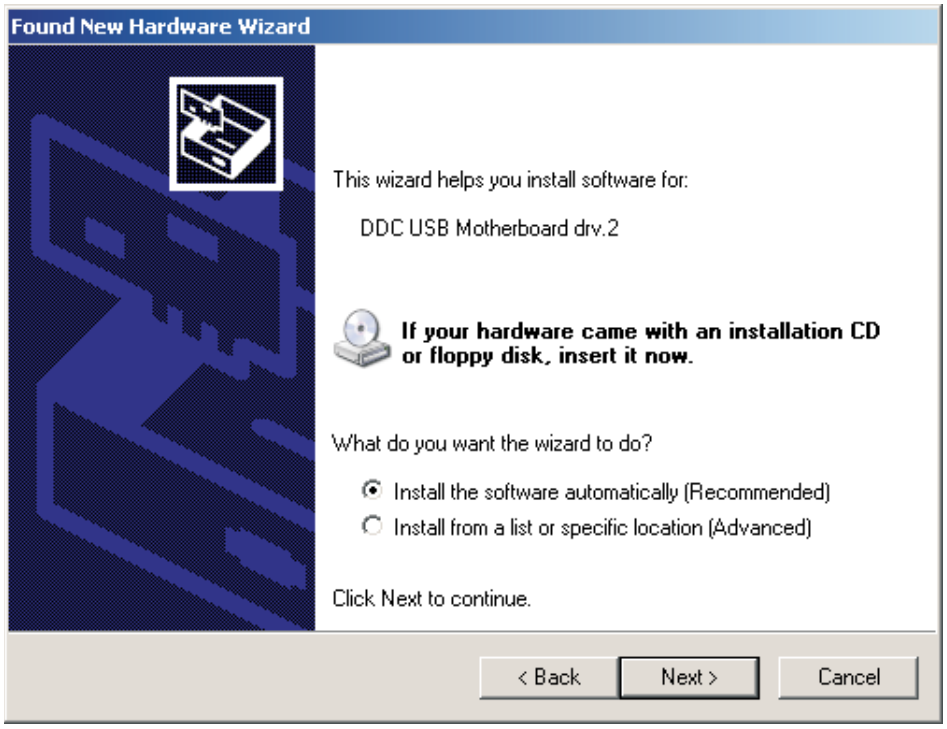


Figure 14. Driver Selection for DDC USB Motherboard drv.2

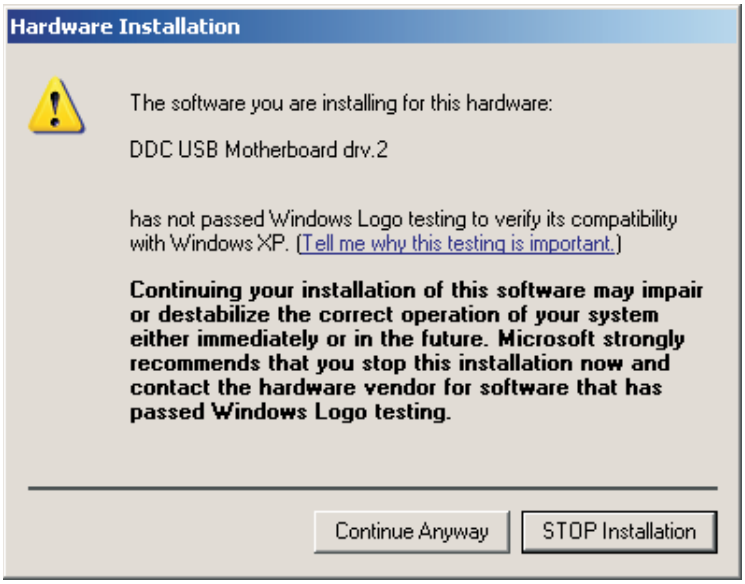


Figure 15. Second Driver Not Signed Notification—Choose Continue Anyway

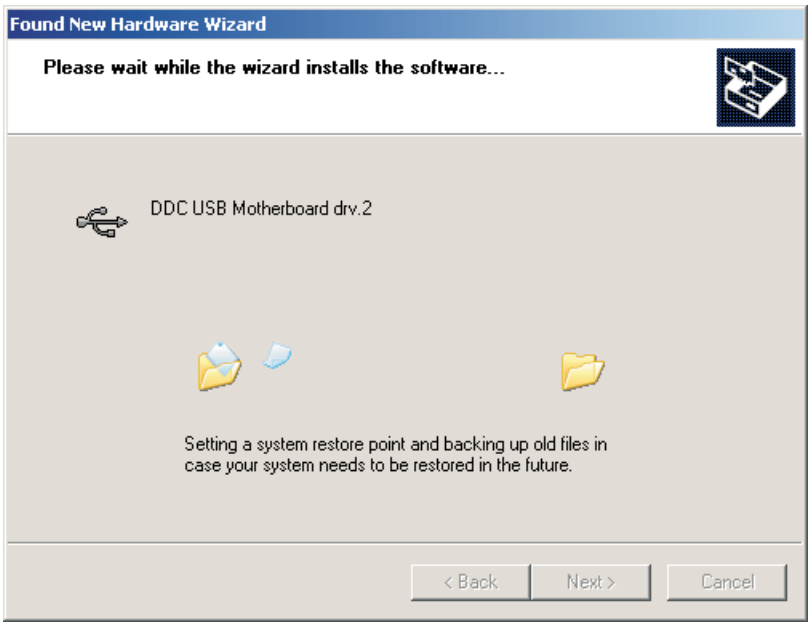


Figure 16. Copying Files for Additional Driver

Once the USB drivers are installed, the DDC11x Evaluation program can be installed. Double-click on setup.exe in the install directory. A screen similar to that shown in Figure 17 appears.

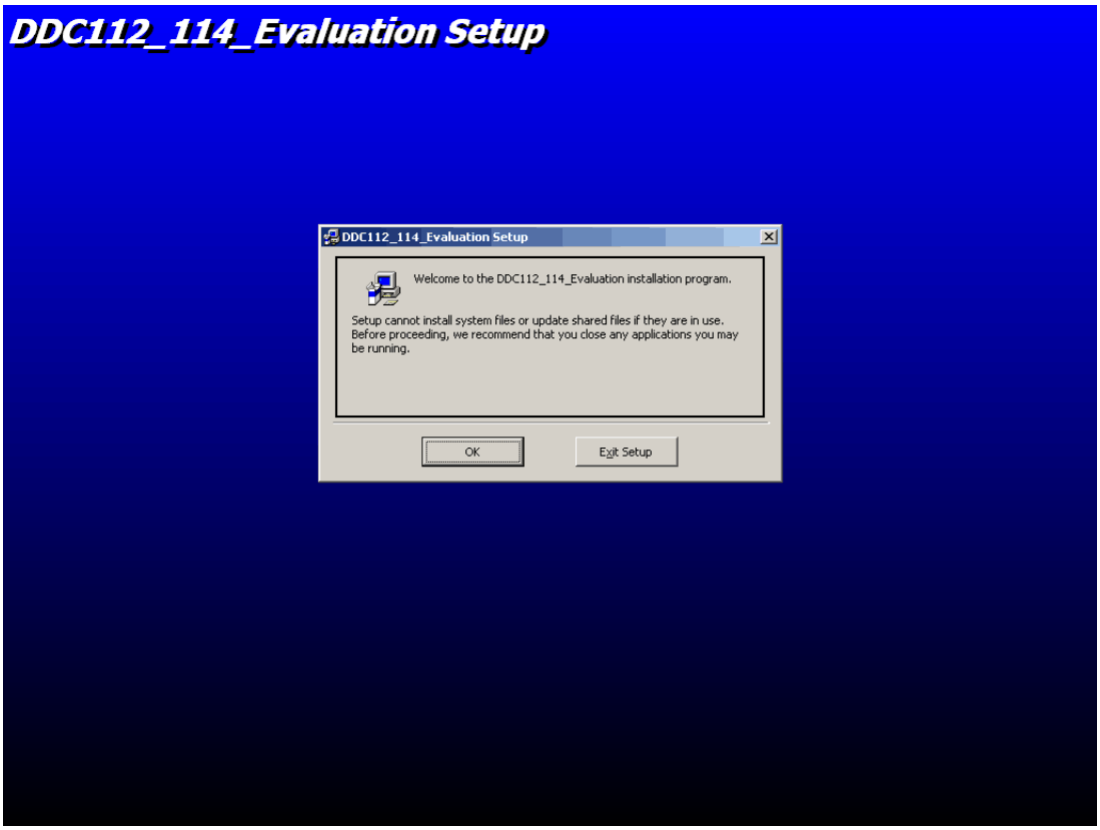


Figure 17. Initial Software Installer Screen

Next, the screen shown in Figure 18 appears. Verify that the installation directory is correct, and press the large button in the upper left corner of this screen to proceed.

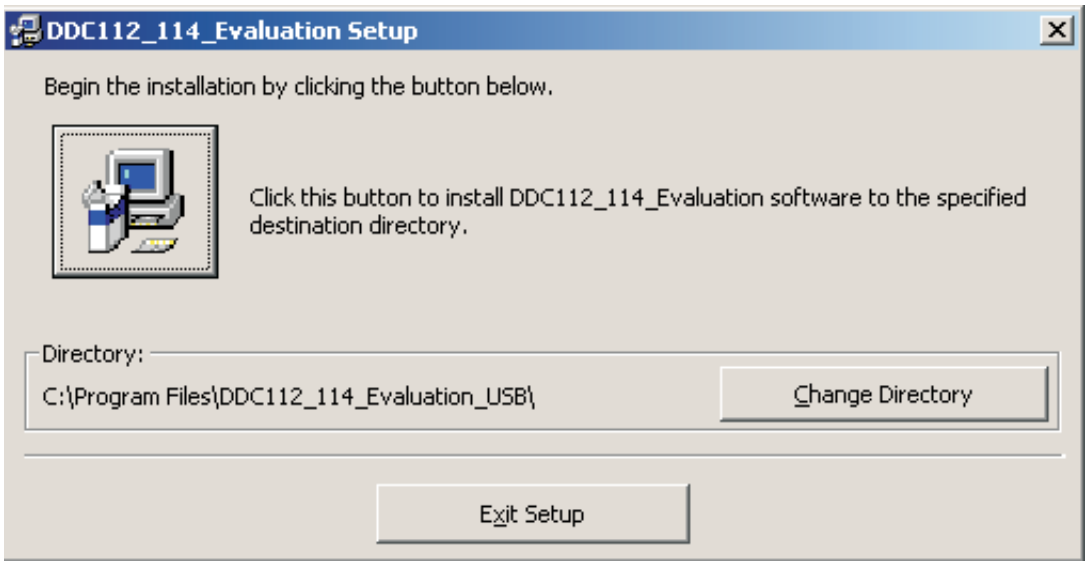


Figure 18. Choose Software Installation Directory

When the installer completes copying files, the screen shown in Figure 19 appears.

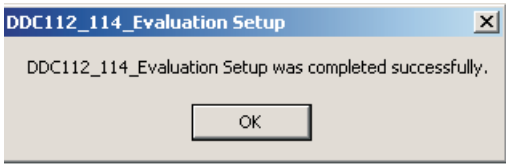


Figure 19. Software Installation Complete

The software installation is now complete. Disconnect power from the DDCMB and proceed to the next section.

7.3 Evaluating a DDC11x Device: Quick Start

With power disconnected to the DDCMB, connect one of the daughtercards to the motherboard by directly connecting the 50-pin header of the daughtercard to the 50-pin socket of the DDCMB.

Connect the power supply to the DDCMB (if not connected). To power the daughtercards from the DDCMB, attach jumpers JP1 and JP2 for the DDC112EVM, and JP2 only for the DDC114EVM. If using the DDC112EVM, attach jumpers JP1 and JP2 on the DDCMB to supply power to the DDC112EVM. When not powering the daughtercards from the DDCMB, remove JP1 and JP2 from the DDCMB. The DDC112EVM requires both 3.3V (J7) and 5V (J6) while the DDC114EVM requires 5V only at J2, assuming JP1 and JP2 of the DDC114EVM are connected. Turn on the power supply.

From the Windows **Start** menu, select the *DDC112_114_Evaluation* program. The program starts and displays a window as shown in Figure 20.

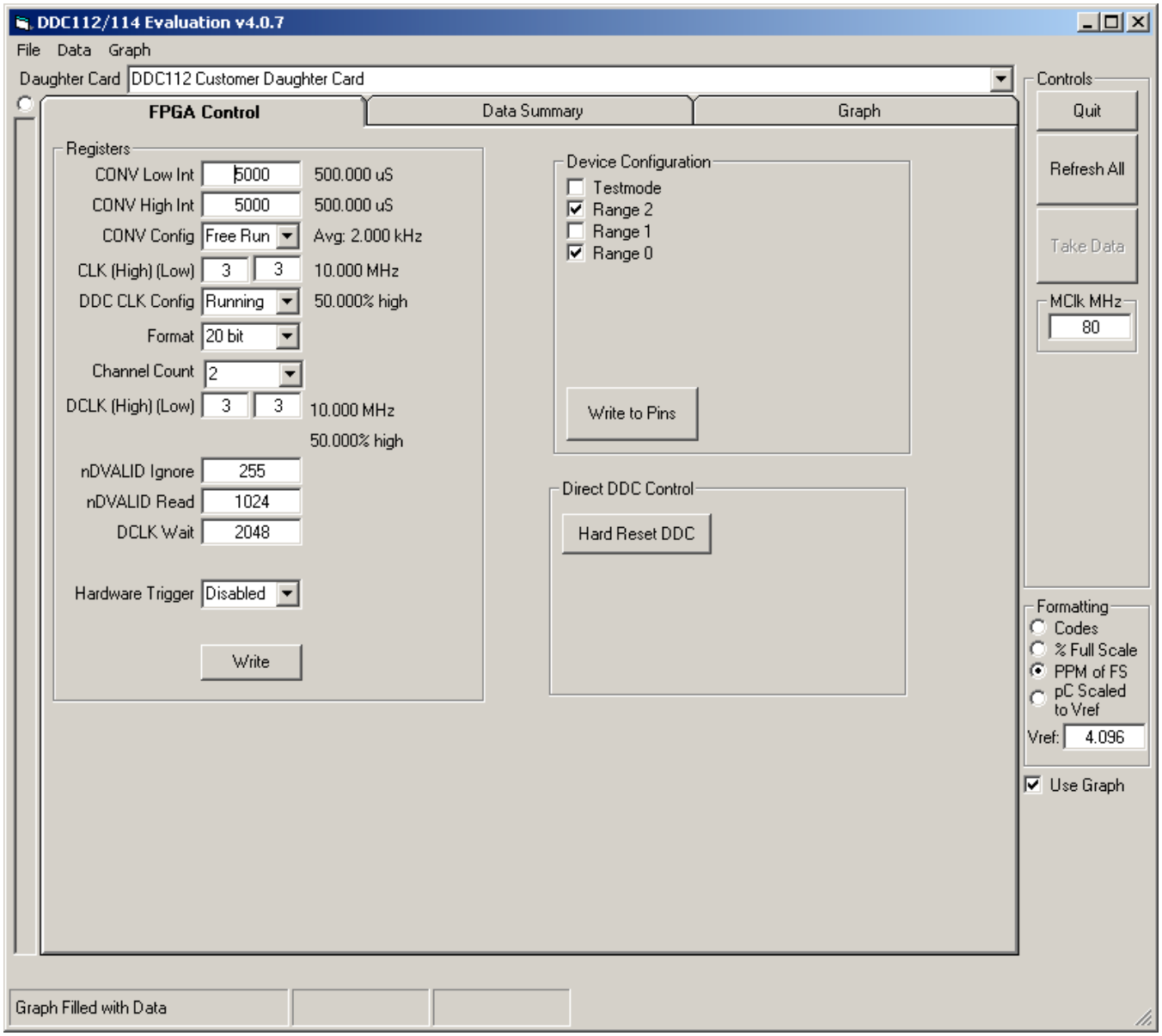


Figure 20. Initial Software Screen, FPGA Control Tab

From the **Daughtercard** drop-down menu at the top of this screen (Figure 21), select the daughtercard that is attached to the DDCMB. The settings shown on the **FPGA Control** tab are populated with the appropriate settings for the device connected.

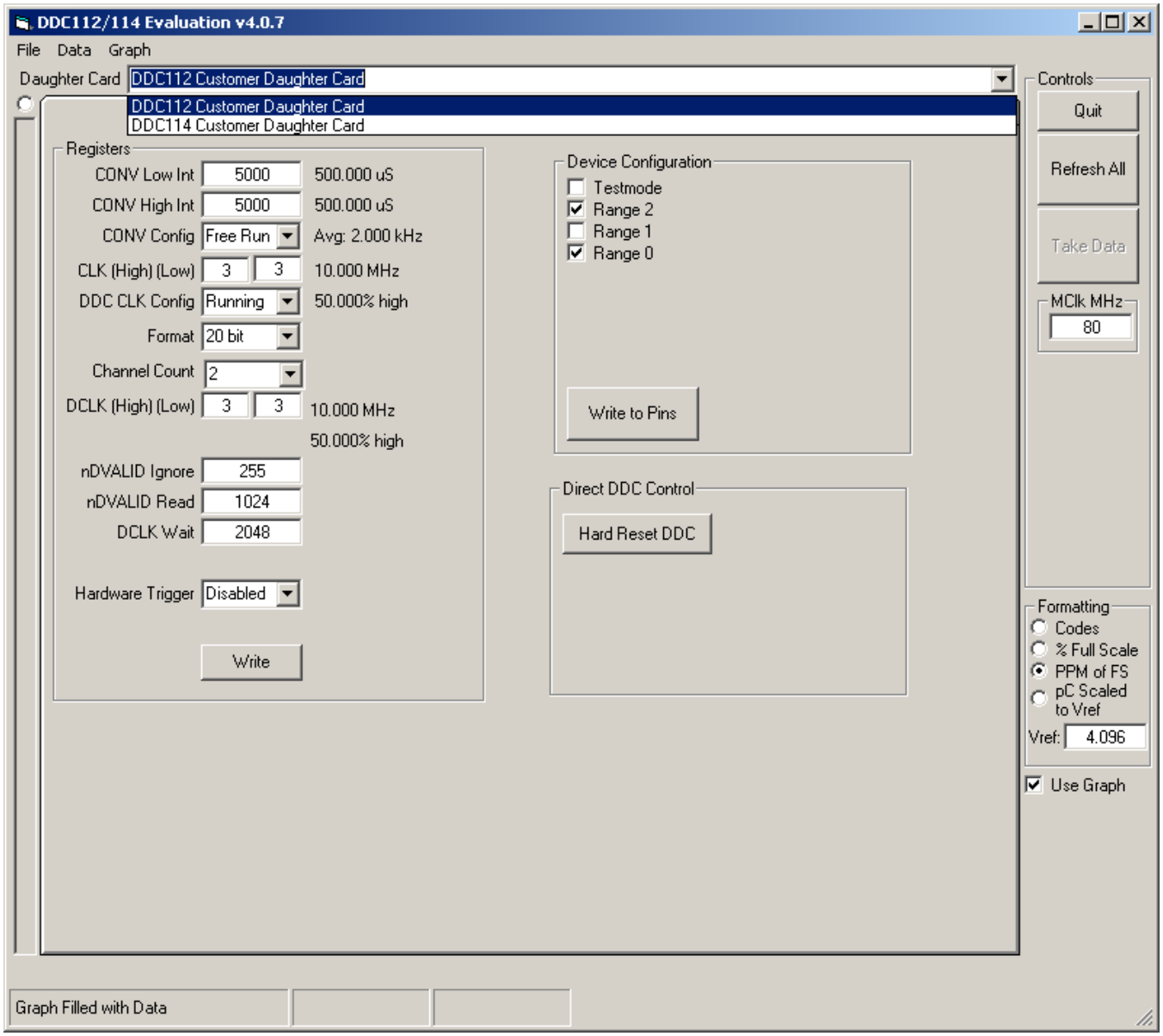


Figure 21. Daughtercard Selection

Next, do a system refresh of the FPGA by clicking on the **Refresh All** button, located in the upper right corner of this screen. This refresh initializes the system to working defaults, and verifies communication with the FPGA. When communication is established, the **Take Data** button is enabled. The software is now ready to receive data from the DDC.

7.3.1 Main Window Controls

A number of controls are always visible, regardless of the tab selected in the main tab control.

The **Quit** button causes the program to exit and releases system resources. The **Refresh All** button updates the state of all FPGA registers and pins to those states set in the FPGA control tab. The **Take Data** button causes an acquisition cycle to occur and loads data into the program memory and will update the graph with the data if the **Use Graph** check box is checked.

Data can be displayed in a number of formats, selected with the **Formatting** controls. The options are:

- *Codes*: data are displayed in raw codes or counts
- *% Full Scale*: data are displayed as a percentage of the full scale range
- *PPM of FS*: data are displayed in units of parts per million (PPM) of the full scale range
- *pC Scaled to Vref*: data are displayed in picocoulombs

The reference voltage can be set in the **Vref** text box control. The default value is 4.096V, which corresponds to the reference voltage provided by the onboard voltage references on the DDC daughtercards, but may be adjusted if a different reference voltage is used.

7.3.2 Main Window Menus

The Main window has three menus: **File**, **Data**, and **Graph**. This section describes the functions of each menu item.

File→ *Quit*

This option releases the USB port, closes all windows, and exits the software.

Data →*Save Data from Memory*

Collected data can be saved to a standard comma-separated value (CSV) formatted spreadsheet file. No header data are written to the file; only raw data. The columns are written in this order: Channel Name, Reading #, Reading [codes], Range [0-7], Vref [V], # of Bits [16 or 20].

Once a reading is made, the data can be saved to a file using the *Save Data from Memory* menu item. The data can then be analyzed further in Microsoft Excel® or a similar spreadsheet application that can parse data in user-defined CSV format.

Graph →*Plot Data on Graph*

If data are loaded into memory but not plotted on the graph (because the **Use Graph** check box is not checked), selecting this menu item plots that data on the graph.

7.3.3 FPGA Control Tab

The controls on this tab directly affect the operating mode of the DDC device being tested. This section explains the various fields and buttons that reside on this tab.

7.3.3.1 Registers Group Box

The fields in this box hold all the data that are used by the FPGA to generate the waveforms for the device under test and retrieve data. The following list summarizes of all the fields and the respective functions. Refer to the individual DDC device data sheets for further information on valid clock times and pin functions.

- **CONV Low Int**: This is the number of DDC System Clock Cycles for the CONV signal to remain low during integration. The actual time is listed next to the text box.
- **CONV High Int**: This is the number of DDC System Clock Cycles for the CONV signal to remain high during integration. The actual time is listed next to the text box.
- **CONV CONFIG**: The default value of this control is *Free Run*, and should be used in the data acquisition process. The other options should not be used.
- **CLK (High) (Low)**: This sets the high and low times of the DDC clock. The default value is 3 in both fields, representing the number of clock cycles that CLK will be high and low.
- **DDC CLK CONFIG**: Choose *Running* to enable the DDC clock or *Low* to disable the DDC clock.

- **FORMAT**: Choose how many bits wide the output word is on the DOUT line (16- or 20-bit). This option does not correspond to the FORMAT pin on the DDC114. It only controls the FPGA, and should be left at 20 bits for the DDC112 for proper operation.
- **Channel Count**: Number of channels to read back. Only the *2* or *4* settings are valid for the DDC112 or DDC114.
- **DCLK (High) (Low)**: The number of master clock cycles for DCLK to remain low and high during data readback. DCLK can be faster than the DDC System Clock, which is why DCLK is separate and may be much smaller than CLK Count.
- **nDVALID Ignore**: This is the number of nDVALID pulses to ignore, or rather the number of samples to initially discard from the device. Setting this number higher can help negate the effects of settling and give cleaner data from a dead conversion stop.
- **nDVALID Read**: This is the number of nDVALID pulses after which to capture data. The device has two sides to each integrator, so if there is a 4-channel device, 256 nDVALID Reads equate to 128 samples on four channels of both A and B sides.
- **DCLK Wait**: This is the number of master clock cycles to wait after detecting an nDVALID signal. Once a signal is detected, the data are ready; in some applications, however, a delay is helpful in achieving desired results.
- **HARDWARE TRIGGER**: In normal operation, this should be *Disabled*. If *Enabled*, a pulse can be issued on IP_1 to start a conversion after **Take Data** is pressed. If enabled and no pulse ever comes, the program appears to be frozen. If this condition happens, disable, cancel out the error messages, and refresh.

The **Write** button sends data from the PC to the FPGA, programming the settings in the FPGA to correspond to the settings listed above. When this button is pressed, the data are written and read back. If the data read back equal the data written, the screen appears as normal; however, if the data read back is different than the data set in the fields above, the text in those fields appears in a different color than black (on most systems, it appears in a dark red color).

7.3.3.2 Device Configuration Group Box

The controls in this box set the state of device configuration bits on the selected device under test, and correspond to those pins directly.

- **Range[2:0]**: These check boxes correspond to the RANGE pins on the DDC devices, and configure the range that the DDC is in. Checked corresponds to a logic 1; unchecked is a logic 0. '000' is range 0 and '111' is range 7, etc.
- **Format**: (DDC114 only) This configures the format that the DDC114 outputs data. '1' is 20-bit data per channel; '0' is 16-bit data.
- **SPEED**: This configures the Power setting for the DDC114. Unchecked ('0') is low speed and checked ('1') is high speed.
- **Testmode**: This configures the test mode for the DDC. Unchecked ('0') turns TEST mode off, and checked ('1') is TEST mode on. TEST mode disconnects the inputs and should produce an ideal baseline for noise and offset in the system.

Pressing the **Write to Pins** button sets the corresponding device hardware pins to the states in the checkboxes.

7.3.3.3 Direct DDC Control Group Box

The **Hard Reset DDC** button applies an approximately 500ms long pulse to the nRESET pin on the DDC, resetting the device.

7.3.4 Data Summary Tab

This tab displays the data in summary form. It displays all the channels, the average value measured by the channels, the RMS noise of the measured data, the peak-to-peak noise of the measured data, and the units that all these measurements are reported in. It also displays the RMS noise of all channels averaged together at the very top left.

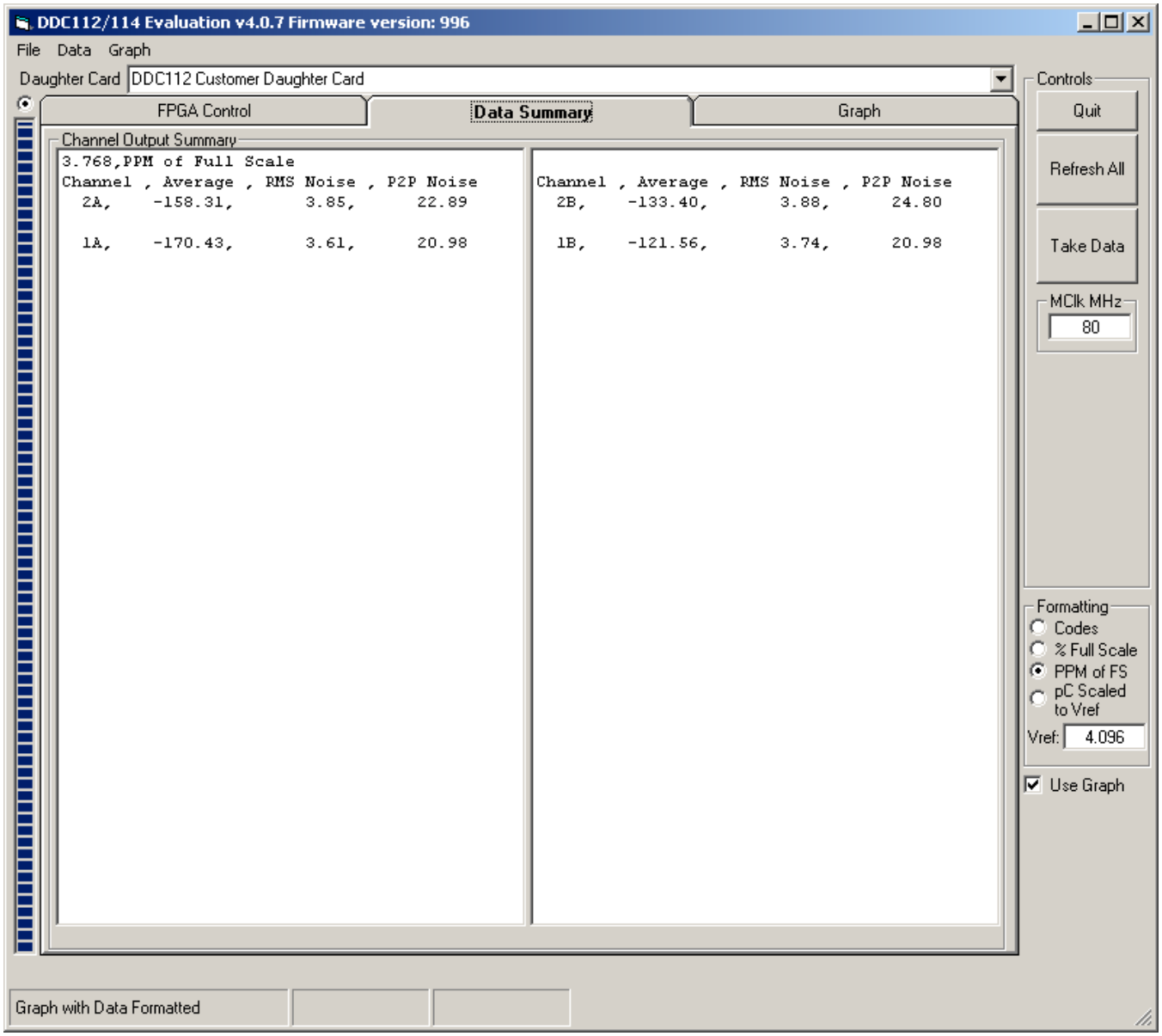


Figure 22. Data Summary Tab

The format that the data are displayed in is controlled by the formatting options set in the main window **Formatting** controls.

7.3.5 Graph Tab

The graph tab displays a graph of data versus sample acquired. It always displays the readings in codes, regardless of the **Formatting** settings. The channel to display is selected using the **Channel** combo box on the bottom of the graph.

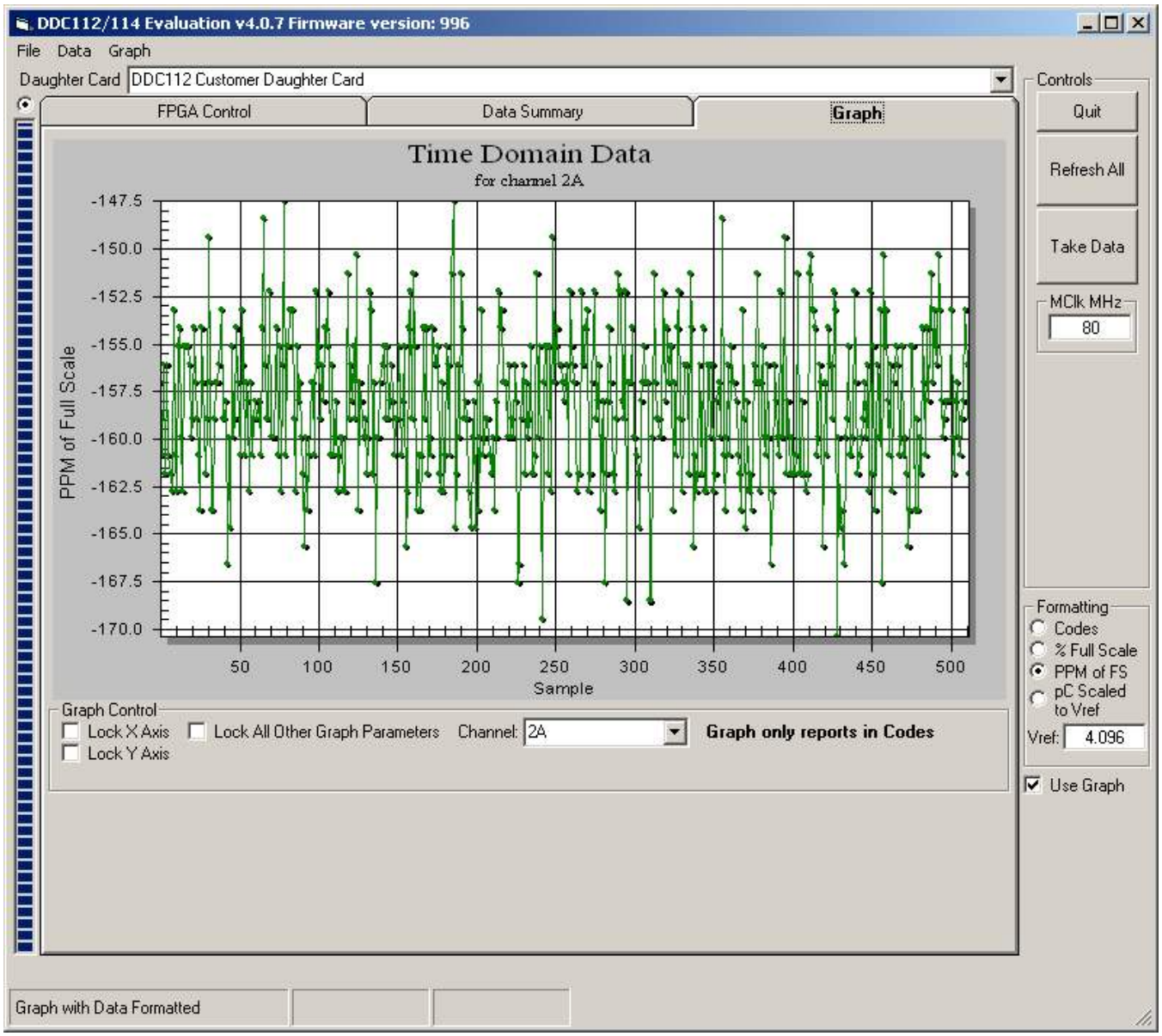


Figure 23. Graph Tab

Left-clicking and dragging a box zooms in to the selected section of the graph.

Right-clicking on the graph brings up limited zoom, format, print, and display features.

The graph zoom features can be disabled or locked using the **Lock X-axis**, **Lock Y-axis**, and **Lock All Other Graph Parameters** check boxes. These controls might be used to make it easier to zoom only horizontally or vertically without inadvertently changing the other axis.

7.4 Troubleshooting

1. If you see a dialog box as shown in Figure 24, or an error message seen on main window status bar saying *Error Writing Registers*, this message indicates that the DDCMB is either not connected via USB or has not been properly detected by the system. Verify that the USB connection is good, or press the RESET_USB (S1) button on the DDCMB to allow communication to be established.

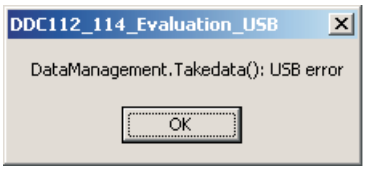


Figure 24. USB Error Notification Dialog

8 Schematics and Layout

Full-size schematics for the DDC112EVM, DDC114EVM, and DDCMB boards are appended to this user's guide. The bills of material for each board are provided in Section 8.1.

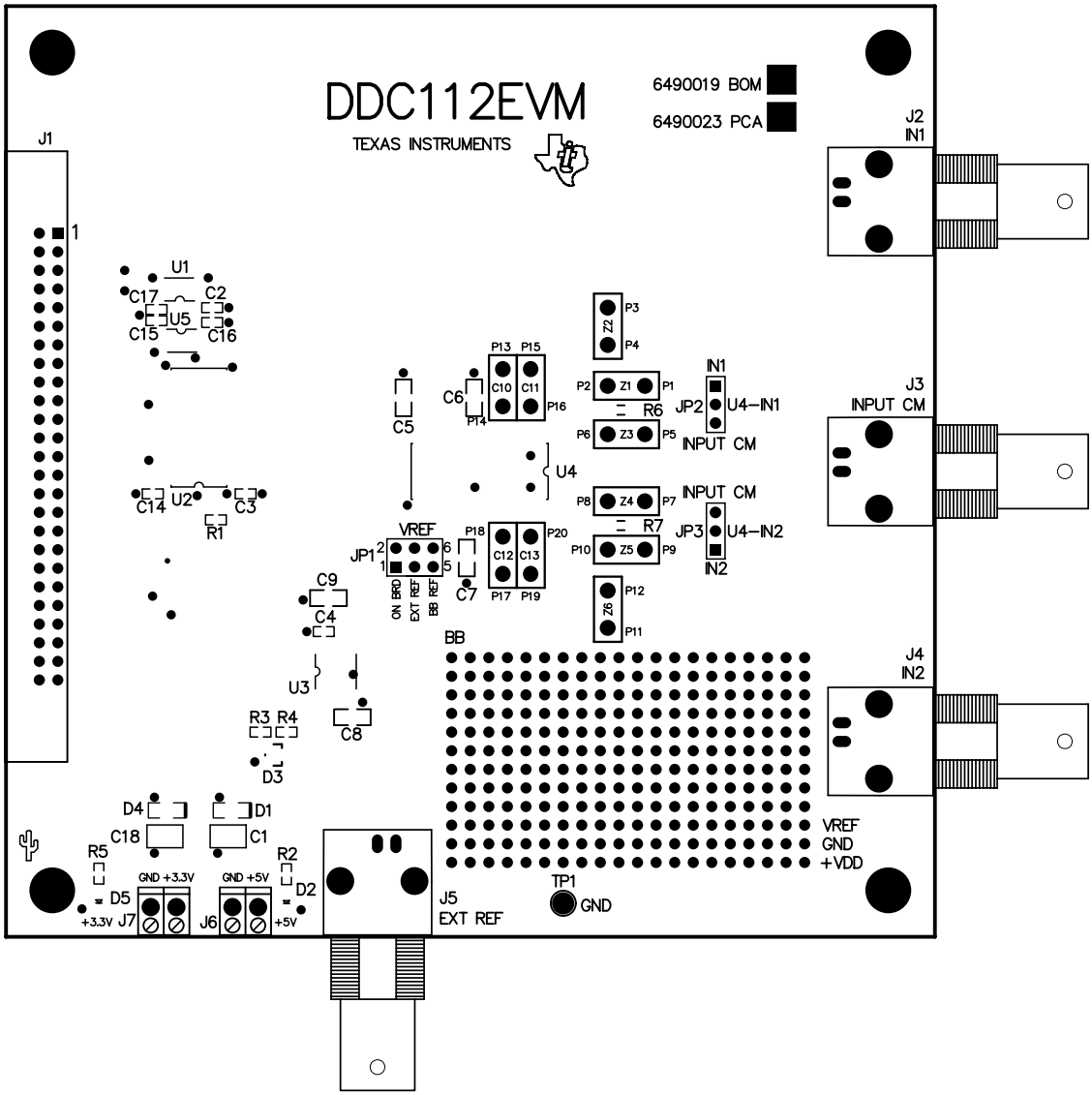


Figure 25. Silkscreen for DDC112EVM DUT Board

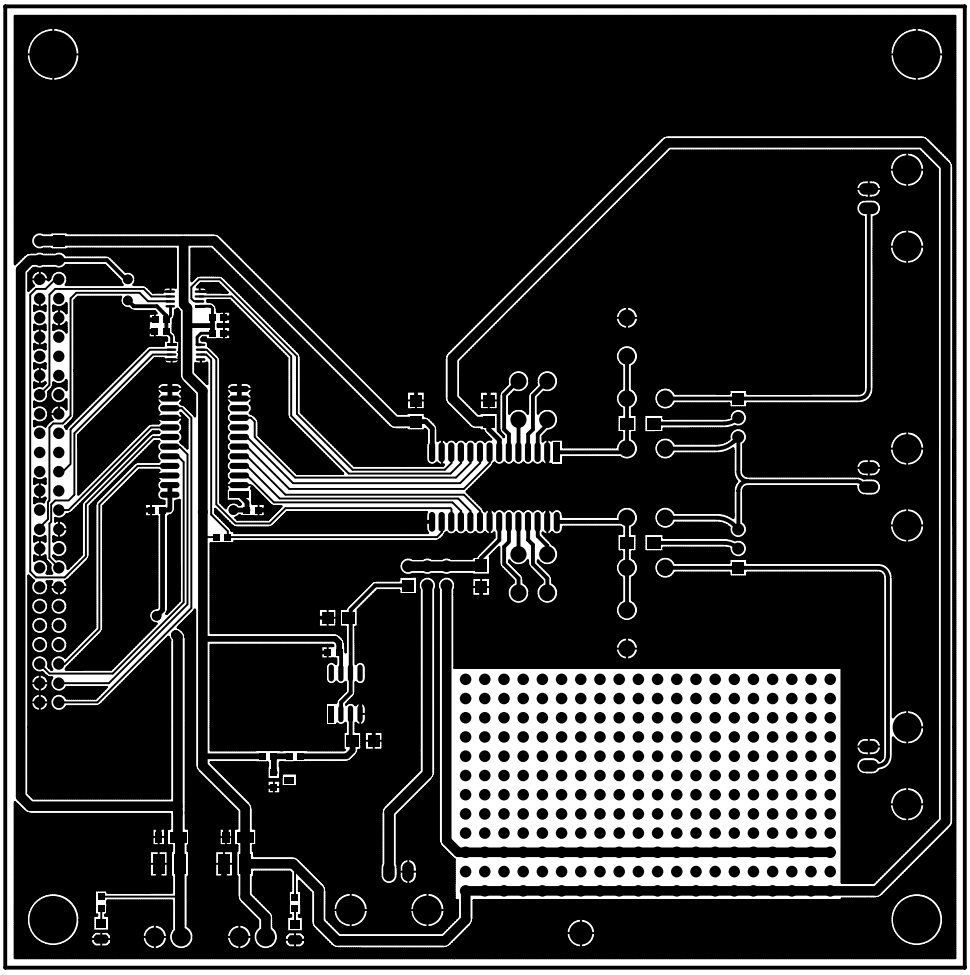


Figure 26. Top Layer of DDC112EVM DUT Board

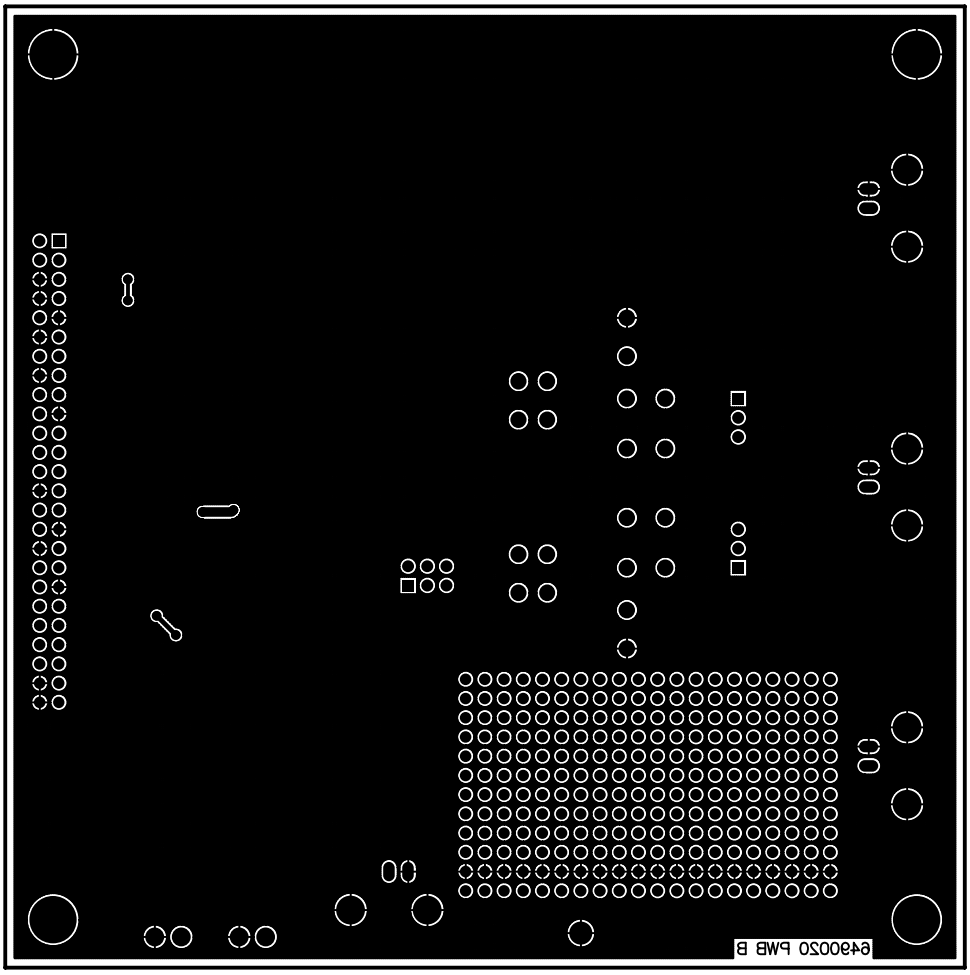


Figure 27. Bottom Layer of DDC112EVM DUT Board

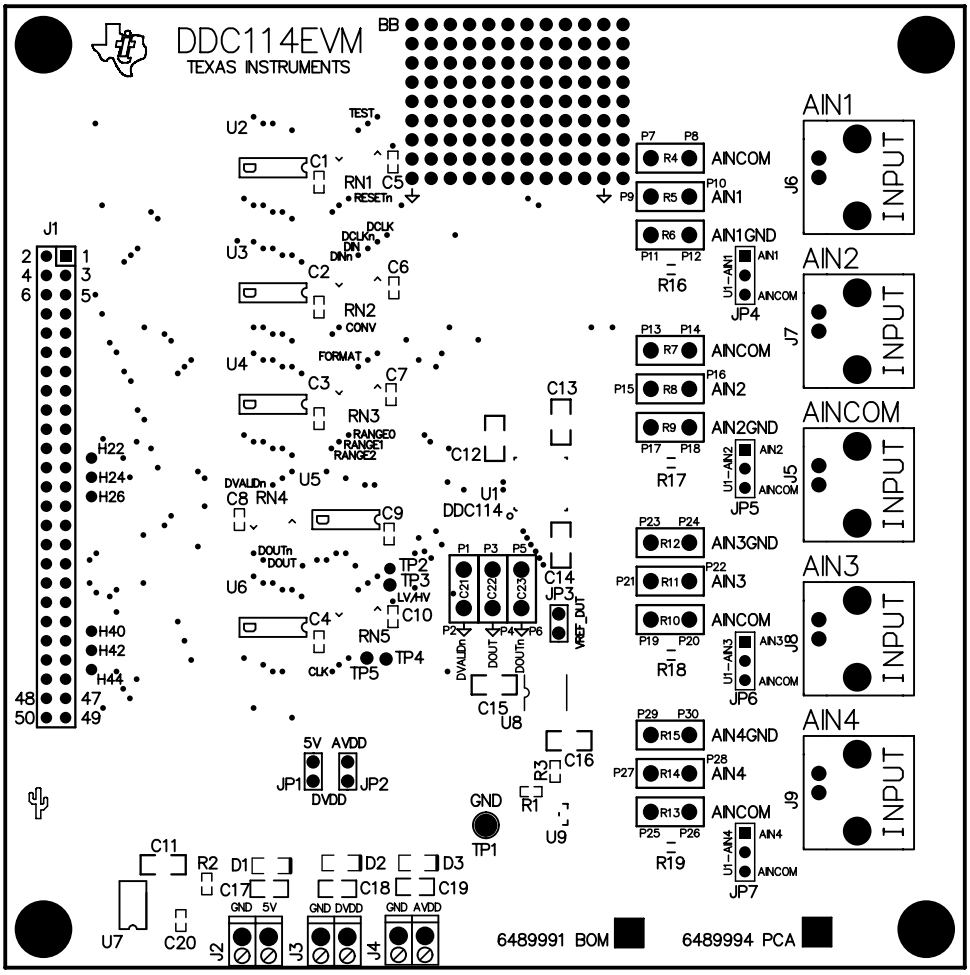


Figure 28. Silkscreen for DDC114EVM DUT Board

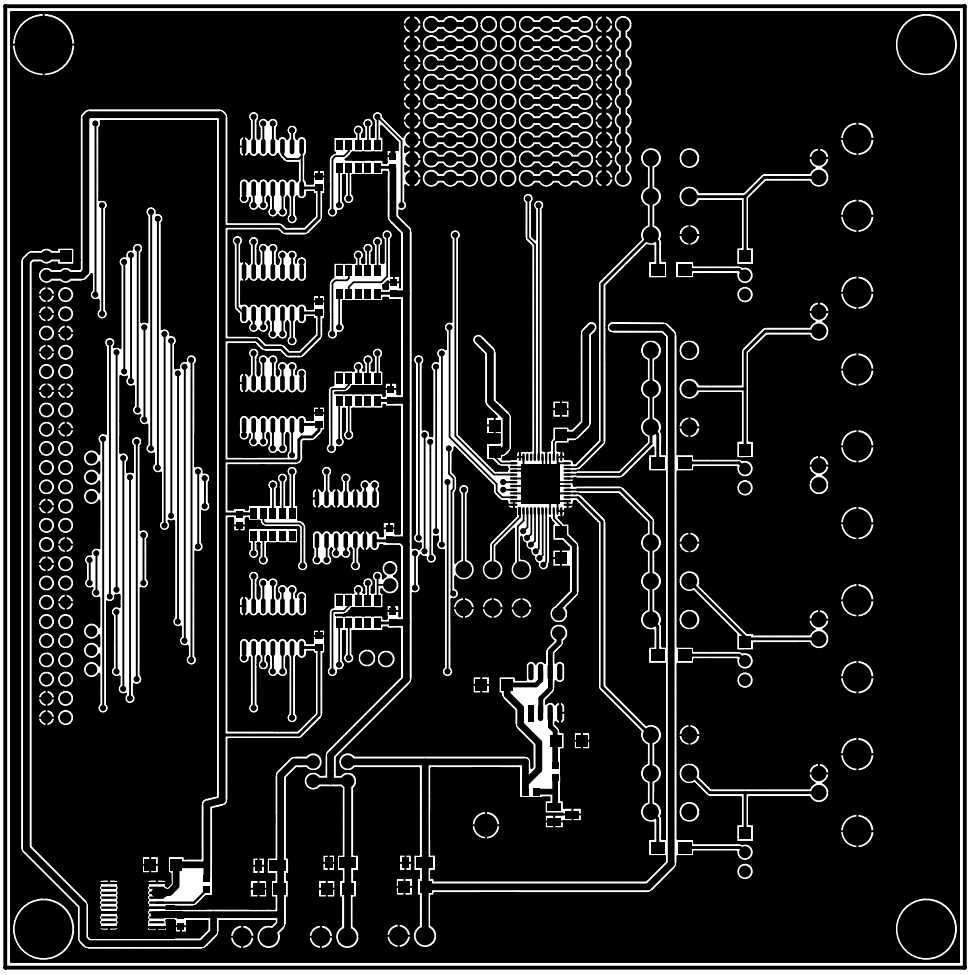


Figure 29. Top Layer of DDC114EVM DUT Board

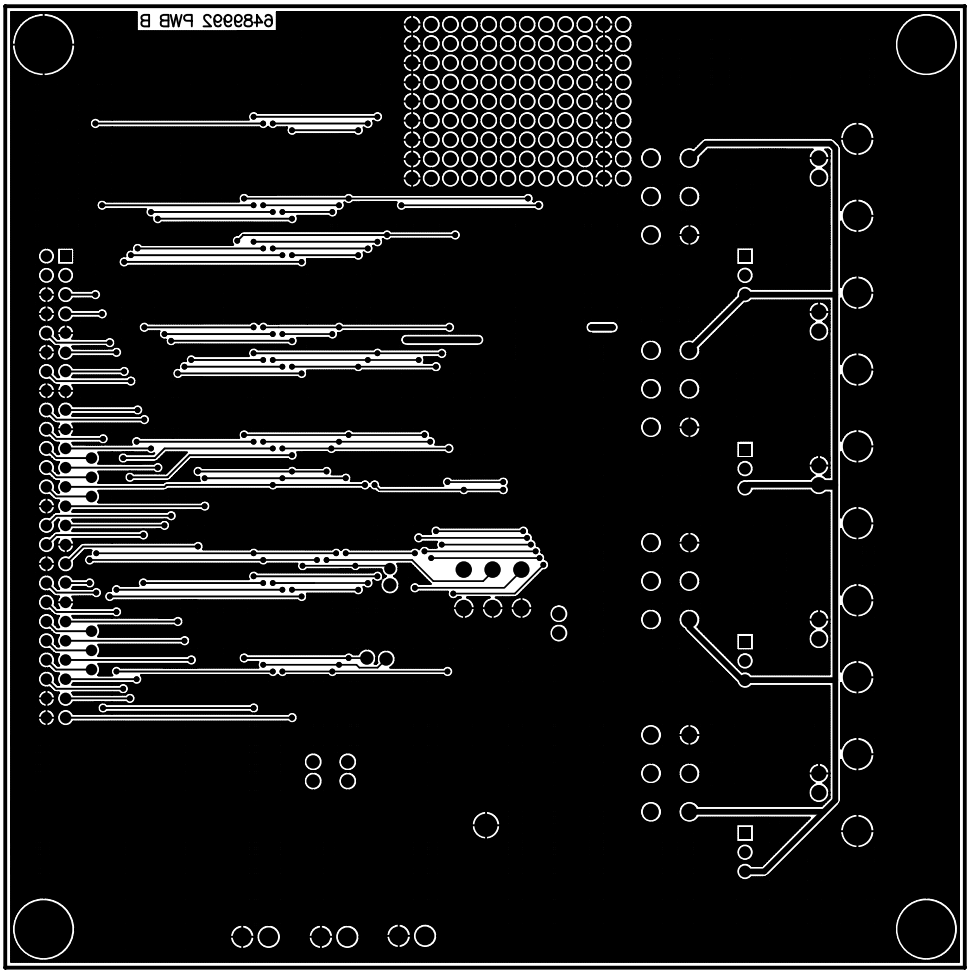


Figure 30. Bottom Layer of DDC114EVM DUT Board

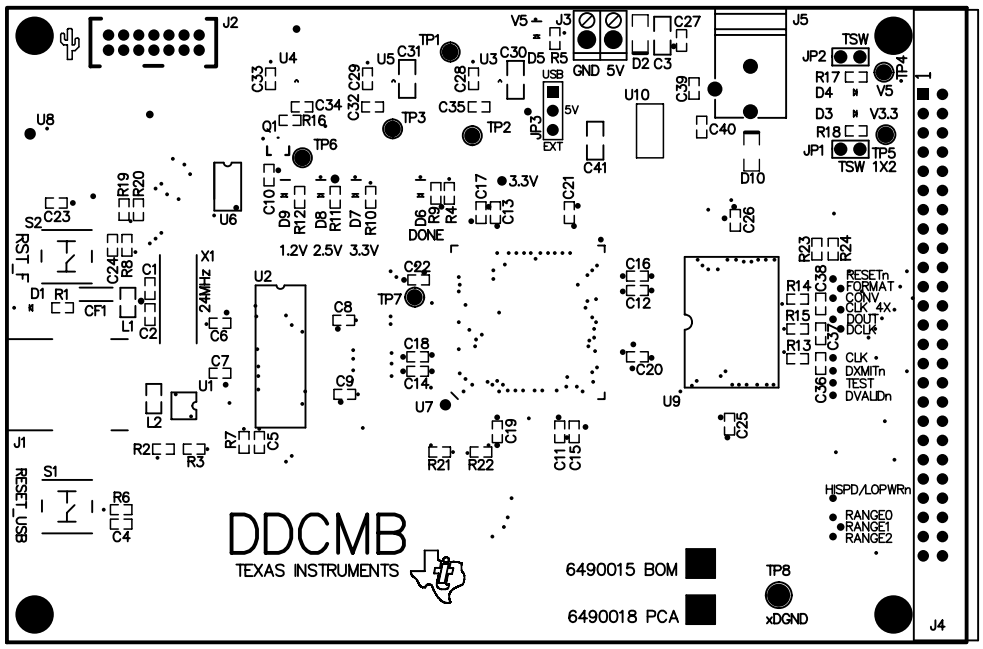


Figure 31. Silkscreen of DDCMB Motherboard

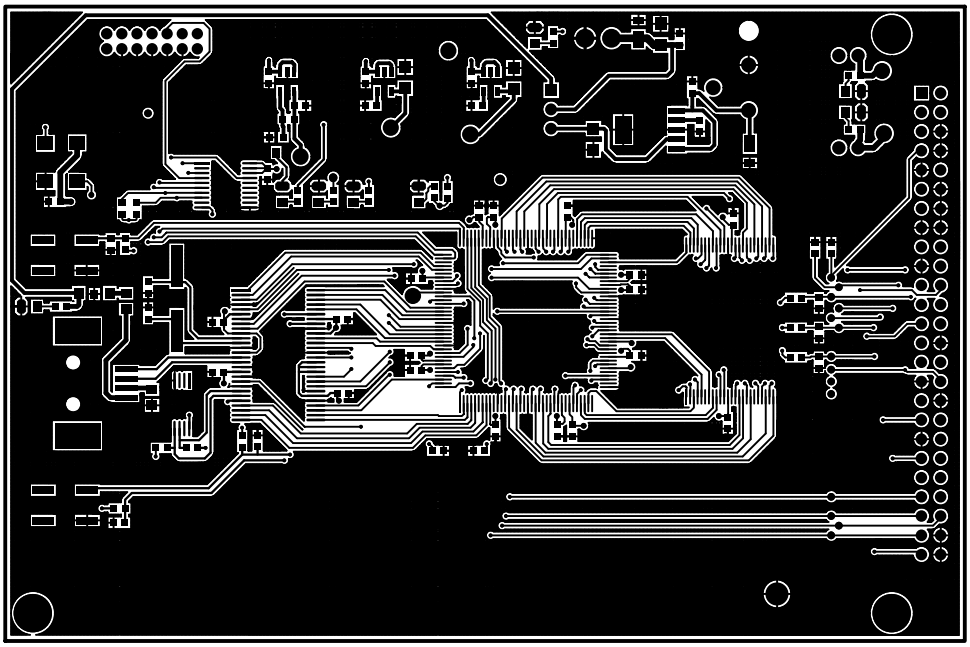


Figure 32. Top Layer of DDCMB Motherboard

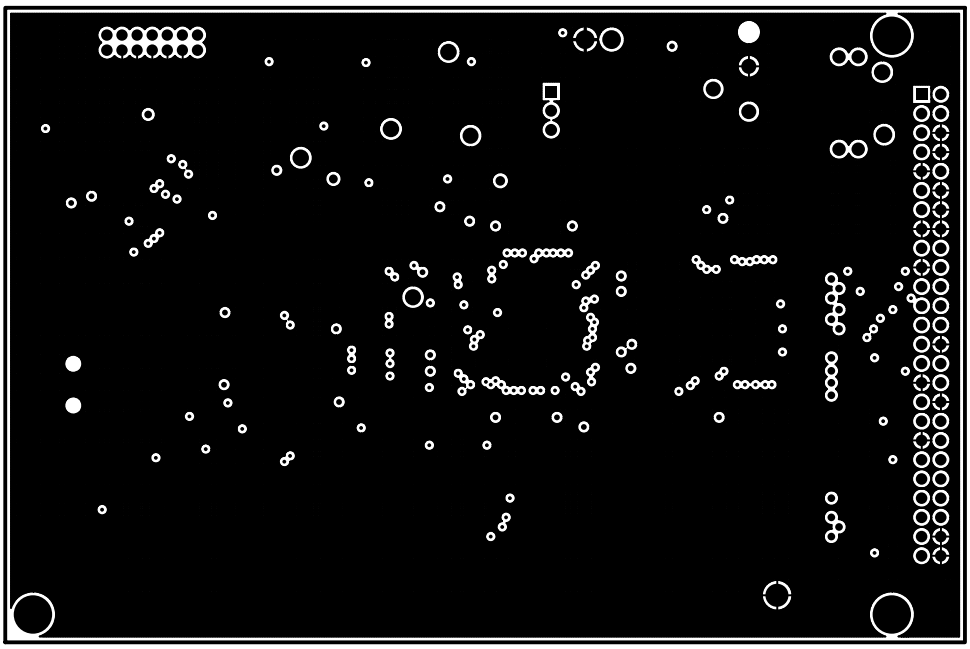


Figure 33. Mid Layer 1 of DDCMB Motherboard

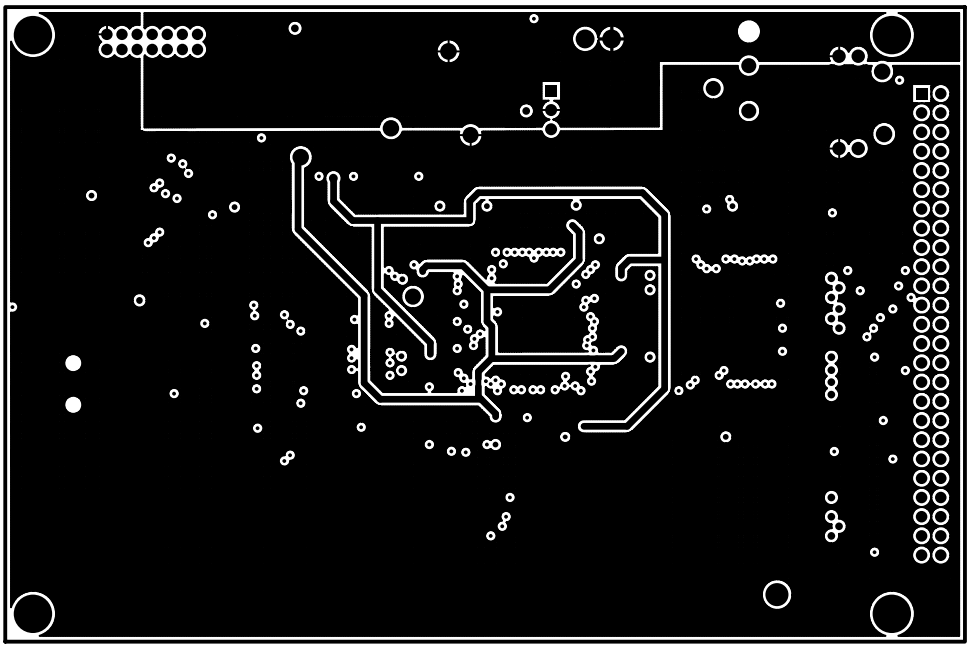


Figure 34. Mid Layer 2 of DDCMB Motherboard

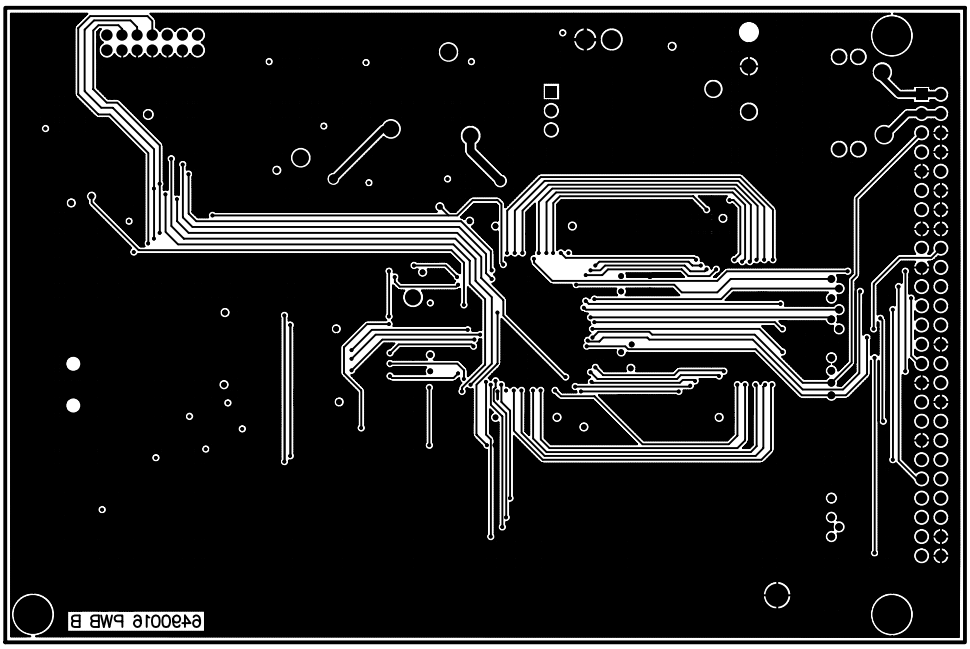


Figure 35. Bottom Layer of DDCMB Motherboard

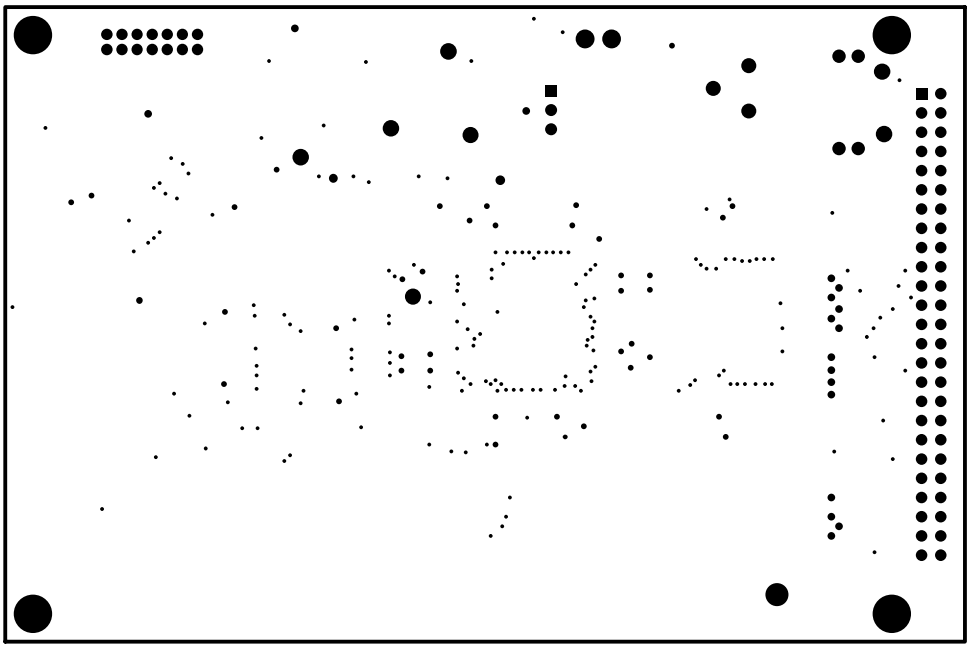


Figure 36. Bottom Silkscreen of DDCMB Motherboard

8.1 Bills of Material

NOTE: All components should be RoHS compliant. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS compliant.

Table 6. DDC112EVM Bill of Materials

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
1	4	270pF	C10, C11, C12, C13	Capacitor, 50V ceramic radial, ±5%, C0G	Vishay/BC Components	K271J15C0GF5TL2
2	7	0.1μF	C2, C3, C4, C14, C15, C16, C17	Ceramic chip capacitor, 0.1μF 50V ±10%, X7R 0603	Murata	GRM188R71H104KA93D
3	5	10μF	C5, C6, C7, C8, C9	Ceramic chip capacitor, 10μF 10V ±10%, X7R 1206	Murata	GRM31CR71A106KA01L
4	2	22μF	C1, C18	Ceramic chip capacitor, 22μF 10V ±10%, X7R 1210	Murata	GRM32ER71A226KE20L
5	2		D1, D4	Diode, Schottky, 40V, 3A, SMD	Diodes Inc.	SBR3U40P1-7
6	1		D3	Precision micropower shunt voltage reference, 4.1V	Texas Instruments	LM4040A41IDBZR
7	2		D2, D5	LED Thin 565NM green diffused 0805 SMD	Lumex	SML-LXT0805GW-TR
8	1		J1	Connector, R/A dual row 50-pin shrouded header	Samtec	TSS-125-04-L-D-RA
9	4		J2, J3, J4, J5	BNC connector, female, RA, 50Ω, PCB	Tyco/AMP	5227161-2
10	2		J6, J7	Screw terminal block, 3.5mm, 2-position PCB	On Shore Technology Inc.	ED555/2DS
11	1		JP1	Terminal strip, 3-pin (3x2)	Samtec	TSW-103-07-G-D
12	2		JP2, JP3	Terminal strip, 3-pin (3x1)	Samtec	TSW-103-07-G-S
13	8		P13-P20	Socket receptacle, 0.014-0.026, 30AU	Tyco/AMP	5050863-5
14	0	—	P1-P12	Not Installed		
15	1	200Ω	R5	Resistor 200Ω, 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF2000V
16	1	402Ω	R2	Resistor 402Ω, 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF4020V
17	1	4.99kΩ	R3	Resistor 4.99kΩ, 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF4991V
18	1	10kΩ	R4	Resistor 10kΩ, 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1002V
19	1	100kΩ	R1	Resistor 100kΩ, 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1003V
20	2	10MΩ	R6, R7	Resistor 10MΩ, 1/4W 1% MELF SMD	Vishay/BC Components	2312 155 11006
21	0	—	Z1, Z2, Z3, Z4, Z5, Z6	Not Installed		
22	1		TP1	Testpoint, Multi-purpose, black, through-Hole	Keystone Electronics	5011
23	2		U1, U5	2-bit Transceiver, noninverting	Texas Instruments	SN74LVC2T45DCTR
24	1		U2	8-bit Transceiver, noninverting	Texas Instruments	SN74LVC4245ADWR
25	1		U3	Op-amp, precision, rail-to-rail	Texas Instruments	OPA350UA
26	1		U4	Dual current input, 20-bit analog-to-digital converter	Texas Instruments	DDC112U
27	1		N/A	DDC112 EVM PWB	Texas Instruments	6490020
28	2		N/A	DDC112 EVM shield PWB	Texas Instruments	6490021
29	4		N/A	1/4", Hex spacer, 6-32 thread	Keystone Electronics	2208
30	2		N/A	3/4", Hex spacer, 6-32 thread	Keystone Electronics	2211
31	2		N/A	3/4", Hinged spacer, 6-32 thread	Keystone Electronics	353
32	2		N/A	1/4", Machine screw, Phillips head, 6-32 thread	B&F Fastener Supply	PMSSS 632 0025 PH
33	4		N/A	1/2", Machine screw, Phillips head, 6-32 thread	B&F Fastener Supply	PMSSS 632 0050 PH
34	3		N/A	Shorting blocks	Samtec	SNT-100-BK-G-H

Table 7. DDC114EVM Bill of Materials

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
1	10	0.1μF	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	Ceramic chip capacitor, 0.1μF 50V ±10%, X7R 0603	Murata	GRM188R71H104KA93D
2	1	0.33μF	C20	Ceramic chip capacitor, 0.33μF 16V ±10%, X7R 0603	Murata	GRM188R71C334KA01D
3	8	10μF	C12, C13, C14, C15, C16, C17, C18, C19	Ceramic chip capacitor, 10μF 10V ±10%, X7R 1206	Murata	GRM31CR71A106KA01L
4	1	47μF	C11	Ceramic chip capacitor, 47μF 6.3V ±20%, X5R 1206	Murata	GRM31CR60J476ME19L
5	—		C21, C22, C23	Not Installed		
6	3		D1, D2, D3	Diode, Schottky, 40V, 3A, SMD	Diodes Inc.	SBR3U40P1-7
7	1		J1	Connector, R/A dual row 50-pin shrouded header	Samtec	TSS-125-04-L-D-RA
8	5		J5, J6, J7, J8, J9	BNC connector, female, RA, 50Ω, PCB	Tyco/AMP	5227161-2
9	3		J2, J3, J4	Screw terminal block,3.5mm 2-position PCB	On Shore Technology Inc.	ED555/2DS
10	3		JP1, JP2, JP3	Terminal strip, 2-pin (1x2)	Samtec	TSW-102-07-G-S
11	4		JP4, JP5, JP6, JP7	Terminal strip, 3-pin (1x3)	Samtec	TSW-103-07-G-S
12	—		P1-P30	Socket receptacle, 0.014-0.026, 30AU—Not Installed		
13	1	6.49kΩ	R1	Resistor 6.49kΩ, 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF6491V
14	2	10kΩ	R2, R3	Resistor 10kΩ, 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1002V
15	4	10MΩ	R16, R17, R18, R19	Resistor 10MΩ, 1/4W 1% MELF SMD	Vishay/BC Components	2312 155 11006
16	—		R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15	Not Installed		
17	1	330Ω	RN4	Resistor Array 330Ω, 10-terminal bussed SMD	CTS Resistor Products	745C101331JPTR
18	4	1kΩ	RN1, RN2, RN3,RN5	Resistor Array 1kΩ, 10-terminal bussed SMD	CTS Resistor Products	745C101102JPTR
19	1		TP1	Testpoint, multi-purpose, black, through-hole	Keystone Electronics	5011
20	—		TP2, TP3, TP4, TP5	Not Installed		
21	1		U1	20-bit quad input ADC, 48-QFN	Texas Instruments	DDC114IRTCT
22	5		U2-U6	Hex buffer/driver w/open drain	Texas Instruments	SN74LVC07AD
23	1		U7	3.3V 2A LDO regulator 20-HTSSOP	Texas Instruments	TPS75233QPWP
24	1		U8	Op-amp, precision, rail-to-rail	Texas Instruments	OPA350UA
25	1		U9	Precision micropower shunt voltage reference, 4.1V	Texas Instruments	LM4040A41IDBZR
26	1		N/A	DDC114VM PWB	Texas Instruments	6489992
27	2		N/A	DDC114EVM-Shield PWB	Texas Instruments	6489997
28	4		N/A	1/4", Hex spacer, 6-32 thread	Keystone Electronics	2208
29	2		N/A	3/4", Hex spacer, 6-32 thread	Keystone Electronics	2211
30	2		N/A	3/4", Hinged spacer, 6-32 thread	Keystone Electronics	353
31	2		N/A	1/4", Machine screw, Phillips head, 6-32 thread	B&F Fastener Supply	PMSSS 632 0025 PH
32	4		N/A	1/2", Machine screw, Phillips head, 6-32 thread	B&F Fastener Supply	PMSSS 632 0050 PH
33	7		N/A	Shorting block	Samtec	SNT-100-BK-G-H

Table 8. DDCMB Bill of Materials

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
1	2	10pF	C1, C2	50V Ceramic chip capacitor, ±5%, C0G, 0603	Murata	GRM1885C1H100JA01D
2	3	47pF	C36, C37, C38	50V Ceramic chip capacitor, ±5%, C0G, 0603	Murata	GRM1885C1H470JA01D
3	3	0.01μF	C32, C35, C40	50V Ceramic chip capacitor, ±10%, X7R, 0603	Murata	GRM188R71H103MA01D
4	25	0.1μF	C4-C27, C39	50V Ceramic chip capacitor, ±10%, X7R, 0603	Murata	GRM188R71H104KA93D
5	2	0.33μF	C28, C29	16V Ceramic chip capacitor, ±10%, X7R, 0603	Murata	GRM188R71C334KA01D
6	2	1μF	C33, C34	16V Ceramic chip capacitor, ±10%, X7R, 0603	Murata	GRM188R71C105KA12D
7	4	10μF	C3, C30, C31, C41	16V Ceramic chip capacitor, ±10%, X5R, 1206	Murata	GRM31CR61C106KC31L
8	1		CF1	50V, 2200pF EMI filter, SMD	Panasonic	EXC-CET222U
9	8		D1, D3, D4, D5, D6, D7, D8, D9	LED green, SMD 0805	Lumex	SML-LXT0805GW-TR
10	2		D2, D10	Diode, Schottky, 40V, 3A, SMD	Diodes Inc.	SBR3U40P1-7
11	1		J1	Connector, USB type B, PCB	KobiConn	154-UBR44-E
12	1		J2	Header, 14-position, 2mm, Vvertical	Molex	87831-1420
13	1		J3	Terminal block, 3.5mm, 2-position	On Shore Technology	ED555/2DS
14	1		J4	Connector, R/A dual row 50-pin socket	Samtec	SSW-125-02-F-D-RA
15	1		J5	2.5mm Power connector	CUI Stack	PJ-102BH
16	2		JP1, JP2	1 X 2 header	Samtec	TSW-102-07-G-S
17	1		JP3	1 X 3 header	Samtec	TSW-103-07-G-S
18	2		L1, L2	Ferrite bead core, 0805	Panasonic	EXC-ML20A390U
19	1		Q1	MOSFET N-channel 30V 2.2A SOT-23-3	Fairchild	FDN337N
20	3	33Ω	R13, R14, R15	1/10W 5% chip resistor SMD, 0603	Panasonic	ERJ-3GEYJ330V
21	1	100Ω	R11	1/10W 1% chip resistor SMD, 0603	Panasonic	ERJ-3EKF1000V
22	2	200Ω	R10, R18	1/10W 1% chip resistor SMD, 0603	Panasonic	ERJ-3EKF2000V
23	3	402Ω	R5, R12, R17	1/10W 1% chip resistor SMD, 0603	Panasonic	ERJ-3EKF4020V
24	2	499Ω	R4, R9	1/10W 1% chip resistor SMD, 0603	Panasonic	ERJ-3EKF4990V
25	1	511Ω	R1	1/10W 1% chip resistor SMD, 0603	Panasonic	ERJ-3EKF5110V
26	2	2.21kΩ	R2, R3	1/10W 1% chip resistor SMD, 0603	Panasonic	ERJ-3EKF2211V
27	2	4.99kΩ	R19, R20	1/10W 1% chip resistor SMD, 0603	Panasonic	ERJ-3EKF4991V
28	1	10kΩ	R16	1/10W 5% chip resistor SMD, 0603	Panasonic	ERJ-3GEYJ103V
29	4	47kΩ	R21, R22, R23, R24	1/10W 5% chip resistor SMD, 0603	Panasonic	ERJ-3GEYJ473V
30	3	100kΩ	R6, R7, R8	1/10W 5% chip resistor SMD, 0603	Panasonic	ERJ-3GEYJ104V
31	2		S1, S2	Momentary tactile switch, 6.2mm, 160gf	C K	KSC222J LFS
32	1		U1	5V, Serial EEPROM 128 bit, TSSOP	Microchip	24LC00-I/ST
33	1		U2	USB Hi-speed periperal IC MCU	Cypress	CY7C68013A-56PVXC
34	1		U3	3.3V, 400mA LDO regulator	Texas Instruments	REG113NA-3.3
35	1		U4	1.2V, 120mA LDO regulator	Texas Instruments	SN105125DBVR
36	1		U5	2.5V, 400mA LDO regulator	Texas Instruments	REG113NA-2.5
37	1		U6	3.3V PROM	Xilinx	XCF04SVOG20C
38	1		U7	FPGA, Spartan 3E	Xilinx	XC3S250E-4TQG144C
39	1	80.0MHz	U8	3.3V Oscillator, ±50ppm, SMD	Connor-Winfield	CWX823-80.0M
40	1		U9	16MB SRAM IC ASYNC	ISSI	IS61WV102416BLL-10TLI
41	1		U10	5V, 800mA LDO regulator	Texas Instruments	REG104GA-5
42	—		TP1, TP2, TP3, TP4, TP5, TP6, TP7	Not Installed		
43	1		TP8	Testpoint, multi-purpose, black, through-hole	Keystone Electronics	5011
44	1	24.000MHz	X1	Crystal, 18pF, HC49/US SMD	Citizen	HCM49 24.000MABJ-UT

Table 8. DDCMB Bill of Materials (continued)

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
45	1		N/A	DDCMB PWB	Texas Instruments	6490016
46	4		N/A	Machine screws, Phillips lead 6-32 x 5/16	Building Fasteners	PMSSS 632 0031 PH
47	4		N/A	Hex standoff 6-32, 0.5"	Keystone Electronics	2210
48	3		N/A	Shorting block	Samtec	SNT-100-BK-G-H

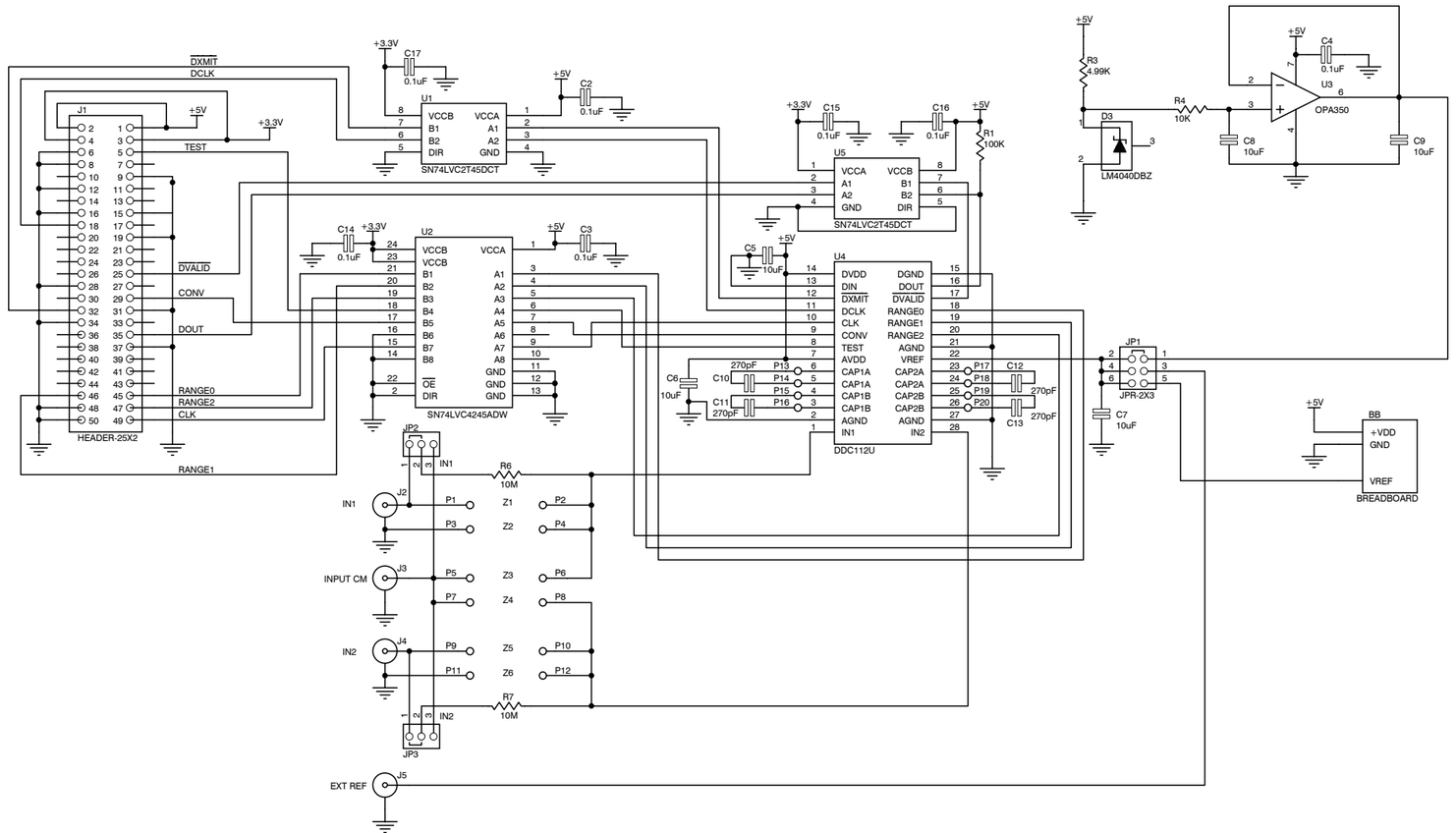
Revision History

Changes from Original (October, 2007) to A Revision **Page**

- Revised name of DDC112EVM board; changed all occurrences of *DEM_DDC112U-C* to *DDC112EVM* 1
- Revised Table 5 3
- Updated identification of sockets on DUT board to reflect new names (P13 to P20) 4
- Changed descriptions of optional external capacitors 4
- Deleted description of Robinson-Nugent socket for DUT on EVM board and previous Figure 4 5
- Updated paragraph discussing why DDCMB and DUT boards are separate boards 5
- Changed name of BNC connector to J5 in text and Table 2 6
- Revised Figure 5 to reflect new nomenclature on board 7
- Updated text that discusses optional component sockets to reflect new nomenclature on board 7
- Changed description of positions where external capacitors can be inserted 8
- Changed Figure 6 to reflect new nomenclature on board 8
- Updated hardware description; changed references of jumpers J6 and J16 to JP1 and JP2 in text and Table 4. Changed J17, J18, and J19 to J2, J3, and J4, respectively 9
- Changed paragraph discussing input channel connections 10
- Deleted previous Table 6 and related text 10
- Updated *Motherboard Connectors* section 10
- Changed *Motherboard Jumpers* section. Deleted previous Table 7 and Table 8 10
- Updated *Motherboard Switches* section 11
- Revised Table 5 11
- Updated paragraph about installing USB drivers 11
- Revised *Evaluating a DDC11x Device: Quick Start* 17
- Updated *Troubleshooting* section 24
- Removed schematics for DEM-DDC112 cable interface adapter (previous Figure30 through Figure 33); updated schematics and PCB layouts for all related devices. Removed smaller-sized schematics (previous Figure 25, Figure 29, Figure 30, and Figure 34 through Figure 36) 25
- Added Figure 31 through Figure 36 30
- Revised Table 6, Table 7, and Table 8 34

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED



TEXAS INSTRUMENTS

PRECISION ANALOG PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

5411 EAST WILLIAMS BOULEVARD, TUCSON, AZ 85711 USA

ENGINEER **RICK DOWNS**	TITLE **DDC112EVM**		
DRAWN BY **BOB BENJAMIN**			
DOCUMENT CONTROL NO. **6490022**	SIZE **B**	DATE **1-APR-2010**	REV **B**
SHEET **1** OF **1**	FILE		

REVISION HISTORY

REV	ENGINEERING CHANGE NUMBER	APPROVED

TO MOTHER BOARD

J1: +5V, +5V, +3.3V, +3.3V, TEST, GNDD, RESETn, GNDD, GNDD, GNDD, GNDD, DCLK, GNDD, H22, H24, DVALIDn, H26, GNDD, CONV, GNDD, GNDD, DOUT, DOUTn, GNDD, EXTRA2, CLK_4X, H40, FORMAT, H42, HISPD/LOPWRn, H44, RANGE0, RANGE1, RANGE2, GNDD, CLK, GNDD

U2, U3, U4, U5, U6: 74LVC07A

RN1, RN2, RN3, RN5: 1K; RN4: 330

C1–C10: 0.1uF; C11: 47uF; C12: 10uF; C13: 10uF; C14: 10uF; C15: 10uF; C16: 10uF; C17: 10uF; C18: 10uF; C19: 10uF; C20: 0.33uF

D1, D2, D3: SBR3U40P1

J2, J3, J4: SBR3U40P1

JP1, JP2, JP3, JP4, JP5, JP6, JP7

R1: 6.49K; R2: 10K; R3: 10K; R4–R15: 10M

TP1, TP2, TP3, TP4, TP5

U1: DDC114

U7: TPS75233Q

U8: OPA350UA

U9: LM4040A41DBZ

BNC: J5, J6, J7, J8, J9

AIN1-4, AIN1, AIN2, AIN3, AIN4

TEST, RESETn, DCLK, CONV, HISPD/LOPWRn, FORMAT, CLK_4X, RANGE2, RANGE1, RANGE0, DVALID, DOUTn, DOUT, CLK

POWER, DUT DIGITAL, DUT ANALOG, REGULATOR

VREF

BB AREA

* C21, C22, C23 : SOCKET.
* R4 THROUGH R15: SOCKET.

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PRECISION ANALOG PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
5411 EAST WILLIAMS BOULEVARD, TUCSON, AZ 85711 USA

ENGINEER **JASON BRIDGMON**	TITLE **DDC114EVM**		
DRAWN BY **M. LOVE/B. BENJAMIN**			
DOCUMENT CONTROL NO. **6489993**	SIZE **B**	DATE **1-APR-2010**	REV **B**
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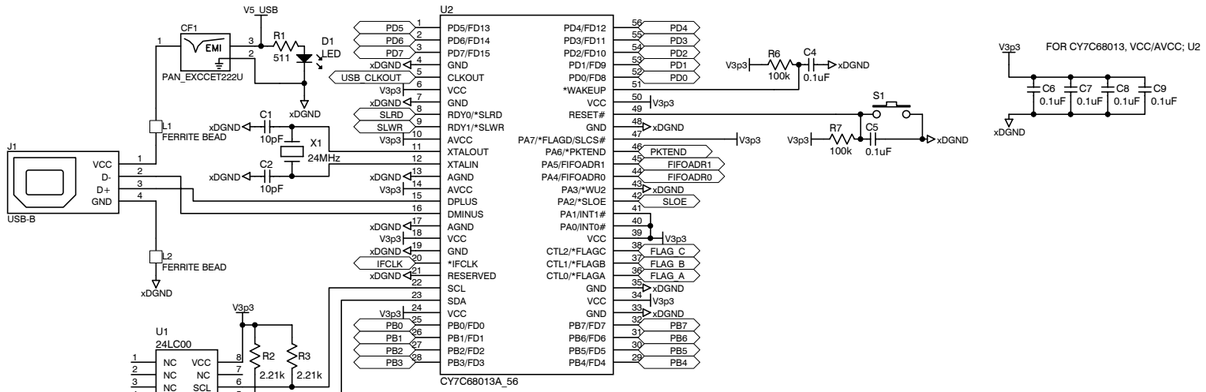
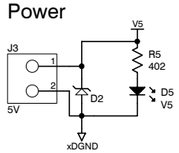
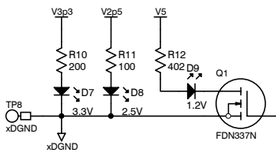
REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED

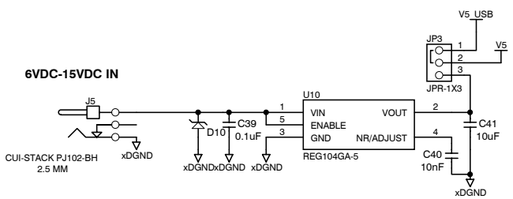
USB and Support Circuitry

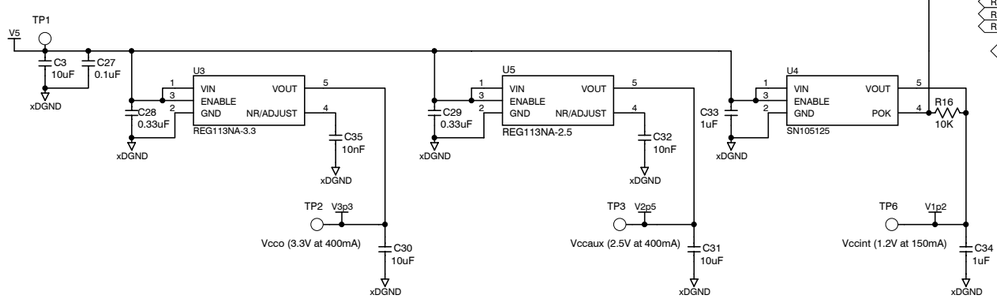


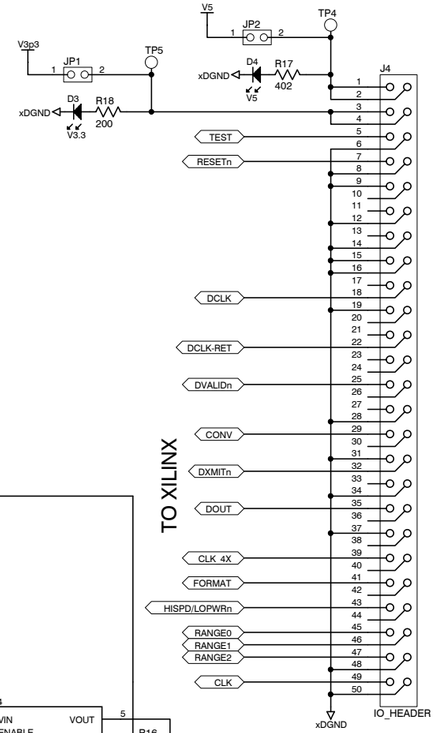
Power











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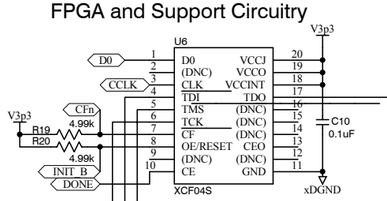
PRECISION ANALOG PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

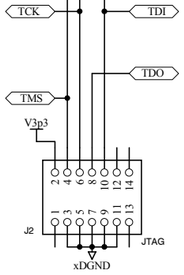
5411 EAST WILLIAMS BOULEVARD, TUCSON, AZ 85711 USA

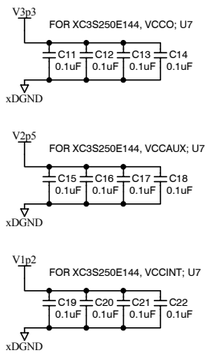
ENGINEER	**JASON BRIDGMON**	TITLE	**DDCMB**		
DRAWN BY	**M LOVE/B BENJAMIN**				
DOCUMENT CONTROL NO.	**6490017**	SIZE **B**	DATE **16-MAR-2010**	REV **B**	
SHEET **1** OF **2**		FILE			

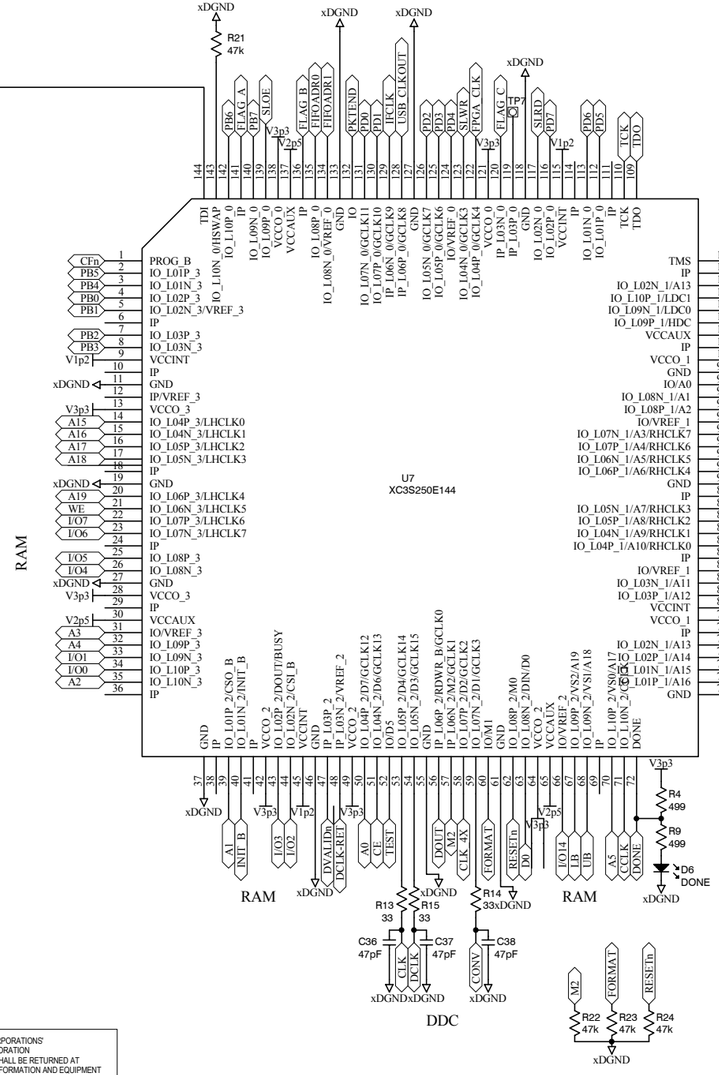
REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED

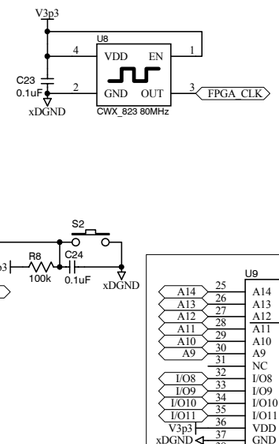
FPGA and Support Circuitry

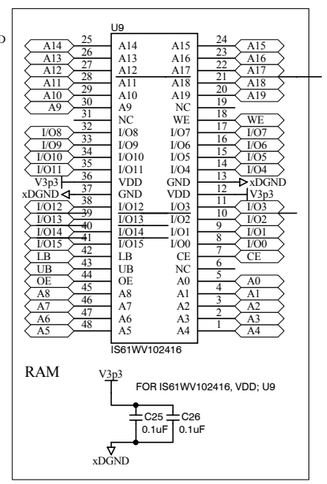












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PRECISION ANALOG PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
5411 EAST WILLIAMS BOULEVARD, TUCSON, AZ 85711 USA

ENGINEER	**JASON BRIDGMON**
DRAWN BY	**M LOVE/B BENJAMIN**
DOCUMENT CONTROL NO.	**6490017**
SHEET	**2** OF **2**

TITLE **DDCMB**

SIZE	DATE	REV
B	**16-MAR-2010**	**B**

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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