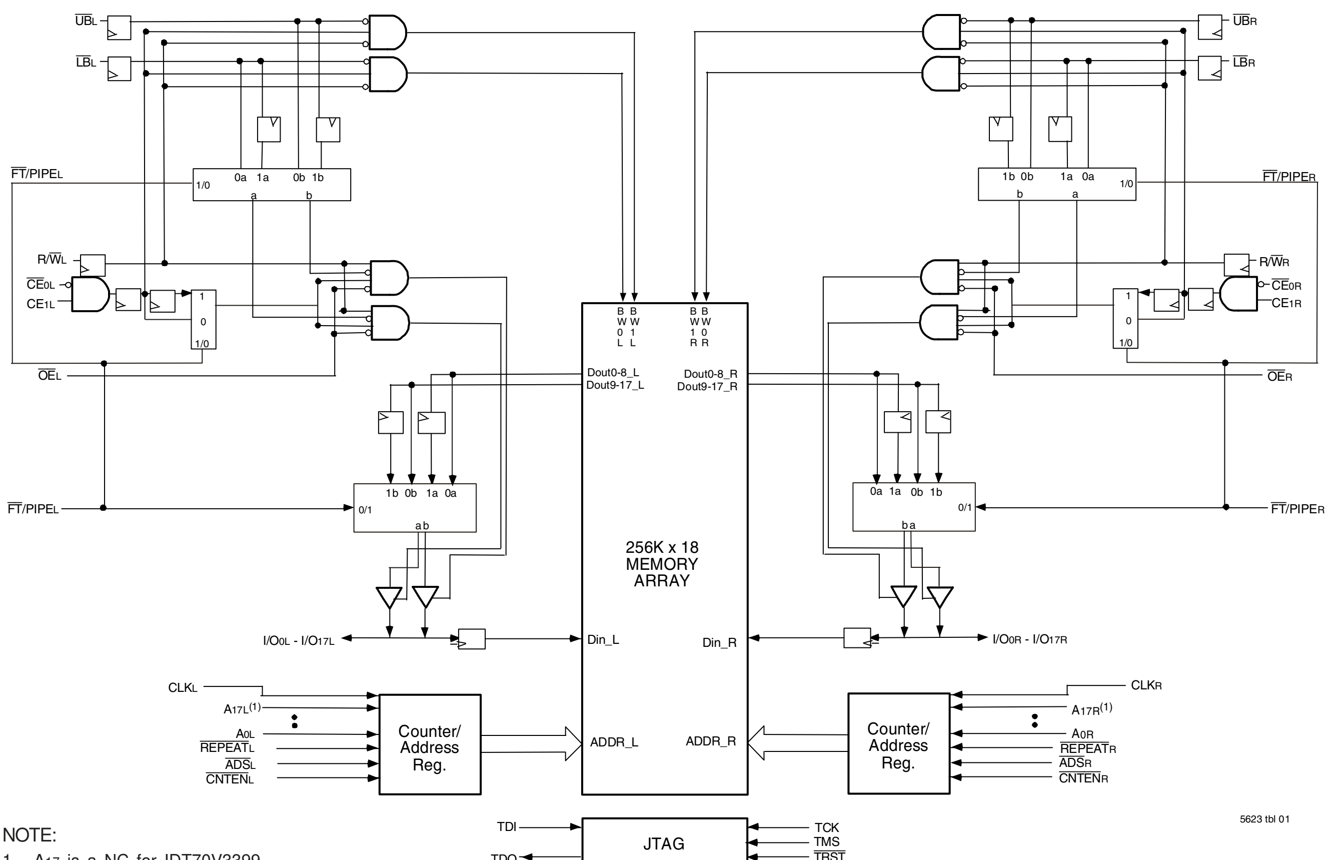
HIGH-SPEED 3.3V 256/128K x 18 SYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

70V3319/99S

Features:

- True Dual-Port memory cells which allow simultaneous access of the same memory location
- High-speed data access
  - *Commercial: 3.6ns (166MHz)/4.2ns (133MHz) (max.)*
  - *Industrial: 4.2ns (133MHz) (max.)*
- Selectable Pipelined or Flow-Through output mode
  - *Due to limited pin count PL/$\overline{FT}$ option is not supported on the 128-pin TQFP package. Device is pipelined outputs only on each port.*
- Counter enable and repeat features
- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - *6ns cycle time, 166MHz operation (6Gbps bandwidth)*
  - *Fast 3.6ns clock to data out*
  - *1.7ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 166MHz*
  - *Data input, address, byte enable and control registers*
  - *Self-timed write allows fast cycle time*
- Separate byte controls for multiplexed bus and bus matching compatibility
- Dual Cycle Deselect (DCD) for Pipelined Output mode
- LVTTL- compatible, single 3.3V (±150mV) power supply for core
- LVTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port
- Industrial temperature range (-40°C to +85°C) is available at 133MHz.
- Available in a 128-pin Thin Quad Flatpack, 208-pin fine pitch Ball Grid Array, and 256-pin Ball Grid Array
- Supports JTAG features compliant to IEEE 1149.1
  - *Due to limited pin count, JTAG is not supported on the 128-pin TQFP package*
- Green parts available, see ordering information

Functional Block Diagram



NOTE:
1. A17 is a NC for IDT70V3399.

NOVEMBER 2019

Description:

The IDT70V3319/99 is a high-speed 256/128K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3319/99 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3319/99 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V_{DD}) remains at 3.3V.

Pin Configuration(1,2,3,4,5)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	I/O9L	NC	VSS	TDO	NC	A16L	A12L	A8L	NC	VDD	CLKL	$\overline{CNTEN}_L$	A4L	A0L	OPTL	NC	VSS
B	NC	VSS	NC	TDI	A17L(1)	A13L	A9L	NC	$\overline{CE}_{0L}$	VSS	$\overline{ADS}_L$	A5L	A1L	VSS	VDDQR	I/O8L	NC
C	VDDQL	I/O9R	VDDQR	PIPE/$\overline{FT}_L$	NC	A14L	A10L	$\overline{UB}_L$	CE1L	VSS	R/$\overline{W}_L$	A6L	A2L	VDD	I/O8R	NC	VSS
D	NC	VSS	I/O10L	NC	A15L	A11L	A7L	$\overline{LB}_L$	VDD	$\overline{OE}_L$	$\overline{REPEAT}_L$	A3L	VDD	NC	VDDQL	I/O7L	I/O7R
E	I/O11L	NC	VDDQR	I/O10R										I/O6L	NC	VSS	NC
F	VDDQL	I/O11R	NC	VSS										VSS	I/O6R	NC	VDDQR
G	NC	VSS	I/O12L	NC										NC	VDDQL	I/O5L	NC
H	VDD	NC	VDDQR	I/O12R										VDD	NC	VSS	I/O5R
J	VDDQL	VDD	VSS	VSS										VSS	VDD	VSS	VDDQR
K	I/O14R	VSS	I/O13R	VSS										I/O3R	VDDQL	I/O4R	VSS
L	NC	I/O14L	VDDQR	I/O13L										NC	I/O3L	VSS	I/O4L
M	VDDQL	NC	I/O15R	VSS										VSS	NC	I/O2R	VDDQR
N	NC	VSS	NC	I/O15L										I/O1R	VDDQL	NC	I/O2L
P	I/O16R	I/O16L	VDDQR	NC	$\overline{TRST}$	A16R	A12R	A8R	NC	VDD	CLKR	$\overline{CNTEN}_R$	A4R	NC	I/O1L	VSS	NC
R	VSS	NC	I/O17R	TCK	A17R(1)	A13R	A9R	NC	$\overline{CE}_{0R}$	VSS	$\overline{ADS}_R$	A5R	A1R	VSS	VDDQL	I/O0R	VDDQR
T	NC	I/O17L	VDDQL	TMS	NC	A14R	A10R	$\overline{UB}_R$	CE1R	VSS	R/$\overline{W}_R$	A6R	A2R	VSS	NC	VSS	NC
U	VSS	NC	PIPE/$\overline{FT}_R$	NC	A15R	A11R	A7R	$\overline{LB}_R$	VDD	$\overline{OE}_R$	$\overline{REPEAT}_R$	A3R	A0R	VDD	OPTR	NC	I/O0L

70V3319/99
BF208(6)
BFG208(6)

208-Pin
fpBGA
Top View(7)

5623 drw 02c

NOTES:
1. A_{17} is a NC for IDT70V3399.
2. All V_{DD} pins must be connected to 3.3V power supply.
3. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
4. All V_{SS} pins must be connected to ground supply.
5. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3,4,5] (con't.)

70V3319/99
BC256[6]
BCG256[6]

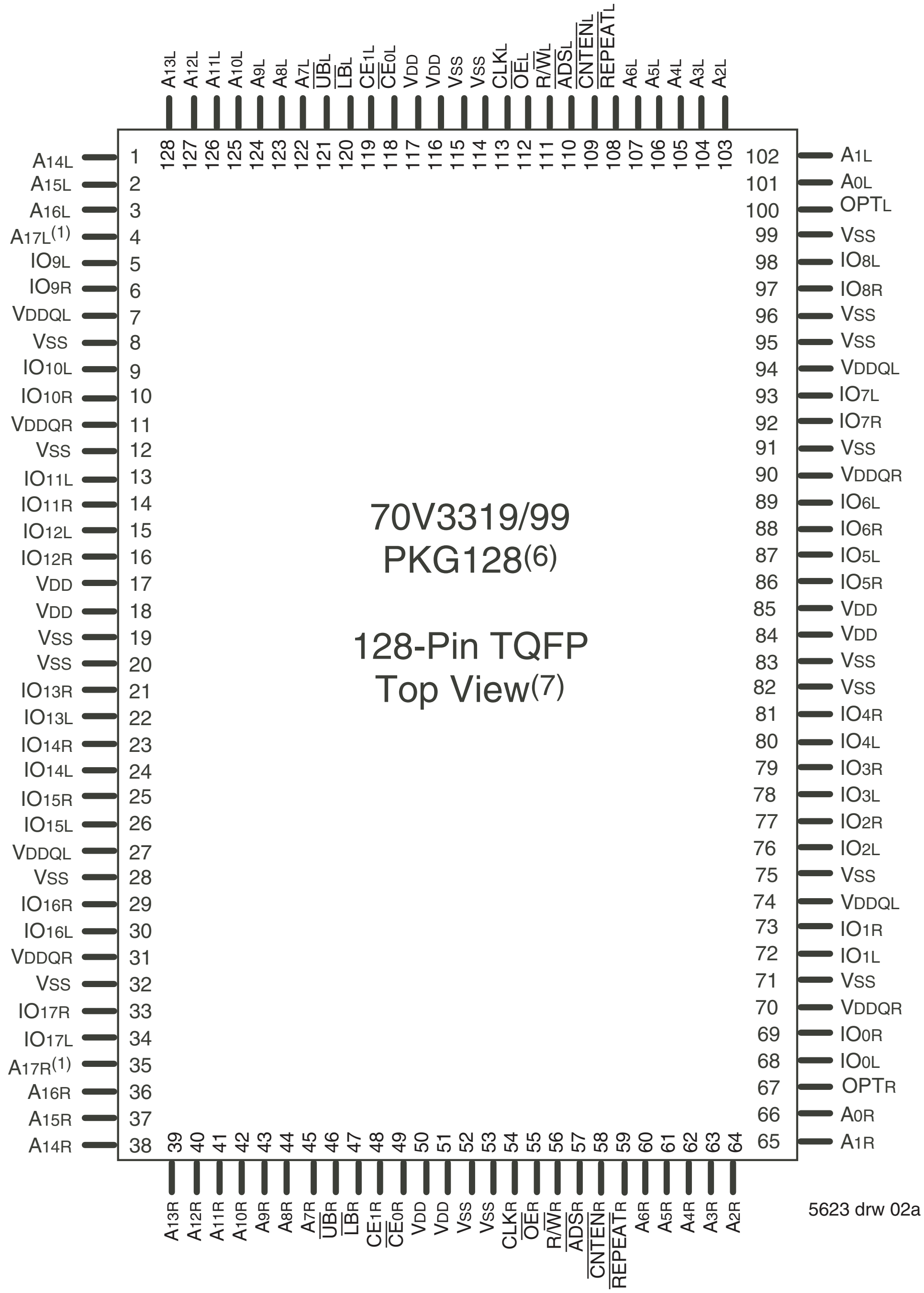
256-Pin BGA
Top View[7]

A1 NC	A2 TDI	A3 NC	A4 A17L(1)	A5 A14L	A6 A11L	A7 A8L	A8 NC	A9 CE1L	A10 $\overline{OE}$L	A11 $\overline{CNTEN}$L	A12 A5L	A13 A2L	A14 A0L	A15 NC	A16 NC
B1 NC	B2 NC	B3 TDO	B4 NC	B5 A15L	B6 A12L	B7 A9L	B8 $\overline{UB}$L	B9 $\overline{CE}$0L	B10 R/$\overline{W}$L	B11 $\overline{REPEAT}$L	B12 A4L	B13 A1L	B14 VDD	B15 NC	B16 NC
C1 NC	C2 I/O9L	C3 VSS	C4 A16L	C5 A13L	C6 A10L	C7 A7L	C8 NC	C9 $\overline{LB}$L	C10 CLKL	C11 $\overline{ADS}$L	C12 A6L	C13 A3L	C14 OPTL	C15 NC	C16 I/O8L
D1 NC	D2 I/O9R	D3 NC	D4 PIPE/$\overline{FT}$L	D5 VDDQL	D6 VDDQL	D7 VDDQR	D8 VDDQR	D9 VDDQL	D10 VDDQL	D11 VDDQR	D12 VDDQR	D13 VDD	D14 NC	D15 NC	D16 I/O8R
E1 I/O10R	E2 I/O10L	E3 NC	E4 VDDQL	E5 VDD	E6 VDD	E7 VSS	E8 VSS	E9 VSS	E10 VSS	E11 VDD	E12 VDD	E13 VDDQR	E14 NC	E15 I/O7L	E16 I/O7R
F1 I/O11L	F2 NC	F3 I/O11R	F4 VDDQL	F5 VDD	F6 VSS	F7 VSS	F8 VSS	F9 VSS	F10 VSS	F11 VSS	F12 VDD	F13 VDDQR	F14 I/O6R	F15 NC	F16 I/O6L
G1 NC	G2 NC	G3 I/O12L	G4 VDDQR	G5 VSS	G6 VSS	G7 VSS	G8 VSS	G9 VSS	G10 VSS	G11 VSS	G12 VSS	G13 VDDQL	G14 I/O5L	G15 NC	G16 NC
H1 NC	H2 I/O12R	H3 NC	H4 VDDQR	H5 VSS	H6 VSS	H7 VSS	H8 VSS	H9 VSS	H10 VSS	H11 VSS	H12 VSS	H13 VDDQL	H14 NC	H15 NC	H16 I/O5R
J1 I/O13L	J2 I/O14R	J3 I/O13R	J4 VDDQL	J5 VSS	J6 VSS	J7 VSS	J8 VSS	J9 VSS	J10 VSS	J11 VSS	J12 VSS	J13 VDDQR	J14 I/O4R	J15 I/O3R	J16 I/O4L
K1 NC	K2 NC	K3 I/O14L	K4 VDDQL	K5 VSS	K6 VSS	K7 VSS	K8 VSS	K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VDDQR	K14 NC	K15 NC	K16 I/O3L
L1 I/O15L	L2 NC	L3 I/O15R	L4 VDDQR	L5 VDD	L6 VSS	L7 VSS	L8 VSS	L9 VSS	L10 VSS	L11 VSS	L12 VDD	L13 VDDQL	L14 I/O2L	L15 NC	L16 I/O2R
M1 I/O16R	M2 I/O16L	M3 NC	M4 VDDQR	M5 VDD	M6 VDD	M7 VSS	M8 VSS	M9 VSS	M10 VSS	M11 VDD	M12 VDD	M13 VDDQL	M14 I/O1R	M15 I/O1L	M16 NC
N1 NC	N2 I/O17R	N3 NC	N4 PIPE/$\overline{FT}$R	N5 VDDQR	N6 VDDQR	N7 VDDQL	N8 VDDQL	N9 VDDQR	N10 VDDQR	N11 VDDQL	N12 VDDQL	N13 VDD	N14 NC	N15 I/O0R	N16 NC
P1 NC	P2 I/O17L	P3 TMS	P4 A16R	P5 A13R	P6 A10R	P7 A7R	P8 NC	P9 $\overline{LB}$R	P10 CLKR	P11 $\overline{ADS}$R	P12 A6R	P13 A3R	P14 NC	P15 NC	P16 I/O0L
R1 NC	R2 NC	R3 $\overline{TRST}$	R4 NC	R5 A15R	R6 A12R	R7 A9R	R8 $\overline{UB}$R	R9 $\overline{CE}$0R	R10 R/$\overline{W}$R	R11 $\overline{REPEAT}$R	R12 A4R	R13 A1R	R14 OPTR	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 A17R(1)	T5 A14R	T6 A11R	T7 A8R	T8 NC	T9 CE1R	T10 $\overline{OE}$R	T11 $\overline{CNTEN}$R	T12 A5R	T13 A2R	T14 A0R	T15 NC	T16 NC

5623 drw 02d

NOTES:
1. A_{17} is a NC for IDT70V3399.
2. All V_{DD} pins must be connected to 3.3V power supply.
3. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
4. All V_{SS} pins must be connected to ground supply.
5. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3,4,5,8,9] (con't.)



NOTES:
1. A17 is a NC for IDT70V3399.
2. All VDD pins must be connected to 3.3V power supply.
3. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
4. All Vss pins must be connected to ground supply.
5. Package body is approximately 14mm x 20mm x 1.4mm.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.
8. PIPE/FT option in PKG128 is not supported due to limitation in pin count. Device is pipelined outputs only on each port.
9. Due to the limited pin count, JTAG is not supported in the PKG128 package.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables(6)
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{17L}(1)	A_{0R} - A_{17R}(1)	Address
I/O_{0L} - I/O_{17L}	I/O_{0R} - I/O_{17R}	Data Input/Output
CLK_L	CLK_R	Clock
$PIPE/\overline{FT}_L$(5)	$PIPE/\overline{FT}_R$(5)	Pipeline/Flow-Through
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{REPEAT}_L$	$\overline{REPEAT}_R$	Counter Repeat(4)
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Enable (I/O_9-I/O_{17})(6)
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Enable (I/O_0-I/O_8)(6)
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V)(2)
OPT_L	OPT_R	Option for selecting V_{DDQX}(2,3)
V_{DD}		Power (3.3V)(2)
V_{SS}		Ground (0V)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz)
TMS		Test Mode Select
$\overline{TRST}$		Reset (Initialize TAP Controller)

5623 tbl 01

NOTES:
1. A_{17} is a NC for IDT70V3399.
2. V_{DD}, OPT_X, and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
3. OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to VIL (0V), then that port's I/Os and address controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
4. When $\overline{REPEAT}_X$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}_X$.
5. $PIPE/\overline{FT}$ option in PK-128 package is not supported due to limitation in pin count. Device is pipelined output mode only on each port.
6. Chip Enables and Byte Enables are double buffered when $PL/\overline{FT} = V_{IH}$, i.e., the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control(1,2,3)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	$R/\overline{W}$	Upper Byte I/O_{9-17}	Lower Byte I/O_{0-8}	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	H	L	L	High-Z	D_{IN}	Write to Lower Byte Only
X	↑	L	H	L	H	L	D_{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	D_{IN}	D_{IN}	Write to Both Bytes
L	↑	L	H	H	L	H	High-Z	D_{OUT}	Read Lower Byte Only
L	↑	L	H	L	H	H	D_{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	D_{OUT}	D_{OUT}	Read Both Bytes
H	↑	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

5623 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter Control(1,2)

External Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{REPEAT}$(6)	I/O(3)	MODE
X	X	An	↑	X	X	L(4)	$D_{I/O}(0)$	Counter Reset to last valid $\overline{ADS}$ load
An	X	An	↑	L(4)	X	H	$D_{I/O}$ (n)	External Address Used
An	Ap	Ap	↑	H	H	H	$D_{I/O}(p)$	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L(5)	H	$D_{I/O}(p+1)$	Counter Enabled—Internal Address generation

5623 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of $R/\overline{W}$, $\overline{CE}_0$, CE_1, $\overline{UB}$, $\overline{LB}$ and $\overline{OE}$.
3. Outputs configured in flow-through output mode: if outputs are in pipelined mode the date out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{REPEAT}$ are independent of all other memory control signals including $\overline{CE}_0$, CE_1 and $\overline{UB}$, $\overline{LB}$.
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE_1, $\overline{UB}$, $\overline{LB}$.
6. When $\overline{REPEAT}$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}$. This value is not set at power-up: a known location should be loaded via $\overline{ADS}$ during initialization if desired. Any subsequent $\overline{ADS}$ access during operations will update the $\overline{REPEAT}$ address location.

Recommended Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0^oC to $+70^oC$	0V	3.3V ± 150mV
Industrial	-40^oC to $+85^oC$	0V	3.3V ± 150mV

5623 tbl 04

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}(3)	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}	DC Output Current	50	mA

5623 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 150mV.
3. Ambient Temperature Under Bias. No AC Conditions. Chip Deselected.

Recommended DC Operating Conditions with VDDQ at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage(3)	2.4	2.5	2.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Address & Control Inputs)	1.7	—	V_{DDQ} + 100mV(2)	V
V_{IH}	Input High Voltage - I/O(3)	1.7	—	V_{DDQ} + 100mV(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.7	V

5623 tbl 05a

NOTES:
1. Undershoot of $V_{IL} \geq$ -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 100mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with VDDQ at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage(3)	3.15	3.3	3.45	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Address & Control Inputs)(3)	2.0	—	V_{DDQ} + 150mV(2)	V
V_{IH}	Input High Voltage - I/O(3)	2.0	—	V_{DDQ} + 150mV(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

5623 tbl 05b

NOTES:
1. Undershoot of $V_{IL} \geq$ -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance[1] (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 3dV	10.5	pF

5623 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V3319/99S Min.	70V3319/99S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[1]	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\|I_{LO}\|$	Output Leakage Currentt[1]	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage[2]	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage[2]	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage[2]	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage[2]	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

5623 tbl 08

NOTE:
1. At $V_{DD} \leq$ 2.0V leakages are undefined.
2. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[3] (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Condition	Version		70V3319/99S166 Com'l Only		70V3319/99S133 Com'l & Ind		Unit
					Typ.[4]	Max.	Typ.[4]	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	370	500	320	400	mA
			IND	S	—	—	320	480	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	125	200	115	160	mA
			IND	S	—	—	115	195	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[1]	COM'L	S	250	350	220	290	mA
			IND	S	—	—	220	350	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports Outputs Disabled $\overline{CE}_L$ and $\overline{CE}_R$ $\geq$ V_{DDQ} - 0.2V, $V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[2]	COM'L	S	15	30	15	30	mA
			IND	S	—	—	15	40	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{DDQ}$ - 0.2V[5] $V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	250	350	220	290	mA
			IND	S	—	—	220	350	

5623 tbl 09

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{DD\ DC}$(f=0) = 120mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X \leq$ 0.2V means $\overline{CE}_{0X} \leq$ 0.2V and $CE_{1X} \geq V_{DDQ}$ - 0.2V
   $\overline{CE}_X \geq V_{DDQ}$ - 0.2V means $\overline{CE}_{0X} \geq V_{DDQ}$ - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.

AC Test Conditions (V_{DDQ} - 3.3V/2.5V)

Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

5623 tbl 10

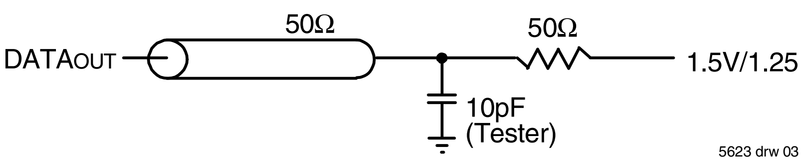


Figure 1. AC Output Test load.

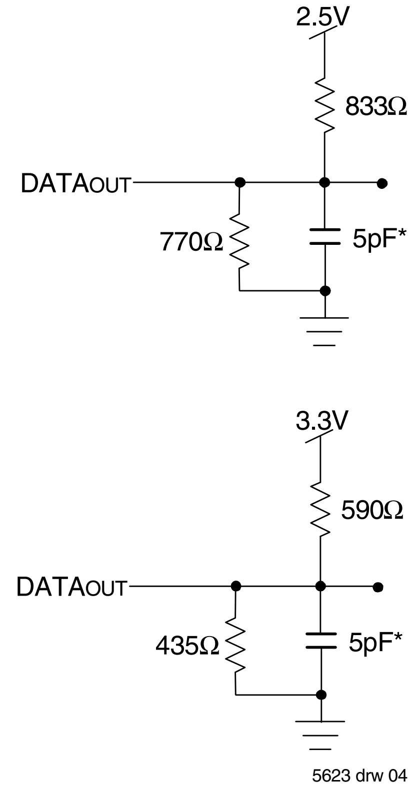


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

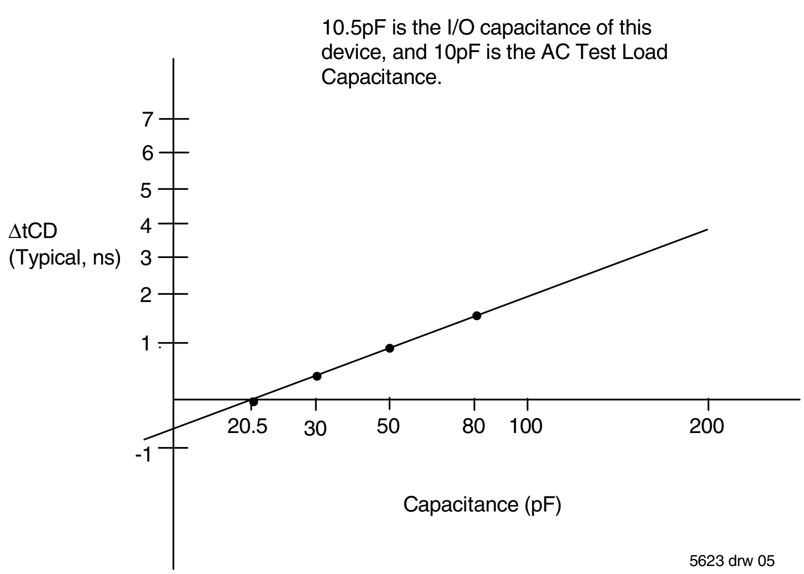


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)(2,3) (V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

		70V3319/99S166 Com'l Only		70V3319/99S133 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CYC1}	Clock Cycle Time (Flow-Through)(1)	20	——	25	——	ns
t_{CYC2}	Clock Cycle Time (Pipelined)(1)	6	——	7.5	——	ns
t_{CH1}	Clock High Time (Flow-Through)(1)	6	——	7	——	ns
t_{CL1}	Clock Low Time (Flow-Through)(1)	6	——	7	——	ns
t_{CH2}	Clock High Time (Pipelined)(2)	2.1	——	2.6	——	ns
t_{CL2}	Clock Low Time (Pipelined)(1)	2.1	——	2.6	——	ns
t_{SA}	Address Setup Time	1.7	——	1.8	——	ns
t_{HA}	Address Hold Time	0.5	——	0.5	——	ns
t_{SC}	Chip Enable Setup Time	1.7	——	1.8	——	ns
t_{HC}	Chip Enable Hold Time	0.5	——	0.5	——	ns
t_{SB}	Byte Enable Setup Time	1.7	——	1.8	——	ns
t_{HB}	Byte Enable Hold Time	0.5	——	0.5	——	ns
t_{SW}	R/W Setup Time	1.7	——	1.8	——	ns
t_{HW}	R/W Hold Time	0.5	——	0.5	——	ns
t_{SD}	Input Data Setup Time	1.7	——	1.8	——	ns
t_{HD}	Input Data Hold Time	0.5	——	0.5	——	ns
t_{SAD}	$\overline{ADS}$ Setup Time	1.7	——	1.8	——	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.5	——	0.5	——	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	1.7	——	1.8	——	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.5	——	0.5	——	ns
t_{SRPT}	$\overline{REPEAT}$ Setup Time	1.7	——	1.8	——	ns
t_{HRPT}	$\overline{REPEAT}$ Hold Time	0.5	——	0.5	——	ns
t_{OE}	Output Enable to Data Valid	——	4.0	——	4.2	ns
t_{OLZ}	Output Enable to Output Low-Z	1	——	1	——	ns
t_{OHZ}	Output Enable to Output High-Z	1	3.6	1	4.2	ns
t_{CD1}	Clock to Data Valid (Flow-Through)(1)	——	12	——	15	ns
t_{CD2}	Clock to Data Valid (Pipelined)(1)	——	3.6	——	4.2	ns
t_{DC}	Data Output Hold After Clock High	1	——	1	——	ns
t_{CKHZ}	Clock High to Output High-Z	1	3	1	3	ns
t_{CKLZ}	Clock High to Output Low-Z	1	——	1	——	ns
Port-to-Port Delay						
t_{CO}	Clock-to-Clock Offset	5	——	6	——	ns

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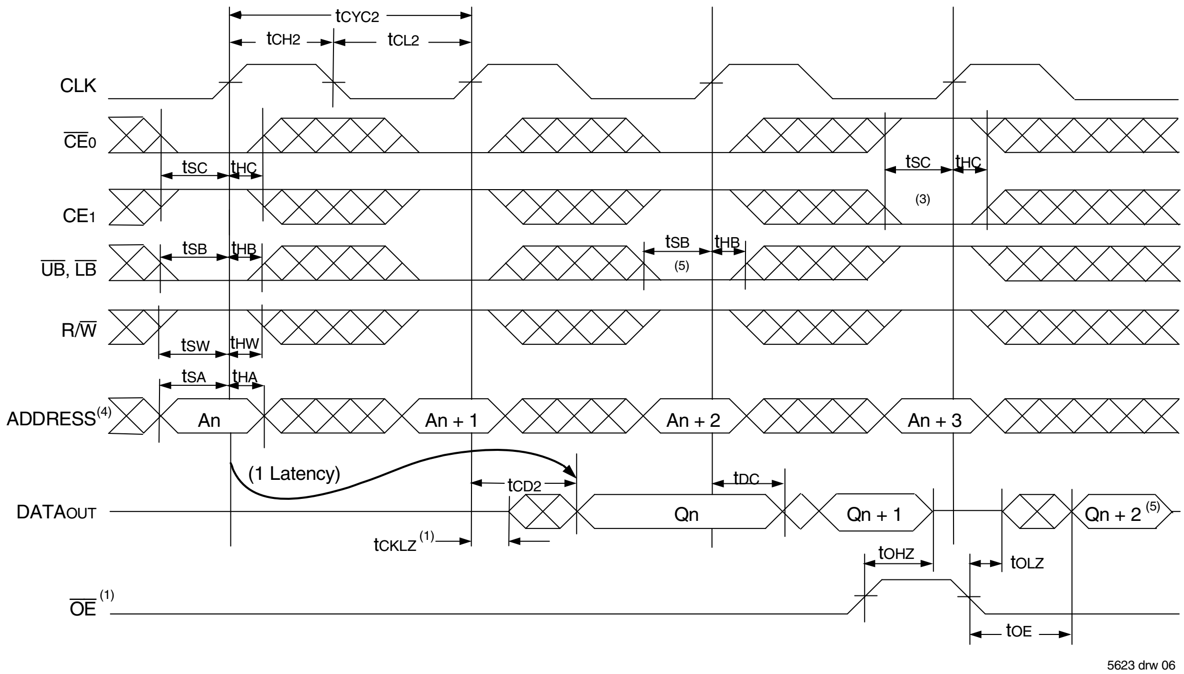
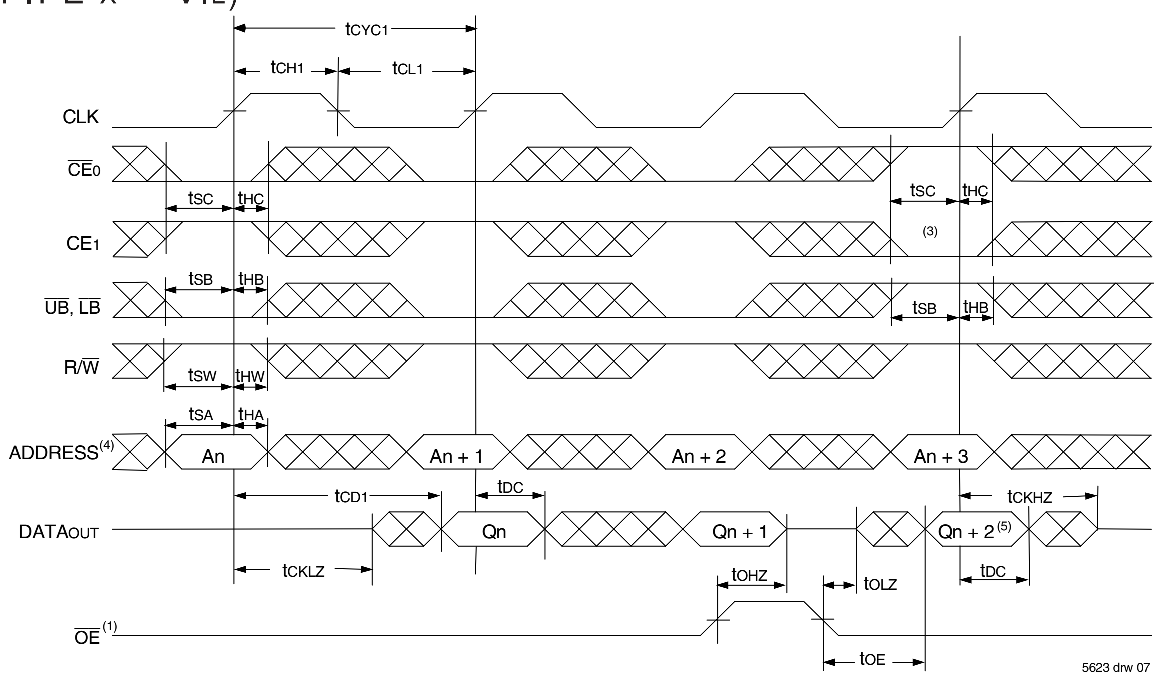
NOTES:
1. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}$/PIPEx = V_{IH}. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{IL} for that port.
2. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}$/PIPE. $\overline{FT}$/PIPE should be treated as a DC signal, i.e. steady state during operation.
3. These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 5 for details on selecting the desired operating voltage levels for each port.

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE'X' = V_{IH})(2)

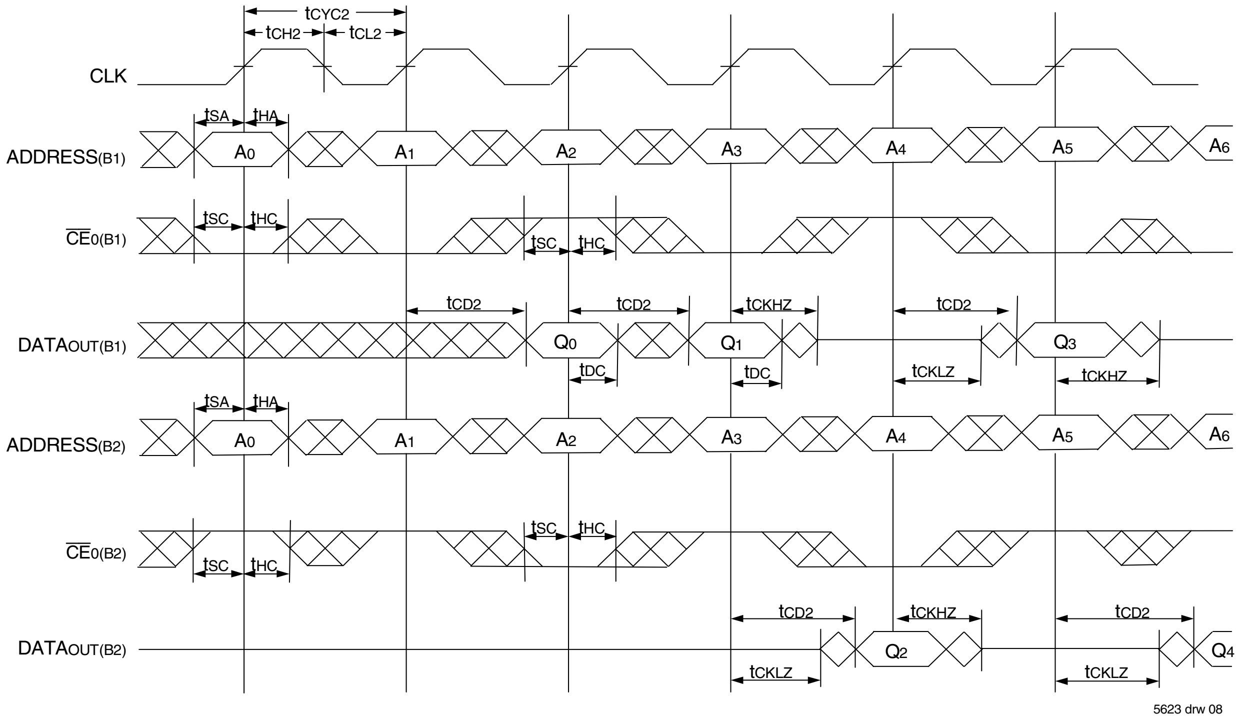


Timing Waveform of Read Cycle for Flow-through Output ($\overline{FT}$/PIPE"X" = V_{IL})(2,6)

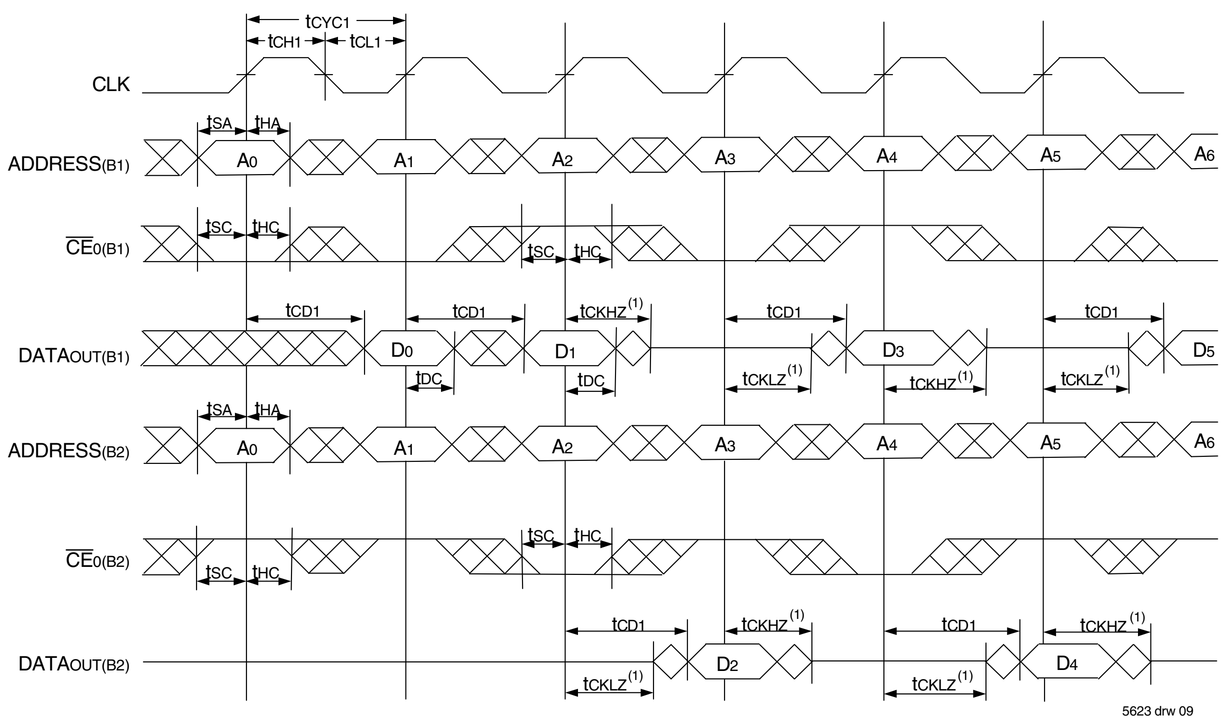


NOTES:
1. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{REPEAT}$ = V_{IH}.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH}, CE_1 = V_{IL}, $\overline{UB}$, $\overline{LB}$ = V_{IH} following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{UB}$, $\overline{LB}$ was HIGH, then the appropriate Byte of DATAOUT for Qn + 2 would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read(1,2)

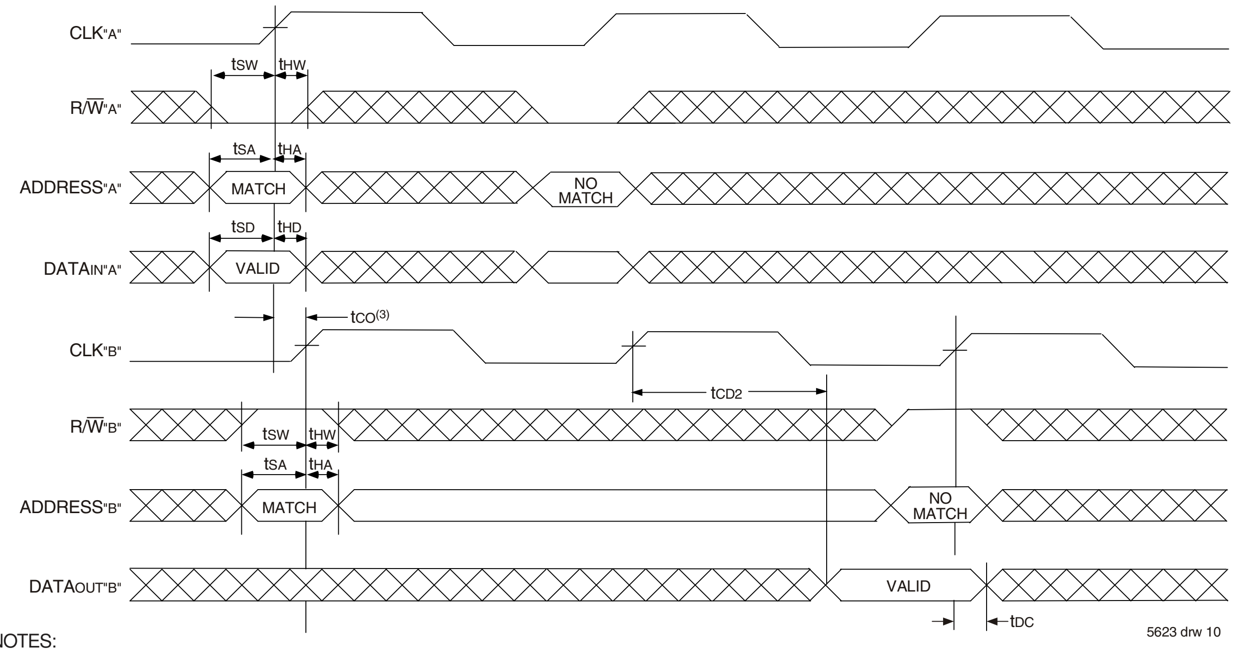


Timing Waveform of a Multi-Device Flow-Through Read(1,2)



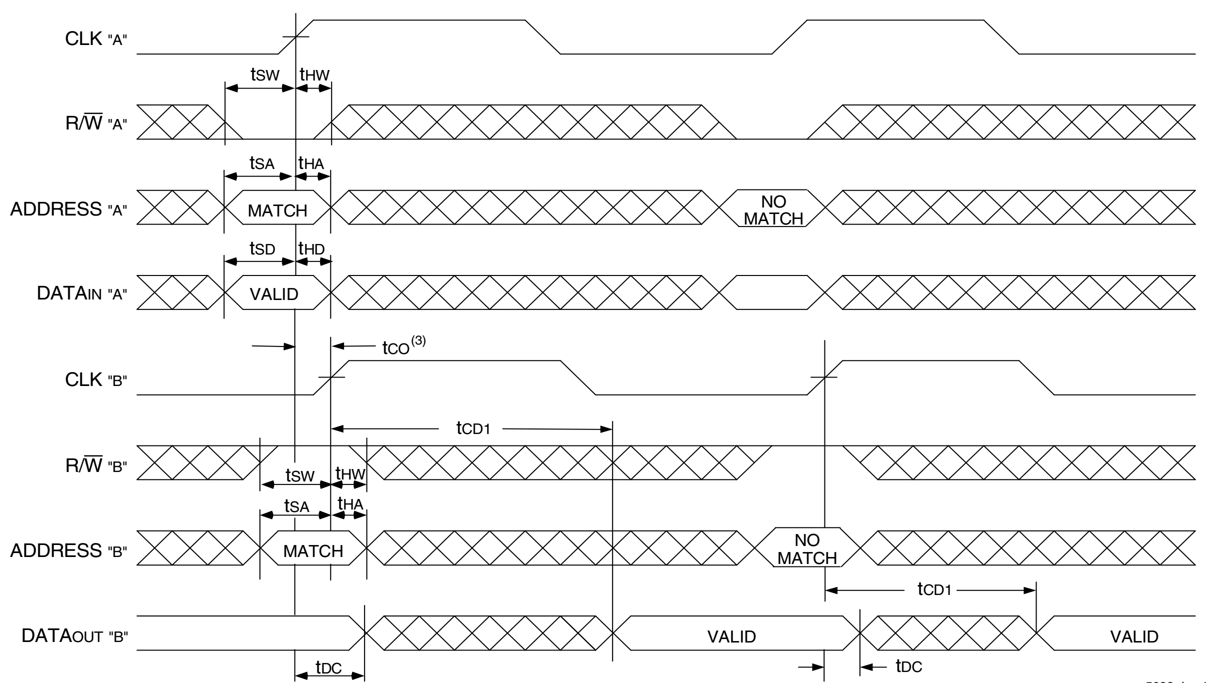
NOTES:
1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3319/99 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS}$ = VIL; CE1(B1), CE1(B2), R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.

Timing Waveform of Left Port Write to Pipelined Right Port Read(1,2,4)



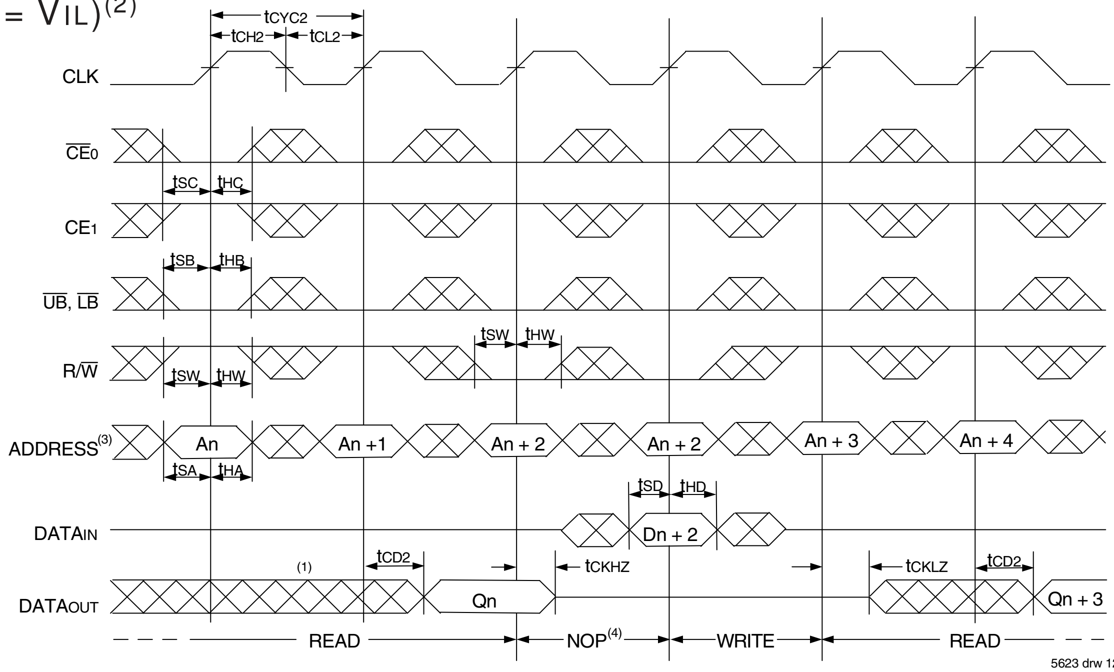
NOTES:
1. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for Port "B", which is being read from. $\overline{OE}$ = V_{IH} for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2\ t_{CYC2} + t_{CD2}$). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

Timing Waveform with Port-to-Port Flow-Through Read(1,2,4)



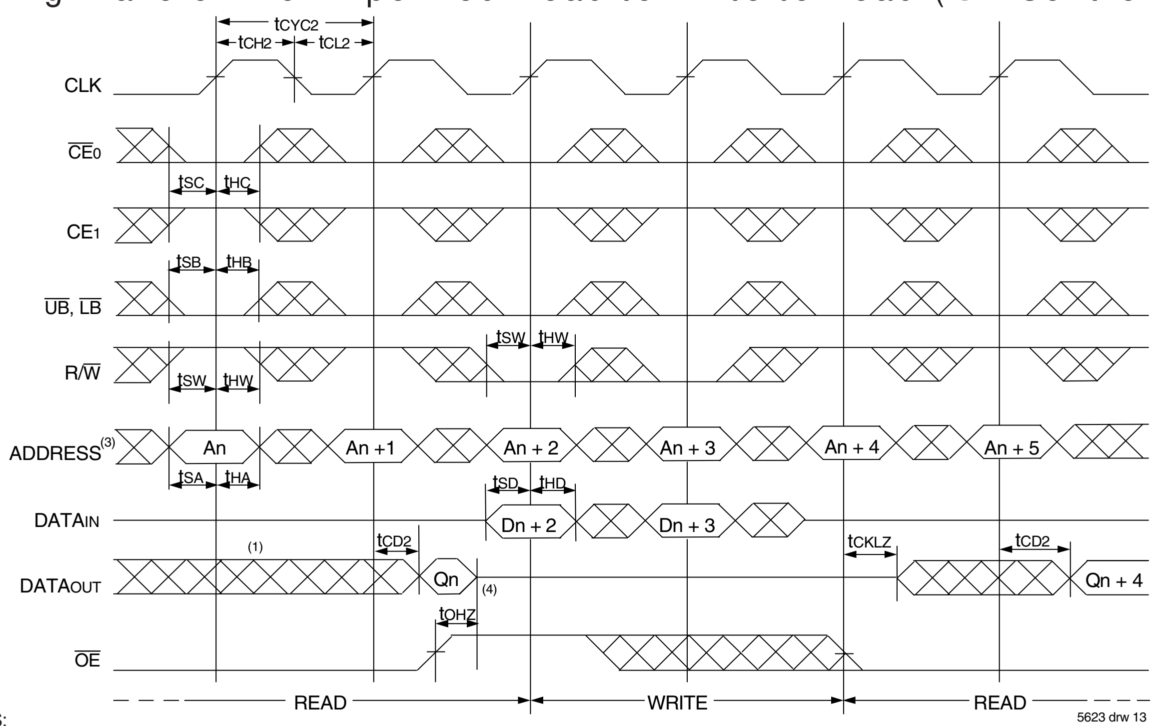
NOTES:
1. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD1}$). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CD1}$).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{\textbf{OE}}$ = VIL)(2)



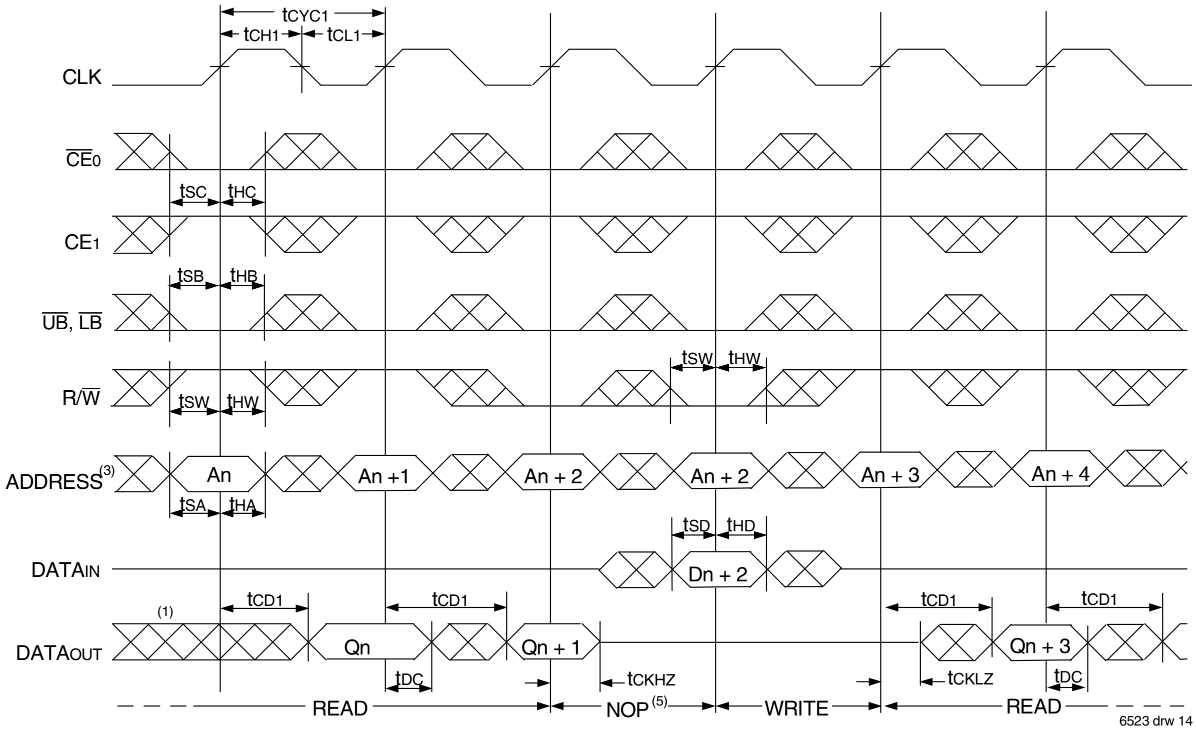
NOTES:
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}$0, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{\textbf{OE}}$ Controlled)(2)

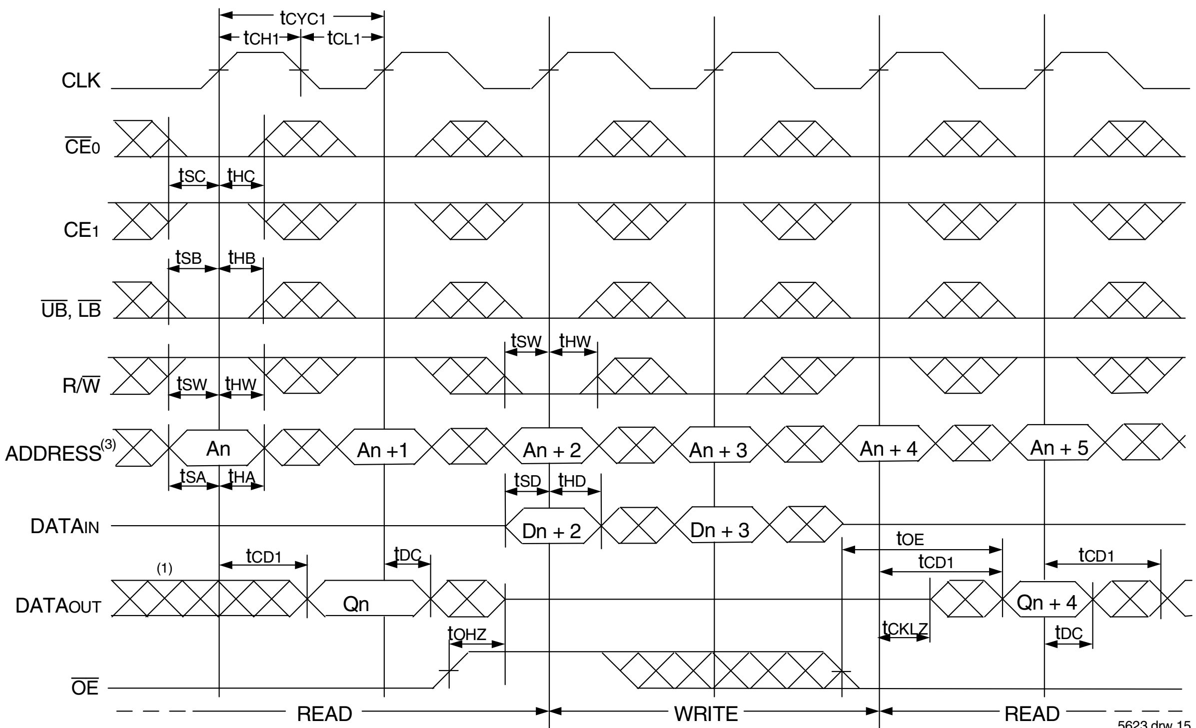


NOTES:
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}$0, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = VIL)(2)

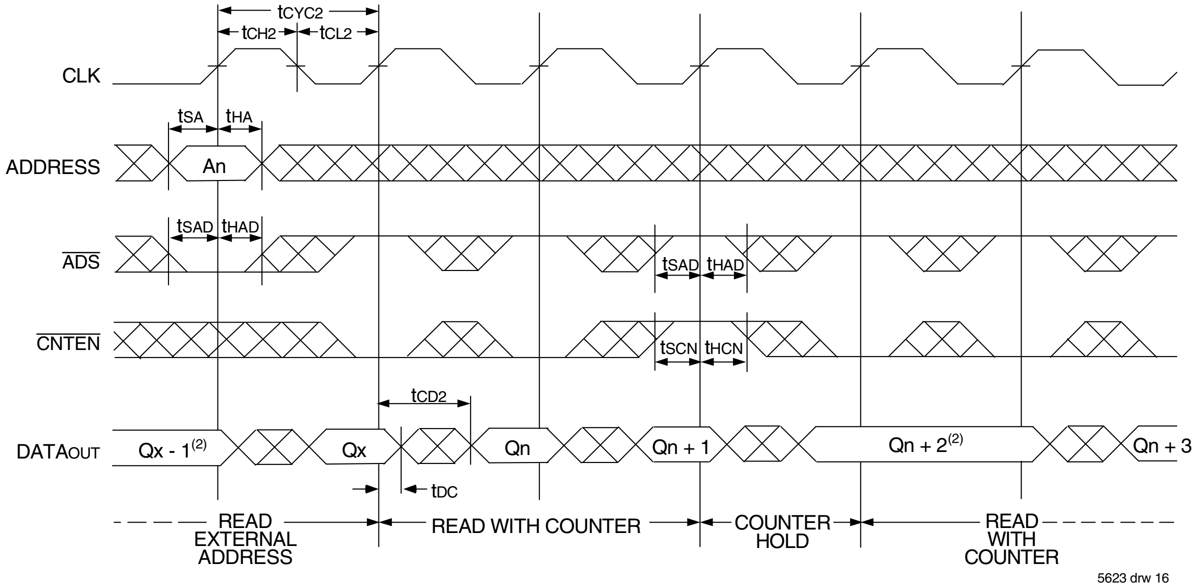


Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)

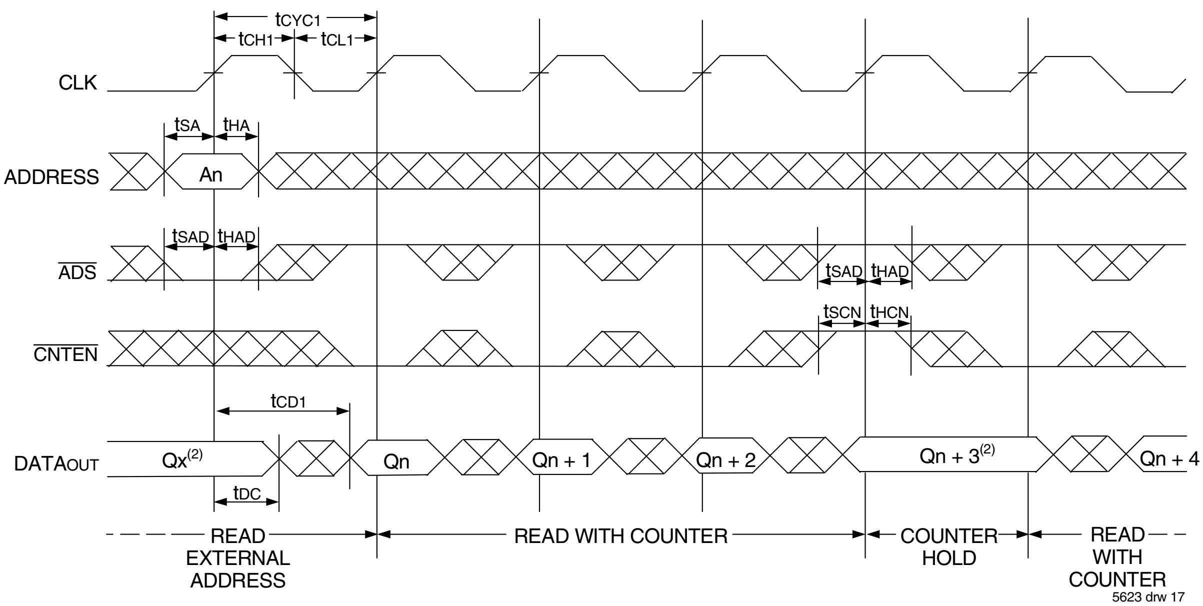


NOTES:
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance(1)

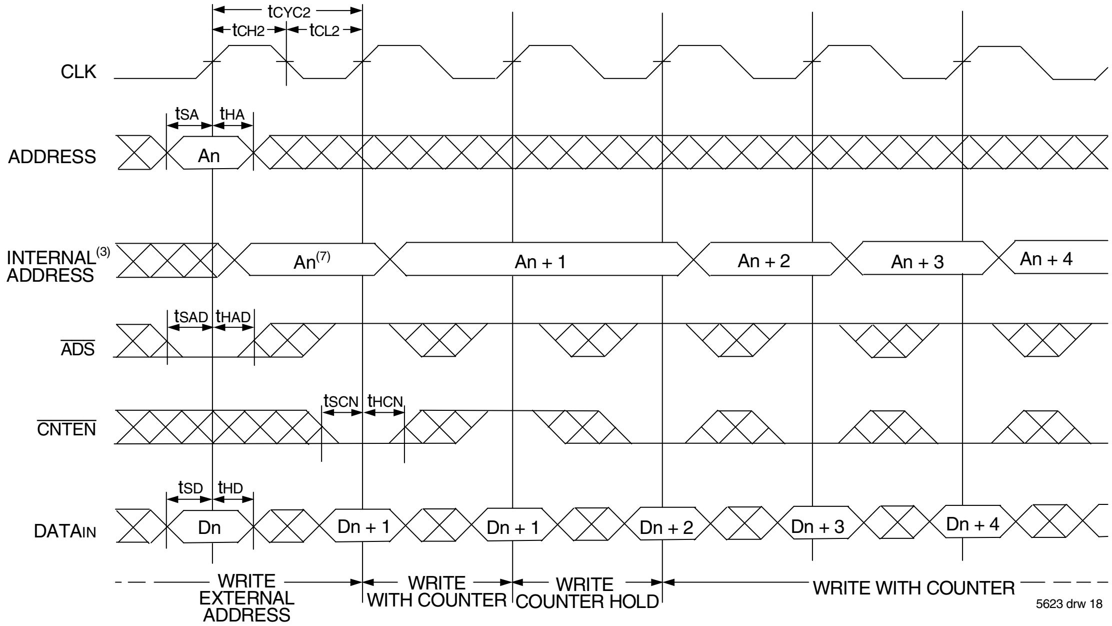


Timing Waveform of Flow-Through Read with Address Counter Advance(1)

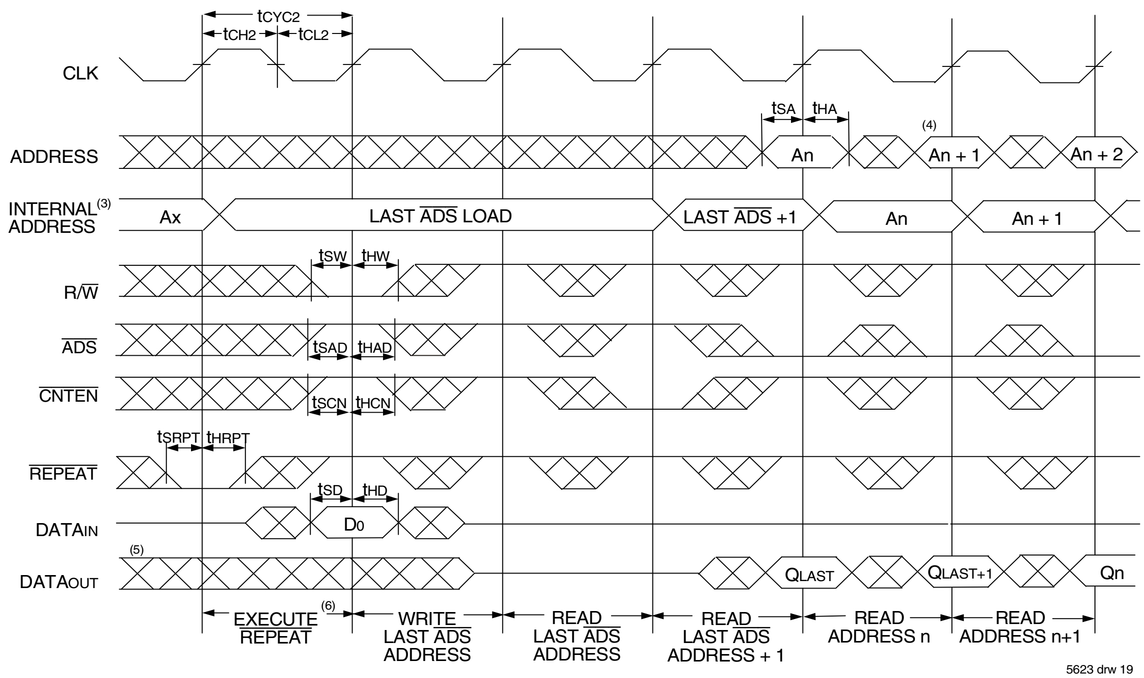


NOTES:
1. $\overline{CE_0}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ = VIL; CE1, R/$\overline{W}$, and $\overline{REPEAT}$ = VIH.
2. If there is no address change via $\overline{ADS}$ = VIL (loading a new address) or $\overline{CNTEN}$ = VIL (advancing the address), i.e. $\overline{ADS}$ = VIH and $\overline{CNTEN}$ = VIH, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)[1]



Timing Waveform of Counter Repeat[2]



NOTES:
1. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = VIL; CE1 and $\overline{REPEAT}$ = VIH.
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$ = VIL; CE1 = VIH.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = VIL and equals the counter output when $\overline{ADS}$ = VIH.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during $\overline{REPEAT}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{REPEAT}$ cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed. Extra cycles are shown here simply for clarification. For more information on $\overline{REPEAT}$ function refer to Truth Table II.
7. $\overline{CNTEN}$ = VIL advances Internal Address from ‘An’ to ‘An +1’. The transition shown indicates the time required for the counter to advance. The ‘An +1’Address is written to during this cycle.

Functional Description

The IDT70V3319/99 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3319/99s for depth expansion configurations. Two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to reactivate the outputs.

Depth and Width Expansion

The IDT70V3319/99 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3319/99 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.

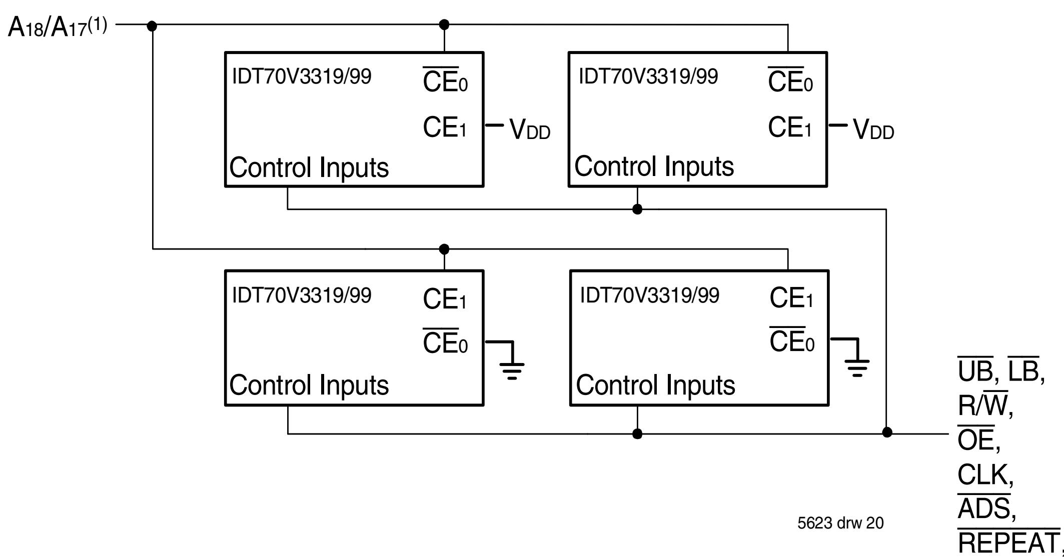


Figure 4. Depth and Width Expansion with IDT70V3319/99

NOTE:
1. A_{17} is for IDT70V3319, A_{16} is for IDT70V3399.

JTAG Timing Specifications

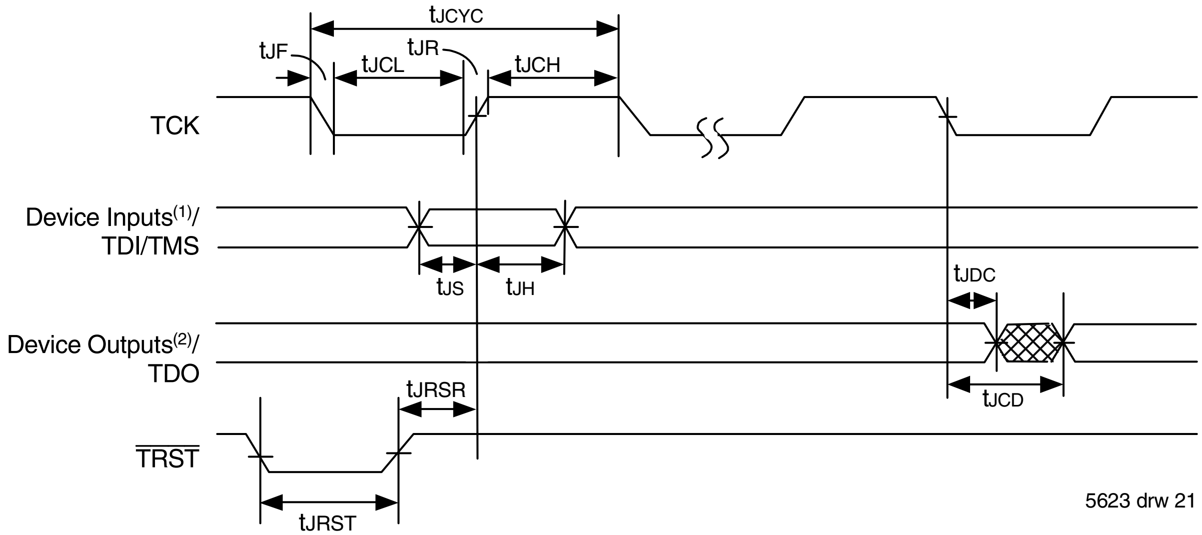


Figure 5. Standard JTAG Timing

NOTES:
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics(1,2,3,4)

Symbol	Parameter	70V3319/99		
		Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	3(1)	ns
t_{JF}	JTAG Clock Fall Time	—	3(1)	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	25	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	15	—	ns
t_{JH}	JTAG Hold	15	—	ns

5623 tbl 12

NOTES:
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x0314[(1)]	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5623 tbl 13

NOTE:
1. Device ID for IDT70V3399 is 0x0315.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5623 tbl 14

System Interface Parameters

Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs[(1)]. Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0011	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs[(2)] to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

5623 tbl 15

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information

XXXXX A 999 A A A A

- **XXXXX — Device Type**
  - 70V3319 — 4Mbit (256K x 18-Bit) Synchronous Dual-Port RAM
  - 70V3399 — 2Mbit (128K x 18-Bit) Synchronous Dual-Port RAM
- **A — Power**
  - S — Standard Power
- **999 — Speed** (Speed in Megahertz)
  - 166 — Commercial Only
  - 133 — Commercial & Industrial
- **A — Package**
  - BF — 208-pin fpBGA (BF208, BFG208)
  - PRF — 128-pin TQFP (PKG128)
  - BC — 256-pin BGA (BC256, BCG256)
- **A**
  - G[1] — Green
- **A — Process/Temperature Range**
  - Blank — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **A**
  - Blank — Tray
  - 8 — Tape and Reel

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NOTES:
1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.
   LEAD FINISH (SnPb) parts are Obsolete excluding BGA & fpBGA. Product Discontinuation Notice - PDN# SP-17-02
   Note that information regarding recently obsoleted parts is included in this datasheet for customer convenience.

Orderable Part Information

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
133	70V3319S133BC	BC256	CABGA	C
	70V3319S133BC8	BC256	CABGA	C
	70V3319S133BCGI	BCG256	CABGA	I
	70V3319S133BCI	BC256	CABGA	I
	70V3319S133BCI8	BC256	CABGA	I
	70V3319S133BF	BF208	CABGA	C
	70V3319S133BF8	BF208	CABGA	C
	70V3319S133BFI	BF208	CABGA	I
	70V3319S133BFI8	BF208	CABGA	I
	70V3319S133PRFGI	PKG128	TQFP	I
	70V3319S133PRFGI8	PKG128	TQFP	I
166	70V3319S166BC	BC256	CABGA	C
	70V3319S166BC8	BC256	CABGA	C
	70V3319S166BCG	BCG256	CABGA	C
	70V3319S166BF	BF208	CABGA	C
	70V3319S166BF8	BF208	CABGA	C
	70V3319S166BFG	BFG208	CABGA	C
	70V3319S166BFG8	BFG208	CABGA	C
	70V3319S166PRFG	PKG128	TQFP	C
	70V3319S166PRFG8	PKG128	TQFP	C

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
133	70V3399S133BC	BC256	CABGA	C
	70V3399S133BC8	BC256	CABGA	C
	70V3399S133BCI	BC256	CABGA	I
	70V3399S133BCI8	BC256	CABGA	I
	70V3399S133BF	BF208	CABGA	C
	70V3399S133BF8	BF208	CABGA	C
	70V3399S133BFI	BF208	CABGA	I
	70V3399S133BFI8	BF208	CABGA	I
166	70V3399S166BC	BC256	CABGA	C
	70V3399S166BC8	BC256	CABGA	C
	70V3399S166BF	BF208	CABGA	C
	70V3399S166BF8	BF208	CABGA	C
	70V3399S166BFG	BFG208	CABGA	C
	70V3399S166BFG8	BFG208	CABGA	C

Datasheet Document History:

06/02/00:	Initial Public Offering
07/12/00:	Page 1 Added mux to functional block diagram
06/20/01:	Page 1 Added JTAG information for TQFP package
	Page 4 Corrected TQFP package size
07/30/01:	Page 1 Added PL/$\overline{FT}$ option
	Page 20 Changed maximum value for JTAG AC Electrical Characteristics for t_{JCD} from 20ns to 25ns
	Page 9 Added Industrial Temperature DC Parameters
11/20/01:	Page 2, 3 & 4 Added date revision for pin configurations
	Page 11 Changed t_{OE} value in AC Electrical Characteristics, please refer to Errata #SMEN-01-05
	Page 1 & 22 Replaced TM logo with ® logo
	Page 10 Changed AC Test Conditions Input Rise/Fall Times
08/06/02:	Consolidated multiple devices into one datasheet
	Page 1 & 5 Added DCD capability for Pipelined Outputs
	Page 7 Clarified T_{BIAS} and added T_{JN}
	Page 9 Changed DC Electrical Parameters
	Page 11 Removed Clock Rise & Fall Time from AC Electrical Characteristics Table
	Removed Preliminary status
05/19/03:	Page 11 Added Byte Enable SetupTime & Byte Enable Hold Time to AC Electrical Characteristics Table
	Page 22 Added IDT Clock Solution Table
02/08/06:	Page 1 Added green availability to features
	Page 6 Changed footnote 2 for Truth Table I from $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = V_{IH} to $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = X
	Page 22 Added green indicator to ordering information
07/25/08:	Page 9 Corrected a typo in the DC Chars table
01/19/09:	Page 22 Removed "IDT" from orderable part number
10/03/14:	Page 22 Added Tape & Reel to the Ordering Information
06/20/18:	Product Discontinuation Notice - PDN# SP-17-02
	Last time buy expires June 15, 2018
09/12/19:	Page 2, 3 & 4 Updated package codes
	Page 22 Added Orderable Part Information table and removed IDT Clock Solution table
11/04/19:	Page 22 Corrected "ns" to "MHz" in the header of the Orderable Part Information tables

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