Synchronous Boost µModule Regulator with Input-Output Short Protection

FEATURES

- **Complete Boost Switch Mode Power Supply**
- **Wide Input Voltage Range: 4.5V to 28V**
- **Output Voltage Range: 6V to 36V**
- **4A Continuous Output Current ($12V_{IN}$, $24V_{OUT}$)**
- **±2% Maximum Total Output Voltage Regulation Over Load, Line and Temperature**
- Input Disconnect in Shutdown
- Inrush Current Limit
- External Frequency Synchronization
- Programmable Frequency (350kHz to 780kHz)
- Parallel Current Sharing
- Up to 98% Efficiency
- Selectable Burst Mode® Operation
- In-Line Overcurrent Protection
- Overtemperature Protection
- LTM4656-1 Adjustable Compensation Version
- 16mm × 16mm × 7.07mm BGA Package

APPLICATIONS

- Telecom and Networking Equipment
- Electronic Test Equipment

DESCRIPTION

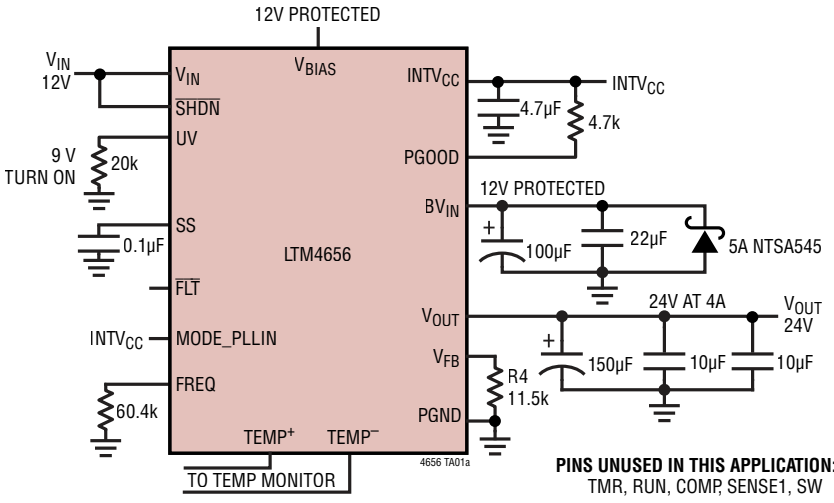
The LTM®4656 is a complete high efficiency boost µModule® (power module) regulator with the switching controller, power FETs, inductor, and all supporting components. Only a few input and output capacitors are needed. Operating over an input voltage range of 4.5V to 28V, the LTM4656 supports an output voltage range of 6V to 36V, set by a single external resistor. Its high efficiency design delivers up to 5A continuous output current. An in-line protection circuit sets the maximum input current, and will trip off the input power if exceeded and retry (see Typical Applications section).

The high density boost design can convert up to 180W of output power.

Fault protection features include overtemperature protection, and overcurrent protection input referred with auto-retry. The µmodule is offered in a space saving and thermally enhanced 16mm × 16mm × 7.07mm BGA package. The LTM4656 is Pb-free and RoHS compliant.

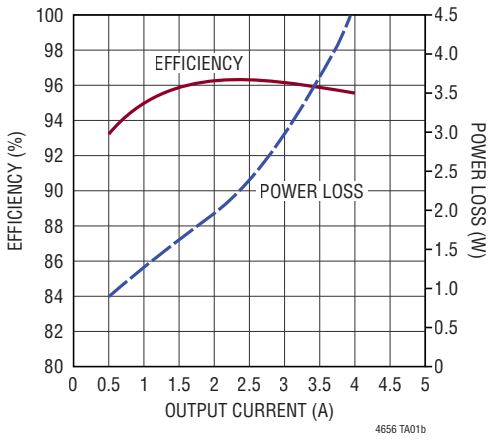
TYPICAL APPLICATION

$12V_{IN}$, $24V_{OUT}$ at 4A



PINS UNUSED IN THIS APPLICATION:
TMR, RUN, COMP, SENSE1, SW

24V Output Efficiency at 550kHz



ABSOLUTE MAXIMUM RATINGS

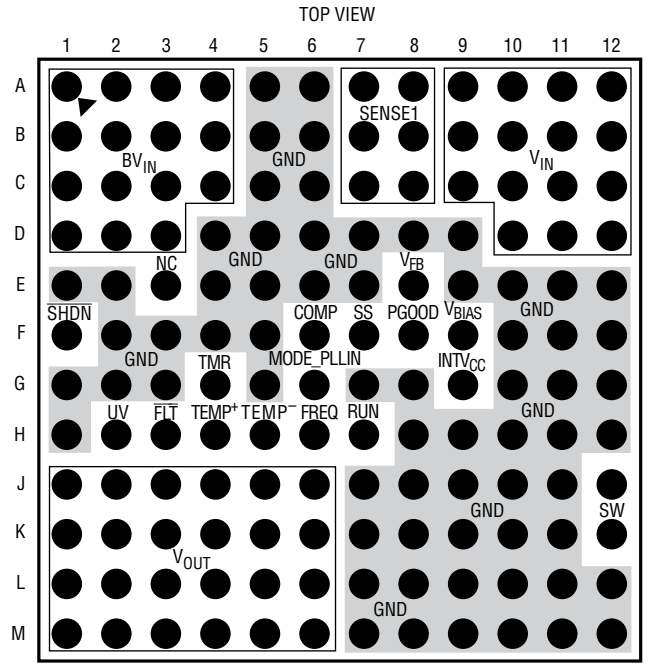
(Note 1)

V_{IN}, SENSE1, BV_{IN}, SW, V_{OUT},
$\overline{SHDN}$, UV, $\overline{FLT}$, V_{BIAS} ..... –0.3V to 36V
$INTV_{CC}$, MODE_PLLIN, PGOOD ..... –0.3V to 6V
FREQ, SS, COMP, V_{FB} ..... –0.3V to $INTV_{CC}$
RUN ..... –0.3V to 5V
TMR 0.5mA
$TEMP^+$, $TEMP^-$ ..... <0.7V Across Pins, No More than 5mA (Current Source)
Operating Junction Temperature (Note 2) .. –40 to 125°C
Storage Temperature Range ..... –55 to 125°C
Peak Solder Reflow Body Temperature ..... 245°C

Note: Not recommended for upside-down reflow.

PIN CONFIGURATION

(See Capacitor Matrix, Pin Configuration Table)



BGA PACKAGE
144-LEAD (16mm × 16mm × 7.07mm)
T_{JMAX} = 125°C, θ_{JA} = 11.8°C/W,
θ_{JCtop} = 7.1°C/W, θ_{JCbot} = 4.4°C/W (Note 7)
WEIGHT = 4.22g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4656EY#PBF	SAC305 (RoHS)	LTM4656Y	e1	BGA	4	–40°C to 125°C
LTM4656IY#PBF	SAC305 (RoHS)		e1			–40°C to 125°C
LTM4656IY	SnPb (63/37)		e0			–40°C to 125°C
LTM4656EY-1#PBF	SAC305 (RoHS)		e1			–40°C to 125°C
LTM4656IY-1#PBF	SAC305 (RoHS)		e1			–40°C to 125°C
LTM4656IY-1	SnPb (63/37)		e0			–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2), V_{IN} = 12, V_{BIAS} = BV_{IN}, $\overline{SHDN}$ = V_{IN} per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input/Output Section							
V_{IN}	Input DC Voltage	Note 4	●	4.5		28	V
$V_{OUT(RANGE)}$	Output Voltage Range	Note 4, V_{IN} = 5V for 6V output	●	6		36	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	R_{FB} = 11.5k, MODE_PLLIN = $INTV_{CC}$ V_{IN} = 12V, I_{OUT} = 0A to 4A	●	23.52	24	24.48	V
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 24V, MODE_PLLIN = $INTV_{CC}$ V_{IN} = 12V, V_{OUT} = 24V, MODE/PLLIN = GND Shutdown, $\overline{SDHN}$ = 0, V_{IN} = 12V			1.7 76 230		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 4A			8		A
$I_{INRUSH(VIN)}$	Input Inrush Current at Startup	C_{IN} = 10µF × 2, 150µF; C_{OUT} = 10µF × 2 Ceramic, 150µF V_{IN} = 12V, V_{OUT} = 24V, TRACK/SS = 0.1µF			0.5		A
$I_{OUT(DC)}$	Output Continuous Current Range Note 4	V_{IN} = 5V, V_{OUT} = 12V (Note 4) V_{IN} =12V, V_{OUT} = 24V		0 0		3.5 4	A A
I_{IN} Limit Range	Input Current Limit	See Typical Applications Based on Internal 0.004 R_{SENSE} and 50mV Trip Typical		10.6	12.5	14	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 24V, V_{IN} = 5 to 12V, I_{OUT} = 0A	●		0.1	0.2	%/V
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 0A to 4.0A	●		0.3	0.6	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 10µF Ceramic × 2, 150µF Aluminum, V_{IN} = 12V, V_{OUT} = 24V			200		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 10µF Ceramic × 2, 150µF Aluminum, SS = 0.1µF, V_{IN} = 12V, V_{OUT} = 24V			100		mV
t_{START}	Turn-On Time	I_{OUT} = 0A, C_{OUT} = 10µF Ceramic × 2, 150µF Aluminum, SS = 0.01µF, V_{IN} = 12V, V_{OUT} = 24V			1		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 10µF Ceramic × 2, 150µF Aluminum, V_{IN} = 12V, V_{OUT} = 24V			200		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load C_{OUT} = 10µF Ceramic × 2, 150µF Aluminum, V_{IN} = 12V, V_{OUT} = 24V			200		µs
Regulator Specifics							
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{IN} = 12V, V_{OUT} = 24V	●	1.180	1.200	1.220	V
I_{FB}	Current at V_{FB} Pin	(Note 6)			±5	±50	nA
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins				221		kΩ
SS (I)	Track Pin Soft-Start Pull-Up Current	V_{SS} = 0V		7	10	13	µA
DC_{MAX}	Maximum Duty Cycle	FB = 1.0V (Note 6)				96	%
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 20V		5.2	5.4	5.6	V
$V_{INTVCC(LOAD)}$	I_{NTVCC} Load Regulation	I_{CC} = 0mA to 50mA			0.5	2	%
UVLO	$INTV_{CC}$ UVLO Thresholds	V_{INTVCC} Ramping Up V_{INTVCC} Ramping Down (Note 6)		 3.6	4.3 3.8	4.5	V V
f_S	Typical Output Ripple Voltage Frequency	V_{IN} = 12V, V_{OUT} = 24V, R_{fSET} = Selectable		350		500	kHz
f_{SYNC}	SYNC Frequency Range			350		780	kHz
f_{LOW}	Lowest Frequency	R_{fSET} = 47.5k			350		kHz
f_{NOM}	Nominal Frequency	R_{fSET} =68.1k			500		kHz
f_{HIGH}	Highest Frequency	R_{fSET} = 95.3k			750		kHz
$t_{ON(MIN)}$	Minimum On-Time	Note 3			110		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2), V_{IN} = 12, V_{BIAS} = BV_{IN}, $\overline{SHDN}$ = V_{IN} per the typical application, or otherwise specified in the table.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising		1.18	1.28	1.38	V
V_{RUNHYS}	RUN Pin ON Hysteresis				100		mV
In-Line Protection Control Section							
$\overline{SHDN}$	Active Low Shutdown	4V to 36V Input Threshold	 ●	0.6 0.385	1.4	1.7 2.1	V V
$\overline{SHDN}$ Reset	$\overline{SHDN}$ Reset Time	$\overline{SHDN}$ = 0.4V (Note 6)				100	µs
UV Threshold	Undervoltage Lockout	UV Lockout Threshold, V_{IN} =12V	●	1.24	1.275	1.31	V
UV Hysteresis	UV Input Hysteresis	V_{IN} > 4.5V, Nominal 12V (Note 6)			12		mV
UV_{IN}	UV Input Current	UV =1 .275V (Note 6)	●		±0.3	±1	µA
$V_{TMR(F)}$	TMR Fault Threshold	TMR Rising (Note 6)			1.275		V
$V_{TMR(G)}$	TMR Gate Off Threshold	TMR Rising			1.375		V
$V_{TMR(H)}$	TMR Cooldown High Threshold	V_{IN} = 12V to 24V, TMR Rising			4.3		V
TMR OVER I (5V)	TMR Overcurrent t_{VDS} = 5V	V_{IN}, $\overline{SHDN}$, UV = 5V, V_{FB} = 24.3k, 12V V_{OUT} Shorted			800		µs
TMR OVER I (12V)	TMR Overcurrent t_{VDS} = 12V	V_{IN}, $\overline{SHDN}$, UV =12V, V_{FB} = 11.5k, 24V V_{OUT} Shorted			220		µs
TMR OVER I (24V)	TMR Overcurrent t_{VDS} = 24V	V_{IN}, $\overline{SHDN}$, UV = 24V, V_{FB} = 7.5k, 36V V_{OUT} Shorted			150		µs
$I_{LEAK(\overline{FLT})}$	$\overline{FLT}$ Pin Leak	$\overline{FLT}$ = 36V	●		±2.5		µA
V_{IN} – BV_{IN} Rising Delta	Path Fully Enhanced	Delta V_{IN} – BV_{IN} Enhancing, Boost RUN Pin Enabled	●	0.25	0.5	0.75	V
V_{IN} – BV_{IN} Falling Delta	Path Being Opened	Delta V_{IN} – BV_{IN} Opening, Boost RUN Pin Pulled Low			2.7		V
DC	Retry Duty Cycle, Shorted Output	V_{IN} = 12V, V_{OUT} = 0V, Referenced to BV_{IN}			1		%
$t_{OFF(UV)}$	Undervoltage Turn-Off Propagation Delay	UV Steps from 1.5V to 1V (Note 6)	●		2	5	µs
$V_{OL(\overline{FLT})}$	$\overline{FLT}$ Output Low	I_{SINK} =100µA	●		0.3	0.8	V
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA				0.3	V
$I_{PGOOD(LEAK)}$	PGOOD Leakage Current	V_{PGOOD} = 6V				±1	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive		 –12 8	 –10 10	 –8 12	 % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4656 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4656E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4656I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The minimum on-time condition is specified for a peak-to-peak inductor ripple current of ~40% of I_{MAX} Load. (See Applications Information section)

Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

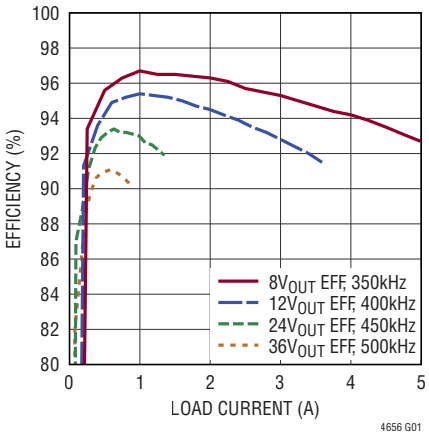
Note 5: Guaranteed by design.

Note 6: 100% tested at wafer level.

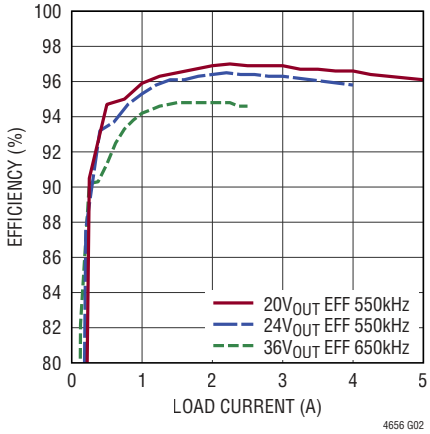
Note 7: JEDEC board θ values are determined by simulation per JESD51 conditions. Demo board θ values are obtained with demo board. Refer to Figure 9 to Figure 17 and Table 2 to Table 5 for lab ameasurement and derating information.

TYPICAL PERFORMANCE CHARACTERISTICS

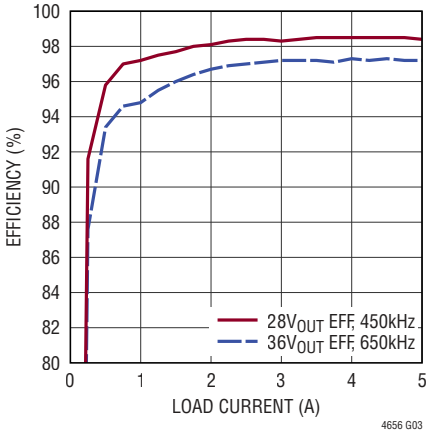
$5V_{IN}$ Efficiency



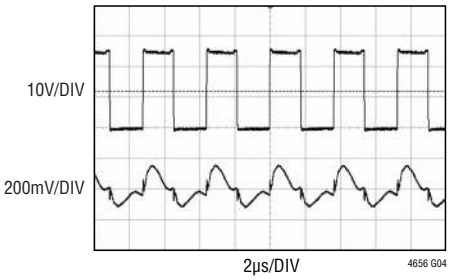
$12V_{IN}$ Efficiency



$24V_{IN}$ Efficiency

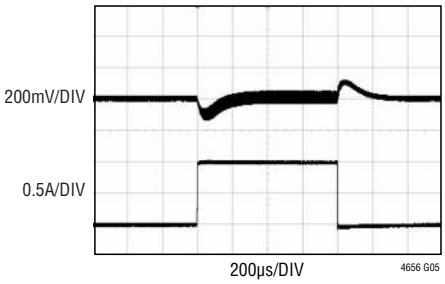


12V to 24V at 4A Switch and Ripple



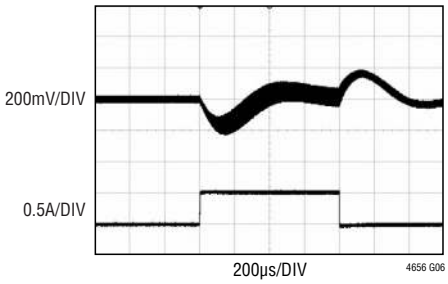
12V TO 24V AT 4A
C_{OUT} = 100µF ×2, 6.8µF ×2 CERAMIC

5V to 12V Boost Load Step



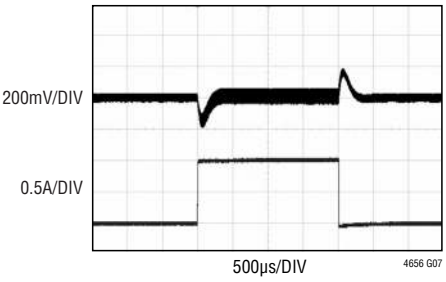
C_{OUT} = 100µF ×2, 6.8µF ×2 CERAMIC,
28mΩ ESR

5V to 24V Boost Load Step



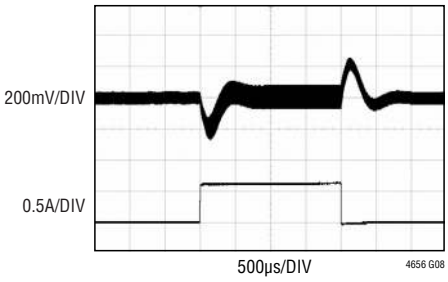
C_{OUT} = 100µF ×2, 6.8µF ×2 CERAMIC
28mΩ ESR

12V to 24V Boost Load Step



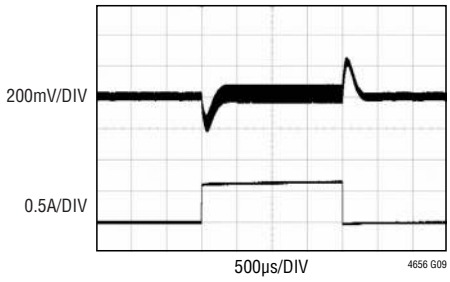
C_{OUT} = 100µF ×2, 6.8µF ×2 CERAMIC
28mΩ ESR

12V to 36V Boost Load Step



C_{OUT} = 100µF ×2, 6.8µF ×2 CERAMIC
28mΩ ESR

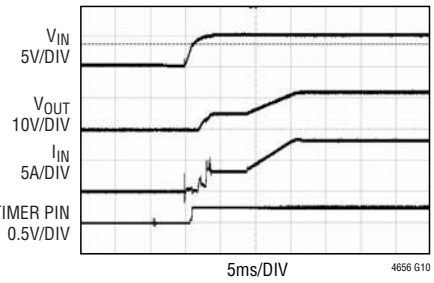
24V to 36V Boost Load Step



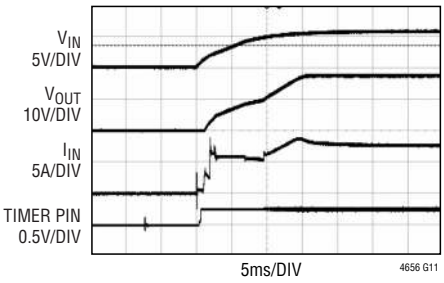
C_{OUT} = 100µF ×2, 6.8µF ×2 CERAMIC
28mΩ ESR

TYPICAL PERFORMANCE CHARACTERISTICS

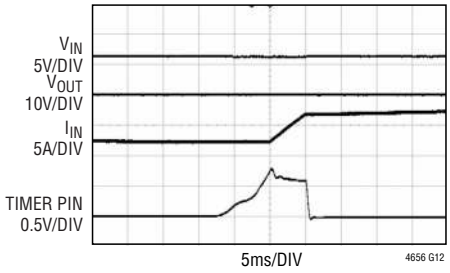
5V to 12V Boost HOT Plugged Start-Up Into 3.5A Load,



12V to 24V Boost HOT Plugged Start-Up Into 4A Load



24V to 36V Boost HOT Plugged Start-Up Into 5A Load



PIN FUNCTIONS

V_{IN} (A9–A12, B9–B12, C9–C12, D10–D12): Power Input Pins to Protection Path. Apply main input voltage between these pins and GND pins. Recommend placing minimum 1µF input decoupling capacitance directly between V_{IN} pins and GND pins.

BV_{IN} (A1–A4, B1–B4, C1–C4, D1–D3): Boost Power Input Pins. Recommend placing input decoupling capacitance directly between BV_{IN} pins and GND pins.

V_{OUT} (J1–J6, K1–K6, L1–L6, M1–M6): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

GND (A5–A6, B5–B6, C5–C6, D4–D9, E1–E7, E9–E12, F2–F5, F10–F12, G1–G3, G5, G7–G8, G10–G12, H1, H8–H12, J7–J11, K7–K11, L7–L12, M7–M12): Ground Pins for the Input and Output Capacitors and Small Signal Component Connection.

SW (J12, K12): Switching node that is used for testing purposes.

MODE_PLLIN (G6): External Synchronization Input to Phase Detector and Mode Operation Input. When an external clock is applied to this pin, it will force the converter into forced continuous mode of operation and the phase-locked loop will force the rising boost switch signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, this input determines how the LTM4656 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to less than $INTV_{CC}$–1.3V selects pulse-skipping operation. This can be done by adding a 100k resistor between the MODE_PLLIN pin and $INTV_{CC}$. Forced continuous operation can be selected by tying this pin to $INTV_{CC}$.

FREQ (H6): The Frequency Control Pin for the Internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. The frequency can be programmed from 300kHz to 780kHz by connecting a resistor from the FREQ pin to GND. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator. See Typical Applications section.

SS (F7): Output Soft-Start Input. A capacitor to ground at this pin sets the ramp rate of the output voltage during start-up.

V_{FB} (E8): The Negative Input of the Error Amplifier for Each Channel. Internally, this pin is connected to V_{OUT} with a 221k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and GND pins. In PolyPhase® operation, tying the V_{FB} pins together allows for parallel operation. See Typical Applications section for details.

COMP (F6): Current Control Threshold and Error Amplifier Compensation Point for the Regulator. The current comparator threshold increases with this control voltage. Tie

PIN FUNCTIONS

all COMP pins together for parallel operation. The device is internal compensated. The LTM4656-1 offers an External Compensation option.

SENSE1 (A7–A8, B7–B8, C7–C8): These pins are the output side of the input protection power MOSFET, and the input to the onboard 4mΩ current sense resistor that sets maximum input current limit to trip off and retry in a output short. Measuring the voltage drop between SENSE1 and BV_{IN}, and dividing by the 4mΩ resistance gives the input current for a given operating condition in the boost converter.

RUN (H7): RUN Pin Monitor. The threshold level of 1.28V will turn on the boost converter. An internal 75k resistor is connected from this pin to BV_{IN}, and a 5.1V Zener diode to GND is internal to the module for limiting the voltage on the RUN pin to 5V. The RUN pin is allowed to turn on from an open-collector control coming from the in-line protection control when the voltage at the BV_{IN} pin is within 0.5V of V_{IN} and 3V above GND, indicating the protection MOSFET is fully on. The state of the pin stays on until the BV_{IN} pin voltage drops below 2V. See Block Diagram.

$INTV_{CC}$ (G9): Output of Internal 5.4V LDO. Power supply for internal control circuits and gate drivers. There is an internal 4.7µF low ESR ceramic capacitor from this pin to ground for decoupling.

V_{BIAS} (F9): Main Control Supply Pin. It is normally tied to the input supply BV_{IN} or to the output of the boost converter. A bypass capacitor should be tied between this pin and the GND pin. The operating voltage range on this pin is 4.5V to 36V.

PGOOD (F8): Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is more than ±10% away from the regulated output voltage. To avoid false trips, the output voltage must be outside of the range for 25µs before this output is activated.

TMR (G4): Fault Timer Input. An internal 0.01µF capacitor to ground sets the times for early fault warning, fault turn-off, and cooldown periods. The current charging up this pin during fault conditions depends on the voltage difference between the V_{IN} and BV_{IN} pins. When TMR reaches 1.275V, the $\overline{FLT}$ pin pulls low to indicate the detection of a fault condition. If the condition persists, the pass transistor turns off when TMR reaches the threshold of 1.375V. A 2µA current source then continues to pull the TMR up. When TMR reaches 4.3V, the 2µA current reverses direction and starts to pull the TMR pin low. When TMR reaches the retry threshold of 0.5V, the GATE pin pulls high turning back on the pass transistor. See Typical Applications section.

NC (E3): Float Pin.

$\overline{SHDN}$ (F1): The LTM4656 can be shut down to a low current mode when the voltage at the $\overline{SHDN}$ pin is pulled below the shutdown threshold of 0.4V. The quiescent current drops down to 40µA with internal circuitry turned off. This pin will shut down the in-line protection and the boost converter. The $\overline{SHDN}$ pin can be pulled up to V_{IN} MAX or below GND by up to V_{IN} MAX without damage. The $\overline{SHDN}$ pin is pulled up to V_{IN} with an internal 100k resistor for active on. An V_{IN} rated open collector can be used to controlled this pin for enabling the in-line protection and the boost converter, or a Zener diode can be placed from this pin to ground to interface to lower voltage rated pull downs.

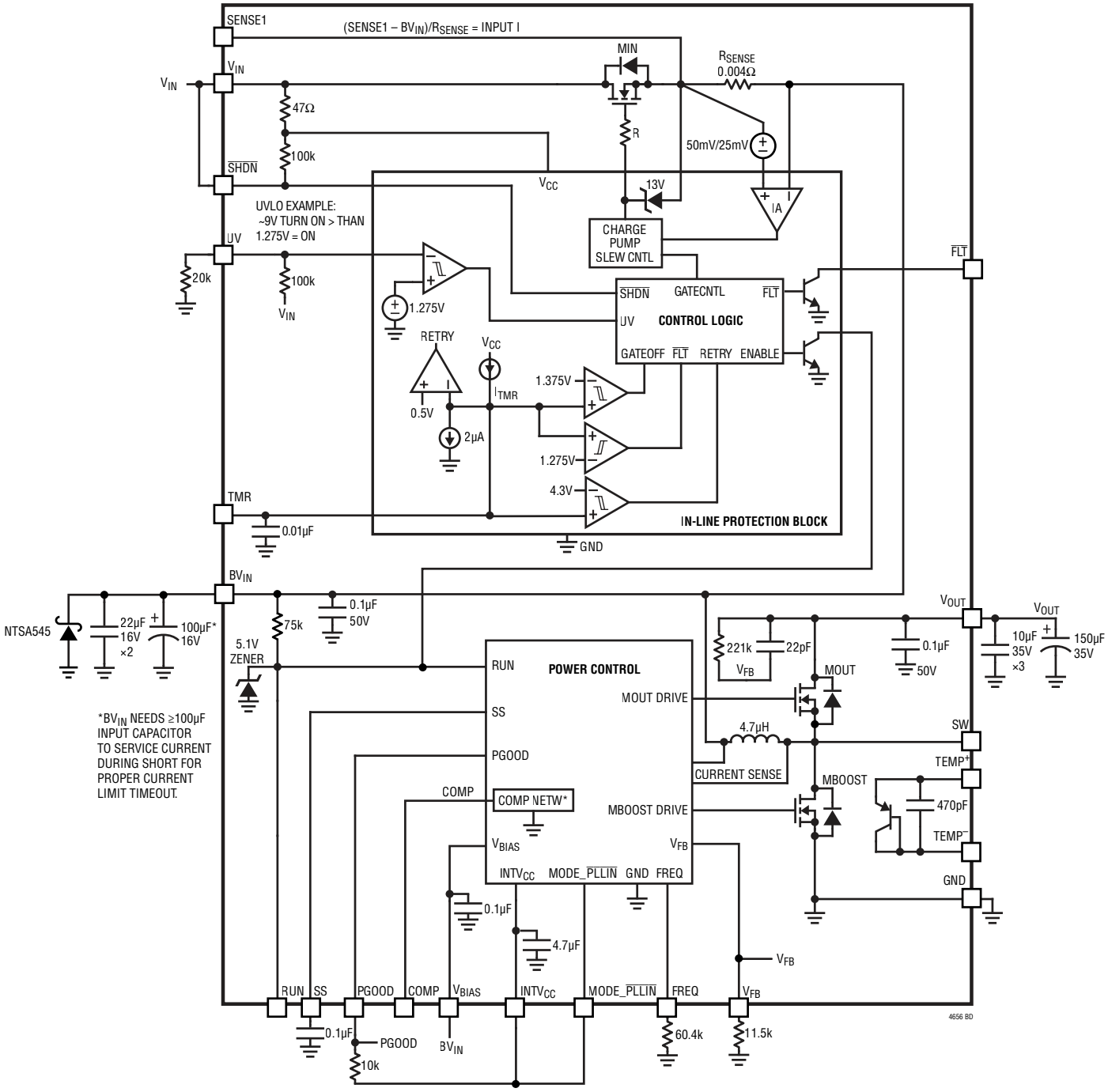
UV (H2): Undervoltage Comparator Input. When UV falls below its threshold of 1.275V, the GATE pin is pulled down with a 1mA current. When UV rises above 1.275V plus the hysteresis, the pull-down current disappears and the GATE pin is pulled up by the internal charge pump. This is used to set up an undervoltage lockout to limit the input current during startup. There is an internal 100k resistor from this pin to V_{IN} to set up with an external resistor an under voltage trip point. If unused, connect to V_{CC}. See Typical Applications section.

$\overline{FLT}$ (H3): Open Collector Fault Output. This pin pulls low after the voltage at the TMR pin has reached the fault threshold of 1.275V. It indicates the pass transistor is about to turn off because the device is in an overcurrent condition (current fault). The internal NPN is capable of sinking up to 100µA of current while maintaining a low level of 0.8V max.

$TEMP^+$ (H4): Onboard temperature diode for monitoring each channel with differential connections for noise immunity. See Block Diagram.

$TEMP^-$ (H5): Onboard temperature diode for monitoring each channel with differential connections for noise immunity. See Block Diagram.

BLOCK DIAGRAM



*LTM4656-1 Optional External Compensation

OPERATION

The LTM4656 is a single output standalone non-isolated step-up switching mode DC/DC power supply with input current limit protection during an output short. This module provides a precisely regulated output voltage programmable via one external resistor from 6V to 36V and delivers up to 5A output current with few external input and output capacitors. During normal operation the LTM4656 senses input current through an input protected front end. The LTM4656 softly turns on with a controlled inrush and will perform a low duty cycle auto-retry during an output short circuit. The output short trip time is controlled by how much short-circuit current is applied and the amount of voltage across the in-line protection switch. The typical application schematic is shown in Figure 17. See Typical Applications section for explanation and curves.

The LTM4656 contains an integrated fixed frequency, current mode boost controller, power MOSFETs, inductor, in-line protect circuitry and other supporting discrete components. The default switching frequency is 500kHz. For noise-sensitive applications, the switching frequency can be adjusted by an external resistor and the µModule regulator can be externally synchronized to a clock.

With current mode control and internal feedback loop compensation, the LTM4656 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control allows the LTM4656 to parallel for increase power delivery.

APPLICATIONS INFORMATION

IN-LINE PROTECTION SECTION

Referring to the Block Diagram, the input voltage is applied to V_{IN}. The power MOSFET MIN is controlled by a charge pump high side drive that is slowly turned on after the $\overline{SHDN}$ pin is either pulled up to V_{IN} or driven from an open collector drive rated to V_{IN}. The UV pin has an internal 100k resistor to V_{IN} that can be used with an external resistor to ground to set a UVLO trip point for V_{IN}. This is valuable to limit turn-on to a specific input voltage level. When both the $\overline{SHDN}$ and UV pin thresholds are met, then the gate voltage begins to ramp up at a control rate and the MIN source pin will follow. Gate turn-on time is ~10ms. The R_{SENSE} in series with this path monitors the current going to the boost converter. The LTM4656 monitors the voltage drop between the SENSE1 and BV_{IN} pins to protect against overcurrent faults. An internal amplifier limits the voltage across the internal 4mΩ current sense resistor to 50mV. This is reduced to 25mV in a severe fault when BV_{IN} is below 2V. In this fault condition, a timer is started inversely proportional to MOSFET stress. Before the timer expires, the $\overline{FLT}$ pin pulls low to warn of an impending power down. If the condition persists, the MOSFET is turned off, and restarts after a cooldown period. BV_{IN} needs at least 100µF capacitance to service proper current limit level to eliminate any overtemperature timeout oscillations.

FAULT TIMER SECTION

A 0.01µF capacitor is connected internal to the TMR pin and ground to set the times for early fault warning, fault turn-off, and cooldown periods. This capacitor is selected to assure the MIN MOSFET is turn-off fast enough. The TMR charging current increases linearly from 8µA with V_{DS} < 0.5V to 120µA with V_{DS} = 40V. V_{DS} is inferred from the drop across V_{IN} and SENSE1. See Figure 1. The current charging up this TMR pin during fault conditions depends on the voltage difference across MIN MOSFET between the V_{IN} and SENSE1 pins. This increase in TMR current is to assure a faster turn off during an overcurrent fault with substantial voltage across the MIN MOSFET. This turn-off time is correlated with the MIN MOSFET SOA capability to assure the MOSFET can handle this power dissipation for that period of time. When TMR reaches 1.275V, the $\overline{FLT}$ pin pulls low to indicate the detection of a fault condition. If the condition persists, the pass transistor turns off when TMR reaches the threshold of 1.375V. A 2µA current source then continues to pull the TMR up. When TMR reaches 4.3V, the 2µA current reverses direction and starts to pull the TMR pin low. When TMR reaches the retry threshold of 0.5V, the GATE pin pulls high turning back on the pass transistor. See overcurrent fault diagram in Figure 2.

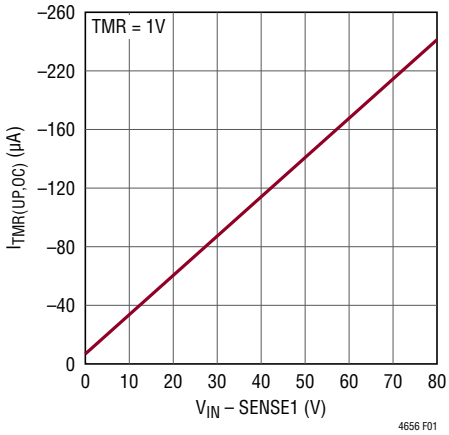


Figure 1. Overcurrent TMR Current vs V_{IN} – SENSE1 Voltage

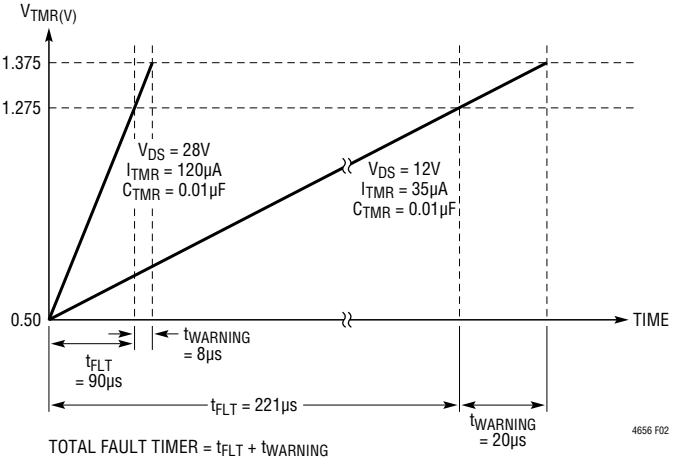


Figure 2. Overcurrent Fault Time with 0.01µF

APPLICATIONS INFORMATION

When the TMR pin reaches 1.275V, the $\overline{FLT}$ pin is latched low as an early warning of impending shutdown, then it continues unabated until the TMR reaches 1.375V, producing an early warning period given by:

$$t_{FLT} = 0.01\mu F \bullet \frac{1.275V - 0.5V}{I_{TMR}}$$

$$t_{WARN} = 0.01\mu F \bullet \frac{1.375V - 1.275V}{I_{TMR}}$$

I_{TMR} taken from Figure 1.

Because I_{TMR} is a function of V_{IN}–SENSE1, the exact time in current limit depends upon the input waveform and the time required for the output current to come into regulation. Testing of the overall solution should be verified, and compared to the MOSFET SOA curves.

COOLDOWN PHASE

Cooldown behavior is initiated by overcurrent. During the cooldown phase, the timer continues to charge from 1.375V to 4.3V with 2µA, and then discharges back down to 0.5V with 2µA, for a total equivalent voltage swing of 6.725V. The cooldown time is given by:

$$t_{COOL} = 0.01\mu F \bullet \frac{6.725V}{2\mu A} = 33.6ms$$

This long cool time assures that during retry the MOSFET does not overheat.

The LTM4656 will auto-retry at the end of the cooldown phase. Retry is automatically initiated. The cooldown phase may be interrupted in the LTM4656 by pulling $\overline{SHDN}$ low for at least 10ms.

The $\overline{FLT}$ pin goes high in shutdown and is cleared high when power is first applied to V_{IN}.

Brief overcurrent conditions interrupt the operation of the timer. If the TMR pin has not yet reached 1.275V when fault drops out of current limit, the timer capacitor is discharged back to 0.5V with a 2µA current sink. If the TMR voltage crosses 1.275V, then $\overline{FLT}$ is set low. If the overcurrent abates before reaching 1.375V, the timer capacitor discharges with 2µA back to 0.5V, whereupon $\overline{FLT}$ resets high. If several short overcurrent events occur in rapid succession, the timer capacitor will integrate the charging and discharging currents. Figure 20 shows an overcurrent fault wave from and a retry cycle.

MIN MOSFET SOA CURVE

Figure 3 shows the MIN MOSFET SOA curve. This curve can be compared to the period of time the MIN Power MOSFET stays on during a fault condition with an overcurrent flowing through MIN, and the worse-case voltage across the MIN MOSFET.

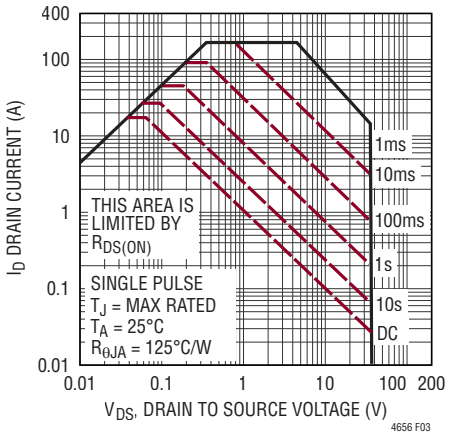


Figure 3. MIN Internal MOSFET SOA Curves

APPLICATIONS INFORMATION

Figure 4 and Figure 5 show the overcurrent fault waveforms, and the timer pin timeout period as a function of the amount of voltage across the MIN power MOSFET during an overcurrent fault. Figure 4 shows a 10V to 36V boost in short-circuit, and Figure 5 shows a 28V to 36V boost in a short-circuit. Figure 2 shows that the over current timer (TIMER pin) will expire at ~240µs in a short-circuit at the 1.375V threshold with 10V input, will expire at 73µs at 40V input. Figure 4 timeout with 10V input and Figure 5 time out with 28V input are very close to Figure 2 time out period relative to input voltage. These timeout periods across the full input range can be checked against the Figure 3 MIN MOSFET SOA curves to ensure adequate margin relative to voltage across the input protection MOSFET and the current flowing through. Adequate guard band is to ensure that these conditions are OK overtemperature.

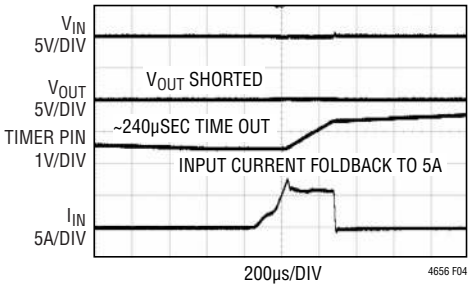


Figure 4. 10V Input to 36V Output Short Input Current Trip Waveform

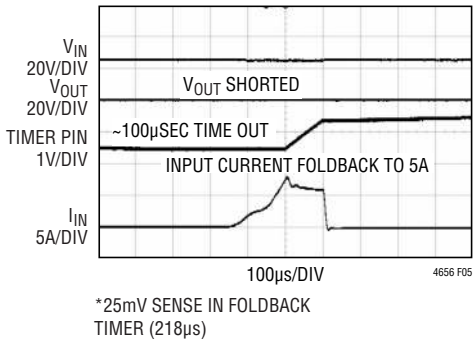


Figure 5. 28V Input to 36V Output Short Input Current Trip Waveform

TURN-ON INRUSH CURRENT CONTROL AND POWER-UP INTO LOAD

The LTM4656 turns on the MIN power MOSFET with a time control ramp of 10ms. When the voltage at the SENSE1 pin is within 0.5V of V_{IN} and 3V above GND, indicating the external MOSFET is fully on, then the internal ENABLE signal goes high impedance to allow the RUN pin to activate the boost converter. The state of the internal ENABLE signal is latched until the SENSE1 pin voltage drops below 2V, resetting the latch. Utilizing the UV pin to set a UVLO voltage before turn on, then having the boost converter turn on after the MIN MOSFET is fully enhanced, and the a 0.1µF soft-start capacitor will assure no false overcurrent trips at start-up.

SYNCHRONOUS BOOST CONVERTER SECTION

The LTM4656 has a high power synchronous converter downstream of the input protection. A synchronous boost converter inherently has difficulty with output short-circuit due to the MOUT output power MOSFET body diode conducting.

The input protection path will control the input current to boost converter and auto-retry during an output short.

The LTM4656 uses a constant-frequency, current mode step-up control architecture. During normal operation, the MBOT bottom MOSFET is turned on when the clock sets the internal RS latch, and is turned off when the main (ICMP) current comparator resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the COMP pin, which is the output of the error amplifier. The error amplifier compares the output voltage feedback signal at the V_{FB} pin.

The LTM4656-1 provides optional External Compensation.

In a boost converter, the required inductor current is determined by the load current, V_{IN} and V_{OUT}. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the error amp to increase the COMP voltage until the average inductor current in the channel matches the new requirement based on the new load current. After the bottom MOSFET is turned off

APPLICATIONS INFORMATION

each cycle, the top MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator or the beginning of the next clock cycle.

In a step-up boost converter, the duty cycle can be calculated at:

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

Note that at low input voltages, small voltage drops due to series resistance become critical and greatly limit the power delivery capability of the converter.

The boost controller has an internal 1.2V reference voltage, and a 221k 1% internal feedback resistor connects V_{OUT} and V_{FB} pins together. Adding a resistor R_{FB} from V_{FB} pin to GND programs the output voltage:

$$R_{FB} = \frac{1.2V}{V_{OUT} - 1.2V} \bullet 221k$$

Table 1. V_{FB} Resistor Value vs Various Output Voltages

V_{OUT} (V)	6V	8V	10V	12V	20V	24V	30V	36V
R_{FB}	54.9k	39.2k	30.9k	24.3k	14k	11.5k	9.31k	7.5k

For parallel operation of N-piece of LTM4656 modules, the following equation can be used to solve for R_{FB}:

$$R_{FB} = \frac{1.2V}{V_{OUT} - 1.2V} \bullet \frac{221k}{N}$$

The V_{FB}, COMP, SS, RUN and $\overline{SDHN}$ pins should be connected together.

The UV pins can be tied together taking into account the internal 100k resistor to V_{IN} will reduce N times when selecting a single resistor to set an UVLO operating point for the paralleled modules.

INPUT DECOUPLING CAPACITORS

The LTM4656 module should be connected to a low AC-impedance DC source. The input ripple current in a boost converter is relatively low (compared with the output ripple current) because this current is continuous. The input capacitor, C_{IN}, voltage rating should comfortably exceed the maximum input voltage, and placed on the BV_{IN} pins.

Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of the C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

The input I_{RMS} current in boost is fairly low since the input current is continuous. Primary input capacitance is to maintain low input ripple voltage.

The input I_{RMS} current equation:

$$I_{RMS} = \sqrt{\frac{I_O{}^2 + (\Delta I)^2}{12}}$$

Where I_O is output current, and

$$\Delta I = \frac{V_{IN} \bullet D}{4.7\mu H \bullet FREQ}$$

The output capacitor will see discontinuous current, thus the peak current can be high, and the C_{OUT} I_{RMS} is significant. The equation for the C_{OUT} I_{RMS} current is:

$$I_{RMS} = I_{OUT} \sqrt{\frac{V_{OUT} - V_{IN}}{V_{IN}}}$$

The output ripple has two components, one that is related to output capacitance minimum:

$$C_{OUT} = \frac{I_{OUT} \bullet D}{FREQ \bullet \Delta V_{OUT}}$$

Where ΔV_{OUT} is the output ripple based on total output capacitance. The second is based on total equivalent output capacitance ESR:

$$\Delta V_{OUTESR} = ESR \bullet \left(\frac{I_{OUT}}{1-D} + \frac{\Delta I}{2} \right)$$

APPLICATIONS INFORMATION

The output capacitor recommendations and internal control loop compensation assure stability over the operating ranges. The Analog Devices LTpowerCAD® design tool is available to download online for RMS current, output ripple, stability and transient response analysis.

LOW VOLTAGE OPERATION

The LTM4656 is designed to allow start-up from input voltages as low as 4.5V. The limiting factors for the low voltage applications become the availability of the power source to supply sufficient power to the output at the low input voltage, and the maximum duty cycle, which is clamped at 96%. Note that at low input voltages, small voltage drops due to series resistance become critical and greatly limit the power delivery capability of the converter. The input current can get large at high boost ratios. The input is limited to a minimum of 9A. The below equation can be used to calculate the input current need to support a particular design.

$$I_{IN} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN}}$$

For example, 5V to 12V at 3.5A output current would equate to an input current of ~8.5A.

$\overline{SHDN}$ AND RUN PINS

The $\overline{SHDN}$ pin controls the complete shutdown of the LTM4656. When this pin is below 0.4V, the LTM4656 will be in complete shutdown drawing only 40µA. When $\overline{SHDN}$ goes above 2.1V then the LTM4656 will enable. The LTM4656 boost converter can be shut down using the RUN pin while the inline overcurrent protection is still powered. Pulling this pin below 1.28V shuts down the main boost control loop. Pulling this pin below 0.7V disables the boost controller and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, total current draw is about 50µA.

SOFT-START (SS PIN)

The start-up of the V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 1.2V reference, the LTM4656 regulates the V_{FB} pin voltage to the voltage on the SS pin instead of 1.2V. Soft-start is enabled by simply connecting a capacitor from the SS pin to ground. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTM4656 will regulate the V_{FB} pin (and hence, V_{OUT}) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from V_{IN} to its final regulated value. The total soft-start time will be approximately:

$$T_{SS} = C_{SS} \bullet \frac{1.2V}{10\mu A}$$

A 0.1µF is a good value to use for C_{SS}. This provides a slow 12ms ramp that will slowly turn on the boost regulator into load, and eliminate false overcurrent tripping at start-up.

$INTV_{CC}$ Power

The LTM4656 boost control section features an internal P-channel low dropout linear regulator (LDO) that supplies power at the $INTV_{CC}$ pin from the V_{BIAS} supply pin. $INTV_{CC}$ powers the gate drivers and much of the boost control's internal circuitry. The V_{BIAS} LDO regulates $INTV_{CC}$ to 5.4V. It can supply at least 50mA and is bypassed to ground with an internal 4.7µF ceramic capacitor.

Power Good

The PGOOD pin is connected to an open-drain of an N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} pin voltage is not within ±10% of the 1.2V reference voltage. The PGOOD pin is also pulled low when the corresponding RUN pin is low (shutdown). When the V_{FB} pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V (ABS max).

Loop Compensation

The LTM4656 has internal compensation while the LTM4656-1 provides for optimized external compensation. LTpowerCAD can be used to optimize External Compensation.

APPLICATIONS INFORMATION

Light Load Current Operation—Burst Mode Operation, Pulse-Skipping or Continuous Conduction (MODE_PLLIN Pin)

The LTM4656 boost converter can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the MODE_PLLIN pin to ground. To select forced continuous operation, tie the MODE_PLLIN pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE_PLLIN pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$–1.3V. When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 30% of the maximum sense voltage even though the voltage on the COMP pin indicates a lower value.

If the average inductor current is higher than the required current, the internal error amplifier will decrease the voltage on the COMP pin. When the COMP voltage drops below 0.425V, an internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The COMP pin is then disconnected from the output of the EA and parked at 0.450V.

In sleep mode, much of the internal boost controller circuitry is turned off and the LTM4656 draws only 50µA of quiescent current. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the internal error amplifier output begins to rise. When the output voltage drops enough, the COMP pin is reconnected to the output of the internal error amplifier, the sleep signal goes low, and the controller resumes normal operation by turning on the bottom external MOSFET on the next cycle of the internal oscillator. When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The internal reverse current comparator (IR) turns off the top external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous current operation.

In forced continuous operation or when clocked by an external clock source to use the phase-locked loop. See the Frequency Selection and Phase-Locked Loop (FREQ and MODE_PLLIN Pins) section, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the COMP pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantages of lower output voltage ripple and less interference to audio circuitry, as it maintains constant-frequency operation independent of load current.

When the MODE_PLLIN pin is connected for pulse-skipping mode, the LTM4656 boost converter operates in PWM pulse-skipping mode at light loads. In this mode, constant-frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the internal current comparator may remain tripped for several cycles and force the external bottom MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and MODE_PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTM4656 boost controllers can be selected using the FREQ pin. If the MODE_PLLIN pin is not being driven by an external clock source, the FREQ pin can be tied to

APPLICATIONS INFORMATION

GND, tied to $INTV_{CC}$, or programmed through an external resistor. Tying FREQ to GND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 6. The recommended operating range for the LTM4656 is 300kHz to 780kHz based on the internal 4.7µH inductor.

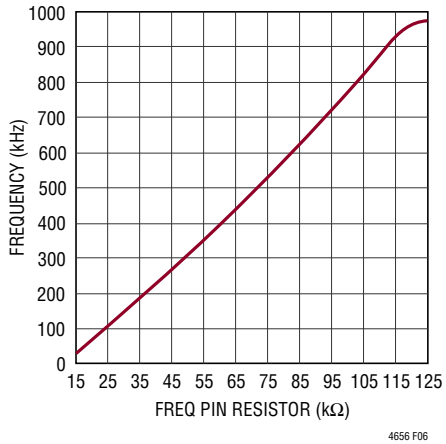


Figure 6. Relationship Between Oscillator Frequencies and Resistor Value at the FREQ Pin

A phase-locked loop (PLL) is available on the LTM4656's boost converter to synchronize the internal oscillator to an external clock source that is connected to the MODE_PLLIN pin. The LTM4656's boost converter phase detector adjusts the voltage (through an internal low pass filter) of the VCO input to align the turn-on of the external bottom MOSFET to the rising edge of the synchronizing signal.

The VCO input voltage is pre-biased to the operating frequency set by the FREQ pin before the external clock is applied. If pre-biased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of BG. The ability to pre-bias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The MODE_PLLIN is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the MODE_PLLIN pin are 1.6V (rising) and 1.2V (falling).

Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating of the boost controller (such as an $INTV_{CC}$ short to ground), the overtemperature shutdown circuitry will shut down the boost converter. When the junction temperature exceeds approximately 170°C, the overtemperature circuitry disables the $INTV_{CC}$ LDO, causing the $INTV_{CC}$ supply to collapse and effectively shut down the entire boost controller chip. Once the junction temperature drops back to approximately 155°C, the $INTV_{CC}$ LDO turns back on. Long-term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten life. As explain above in the inline protection, if an overcurrent short occurs in the boost converter section, then the inline protection will operate in a low duty cycle retry mode.

Thermal Performance

The LTM4656 provides adequate heat sinking utilizing the inductor on top of package, and can either be cooled with airflow or other heat sinking methods. Figure 7 shows a 12V to 24V boost at 96W conversion with only ~ 36°C rise with 200LFM.

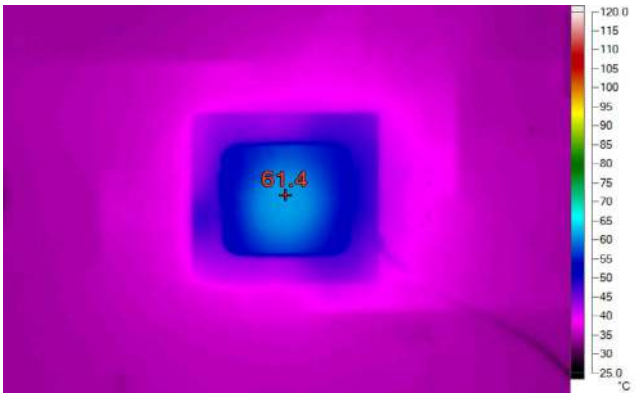


Figure 7. $12V_{IN}$ to $24V_{OUT}$ at 4A (96W), 200LFM Air Flow Thermal Plot

APPLICATIONS INFORMATION

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 (Test Boards for Area Array Surface Mount Package Thermal Measurements). The motivation for providing these thermal coefficients is found in JESD51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

θ_{JA}, the thermal resistance from junction-to-ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$, the thermal resistance from junction-to-ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

θ_{JCtop}, the thermal resistance from junction-to-top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured at a specified distance from the package, using a two-sided, two-layer board. This board is described in JESD 51-9.

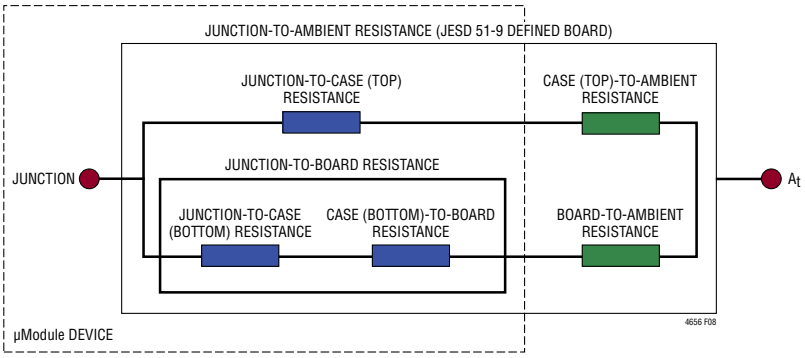


Figure 8. Graphical Representation of JESD51-12 Thermal Coefficients

APPLICATIONS INFORMATION

A graphical representation of the aforementioned thermal resistances is given in Figure 8; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory tests have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly define chamber. This $\theta_{JB} + \theta_{BA}$ value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 5V, 12V and 24V input power loss curves in Figure 9 to Figure 11 can be used in coordination with the load current derating curves in Figure 12 to Figure 17 for calculating an approximate θ_{JA} thermal resistance for the LTM4656 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the ambient temperature. These approximate factors is 1.4 assuming the junction temperature at 120°C. The output voltages are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 15, the load current is derated to ~3.2A at ~ 80°C with no air or heat sink and the power loss for the 12V to 24V at 3.2A output is about 3W. The 4.48W loss is calculated with the ~ 3W room temperature loss from the 12V to 24V power loss curve at 3.2A, and the 1.4 multiplying factor. If the 80°C ambient temperature is subtracted from the 120°C junction temperature, then

APPLICATIONS INFORMATION

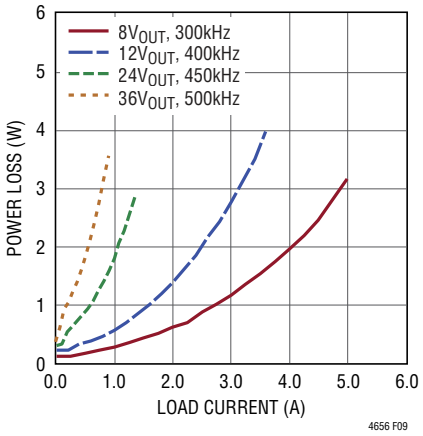


Figure 9. Power Loss vs Load Current $5V_{IN}$ Based on LTM4656

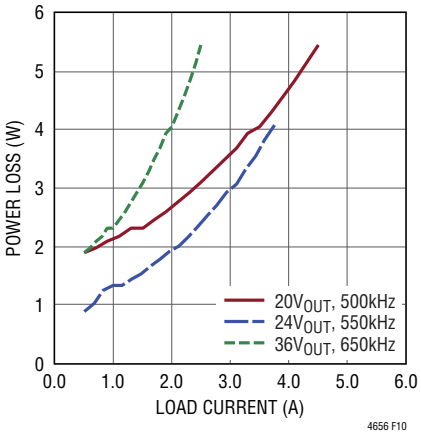


Figure 10. Power Loss vs Load Current $12V_{IN}$ Based on LTM4656

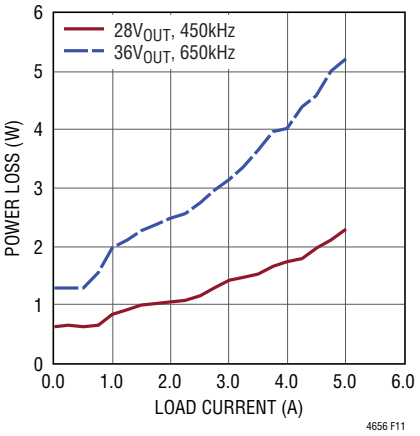


Figure 11. Power Loss vs Load Current $24V_{IN}$ Based on LTM4656

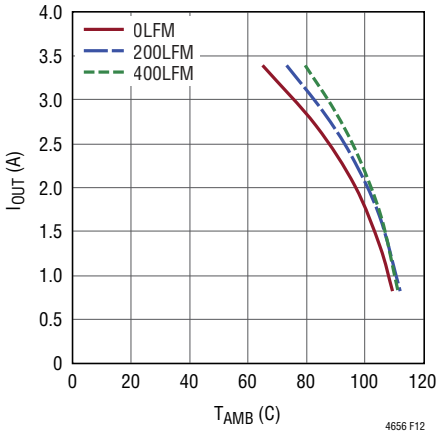


Figure 12. LTM4656 $5V_{IN}$ $12V_{OUT}$ 400kHz no HS

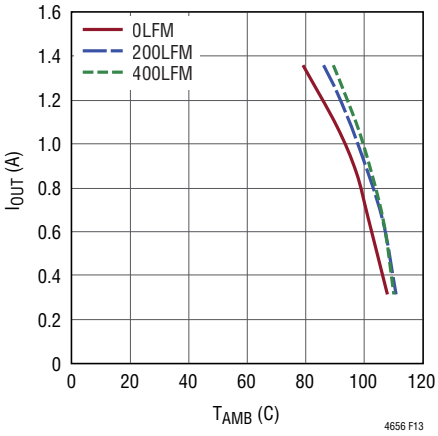


Figure 13. LTM4656 $5V_{IN}$ $24V_{OUT}$ 500kHz no HS

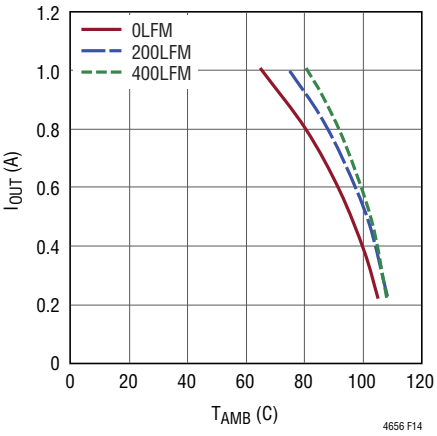


Figure 14. LTM4656 $5V_{IN}$ $36V_{OUT}$ 500kHz no HS

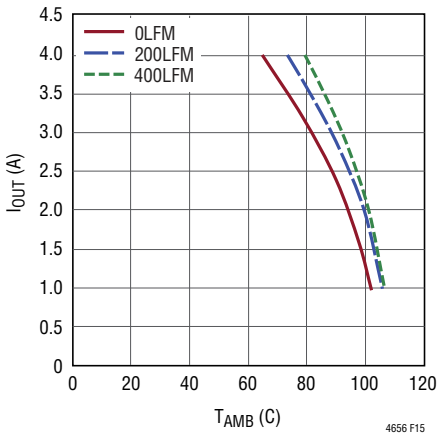


Figure 15. LTM4656 $12V_{IN}$ $24V_{OUT}$ 550kHz no HS

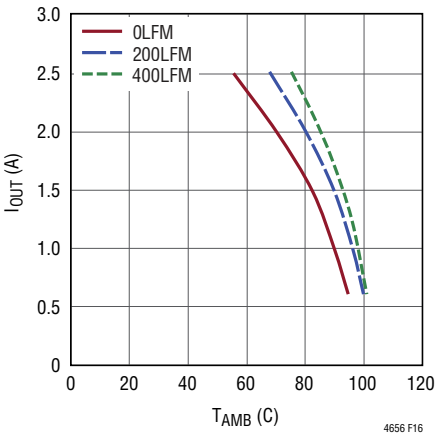


Figure 16. LTM4656 $12V_{IN}$ $36V_{OUT}$ 650kHz no HS

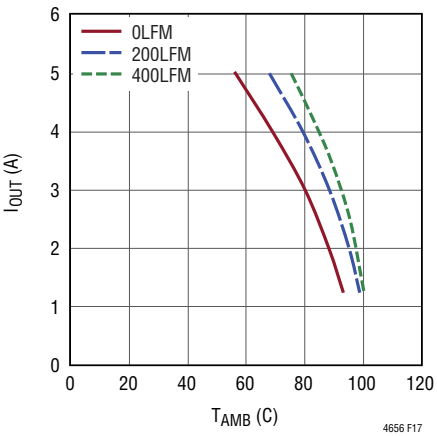


Figure 17. LTM4656 $24V_{IN}$ $36V_{OUT}$ 650kHz no HS

APPLICATIONS INFORMATION

Table 2. 12V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA}(°C/W)
Figure 12	5	Figure 9	0	None	10
Figure 12	5	Figure 9	200	None	8
Figure 12	5	Figure 9	400	None	7.5

Table 3. 24V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA}(°C/W)
Figures 13, 15	5, 12	Figure 10	0	None	10
Figures 13, 15	5, 12	Figure 10	200	None	8
Figures 13, 15	5, 12	Figure 10	400	None	7.5

Table 4. 36V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA}(°C/W)
Figures 14, 16, 17	5, 12, 24	Figure 11	0	None	10
Figures 14, 16, 17	5, 12, 24	Figure 11	200	None	8
Figures 14, 16, 17	5, 12, 24	Figure 11	400	None	7.5

Table 5. Capacitor Matrix

BV_{IN} (BULK) (µF)	BV_{IN} (CER) (µF)	V_{IN} (V)	V_{OUT} (V)	FREQ (kHz)	MAX IN 8.5A			OUT (W)	C_{OUT} (CER) (µF)	C_{OUT} (Bulk)
					LOAD	I_{IN}	DC			
100	22	5	8	300	5	8.65	0.38	40	10 ×2	100µF, 30mΩ ×2
100	22	5	12	400	3.6	9.34	0.58	43.2	10 ×2	100µF, 30mΩ ×2
100	22	5	24	500	1.35	7.18	0.79	32.4	10 ×2	100µF, 30mΩ ×2
100	22	5	36.	500	1	7.83	0.86	36	10 ×2	100µF, 30mΩ ×2
100	22	12	20	500	5	8.68	0.40	100	10 ×2	100µF, 30mΩ ×2
100	22	12	24	550	4	8.42	0.50	96	10 ×2	100µF, 30mΩ ×2
100	22	12	36	650	2.5	7.95	0.67	90	10 ×2	100µF, 30mΩ ×2
100	22	12	28	650	3.25	8.02	0.57	91	10 ×2	100µF, 30mΩ ×2
100	10	24.	28	500	5	5.94	0.14	140	10 ×2	100µF, 30mΩ ×2
100	10	24	36	650	5	7.70	0.33	180	10 ×2	100µF, 30mΩ ×2

BV_{IN} BULK	Suncon HVA Series	100µF, 10V	V_{OUT} BULK	Suncon HVA Series	100µF, 16V
	Suncon HVA Series	100µF, 16V		Suncon HVPF Series	100µF, 25V
	Suncon HVPF Series	100µF, 25V		Suncon HVT Series	150µF, 35V
				Suncon HVP Series	82µF, 50V
BV_{IN} CER	Murata GRM31CR71A226K	22µF, 16V	V_{OUT} CER	Murata GRM32DR71E106KA12L	10µF, 25V
	Murata GRM32ER61C226ME20	22µF, 16V		Murata GRM32ER71H106KA12L	10µF, 50V
	Murata GRM31CR71E106KA12L	10µF, 25V			
	Murata GRM32ER71H106KA12L	10µF, 50V			

APPLICATIONS INFORMATION

the difference of 40°C divided by 4.48W equals a 9°C/W θ_{JA} thermal resistance. Table 2 specifies a 10°C/W value which is very close. Table 2, Table 3, and Table 4 provide equivalent thermal resistances for 12V, 24V and 36V outputs with and without airflow and heat sinking. The derived thermal resistances in Table 2 to Table 4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four-layer board with two-ounce copper for the two outer layers and one-ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

SAFETY CONSIDERATIONS

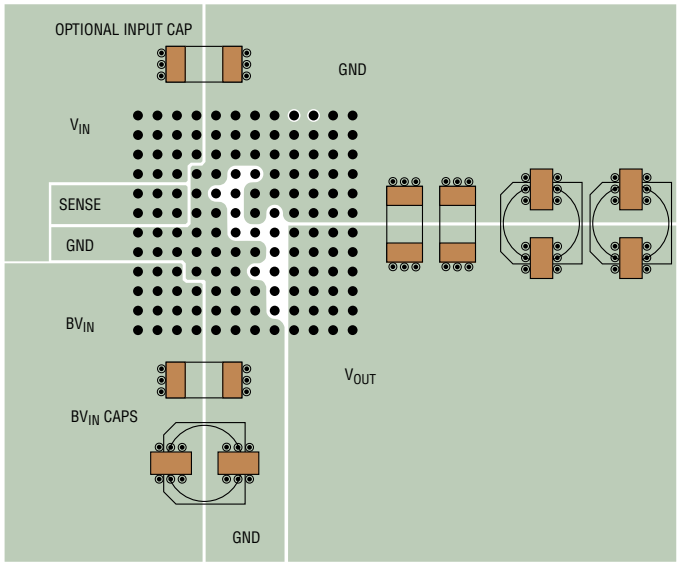
The LTM4656 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. The device does support thermal shutdown and overcurrent protection with retry. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

LAYOUT CHECKLIST/EXAMPLE

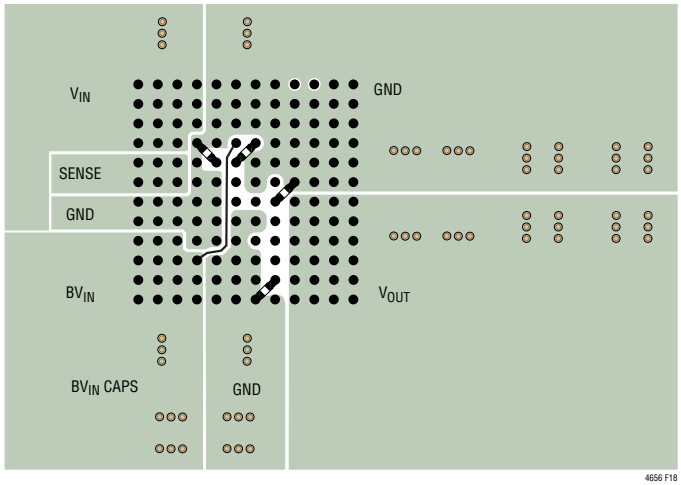
The high integration of LTM4656 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, BV_{IN} GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the BV_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{FB}, COMP, SS, and $\overline{SDHN}$ pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 18 gives a good example of the recommended layout.



(a) TOP LAYER: LTM4656 16mm × 16mm



(b) BOTTOM LAYER: LTM4656 16mm × 16mm

Figure 18. Recommended PCB Layout

TYPICAL APPLICATIONS

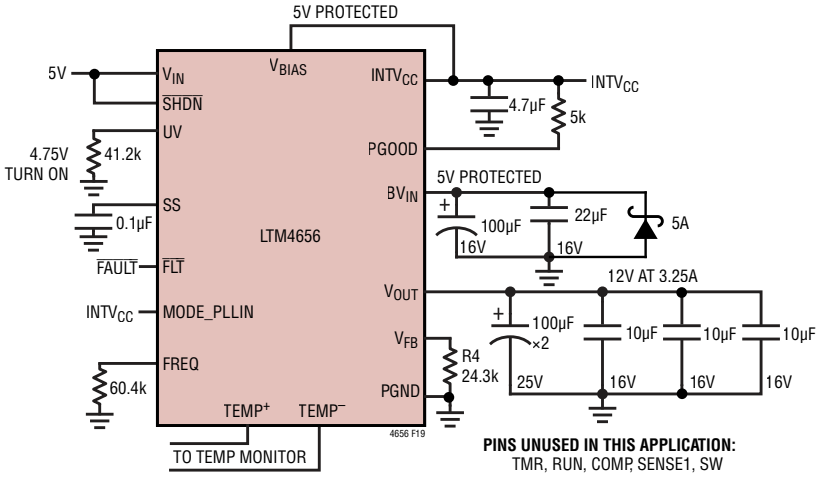
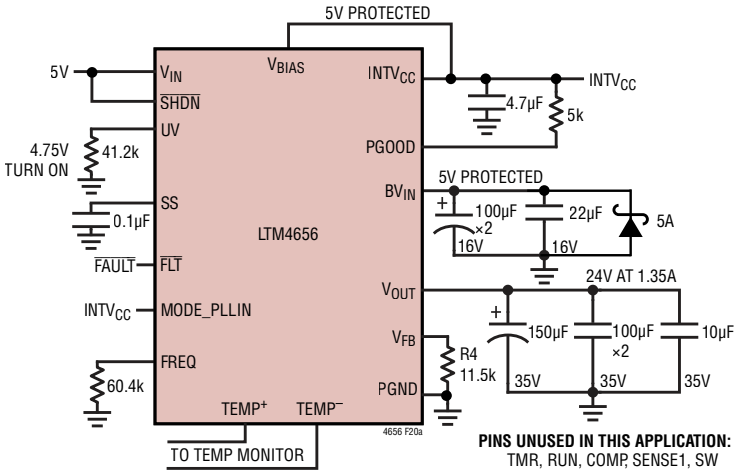
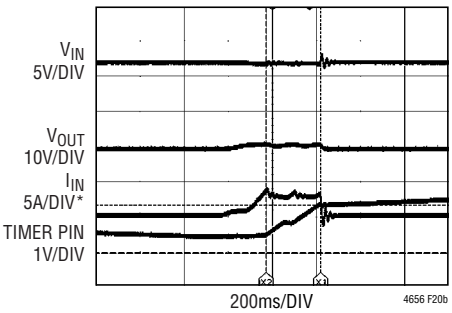


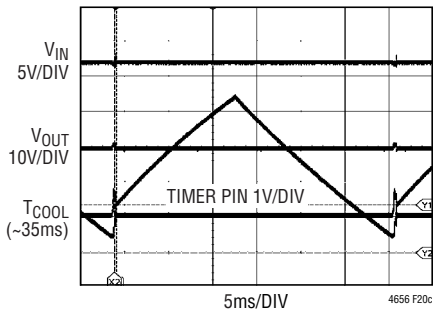
Figure 19. 5V Input to $12V_{OUT}$ at 3.25A Design



Short Circuit Trip



Retry Cycle



*25mV SENSE IN FOLDBACK
TIMER (218µs)

Figure 20. 5V Input to $24V_{OUT}$ at 1.35A Design

TYPICAL APPLICATIONS

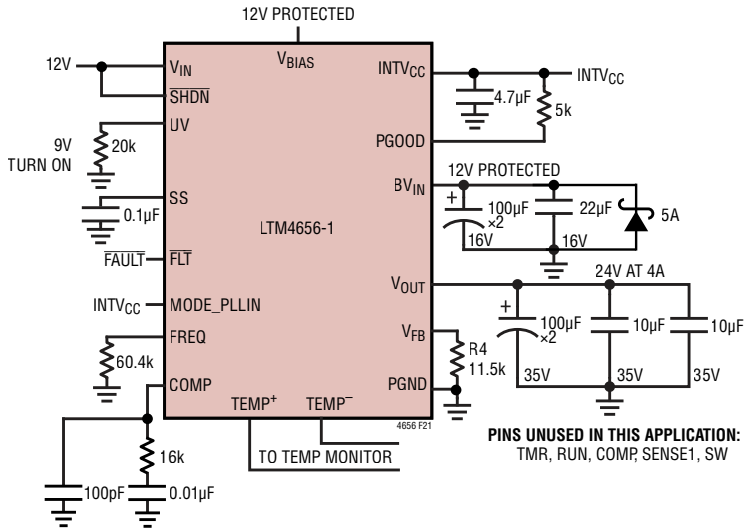


Figure 21. 12V Input to 24V_{OUT} at 4A Design

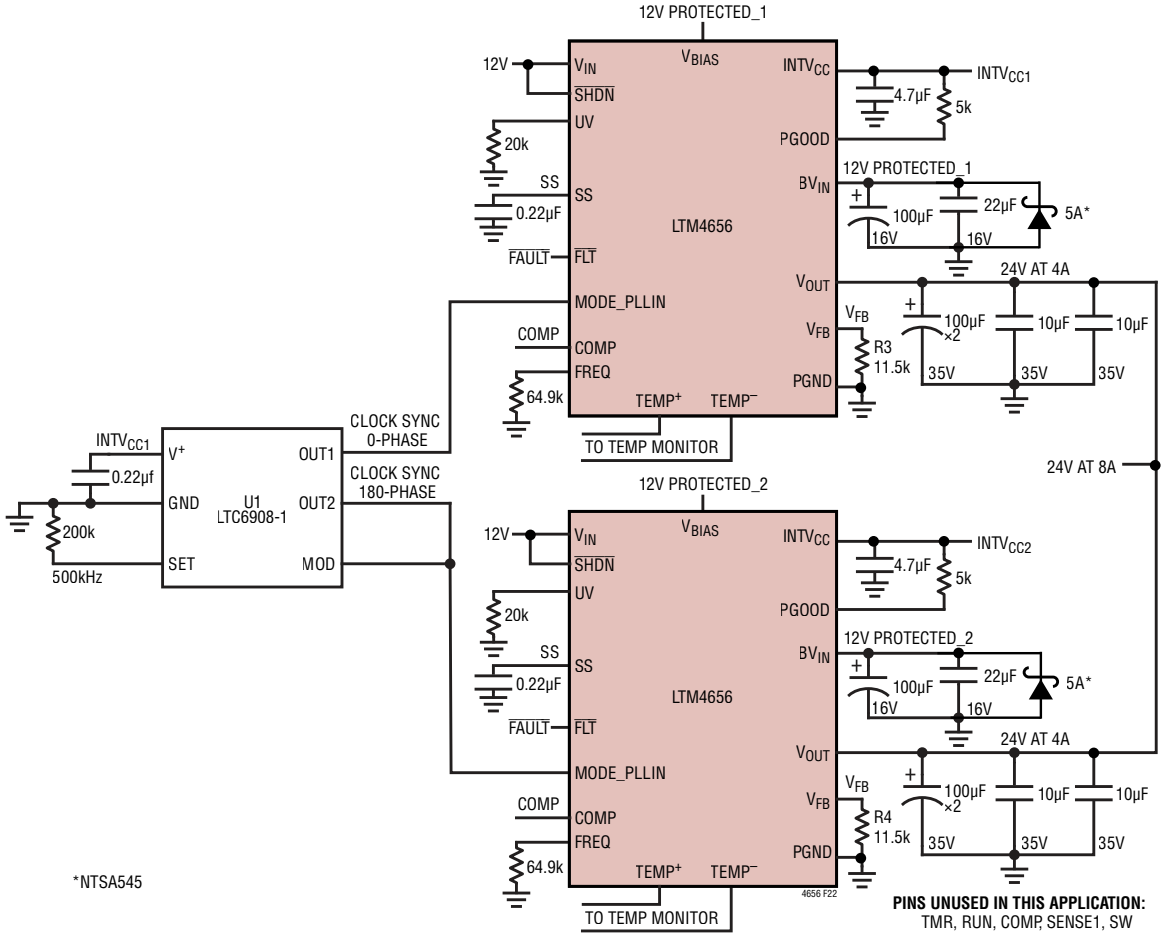


Figure 22. 2-Phase 12V Input to 24V_{OUT} at 8A Design

TYPICAL APPLICATIONS

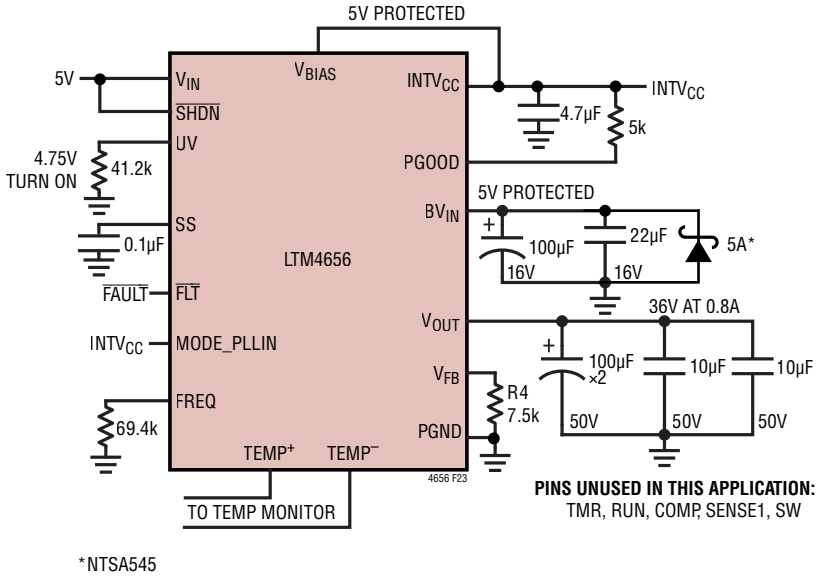


Figure 23. 5V Input to 36V_{OUT} at 0.8A Design

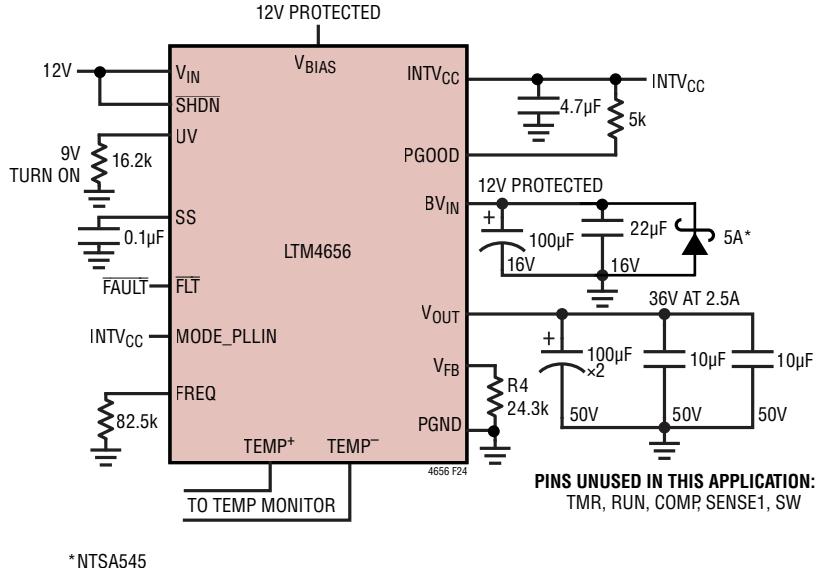


Figure 24. 12V Input to 36V_{OUT} at 2.5A Design

TYPICAL APPLICATIONS

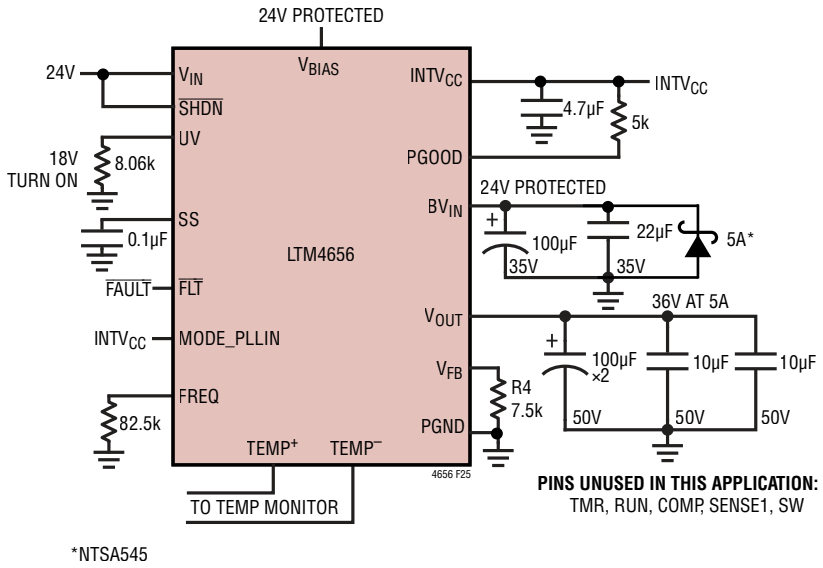


Figure 25. 24V Input to 36V_{OUT} at 5A Design

PIN CONFIGURATION TABLE

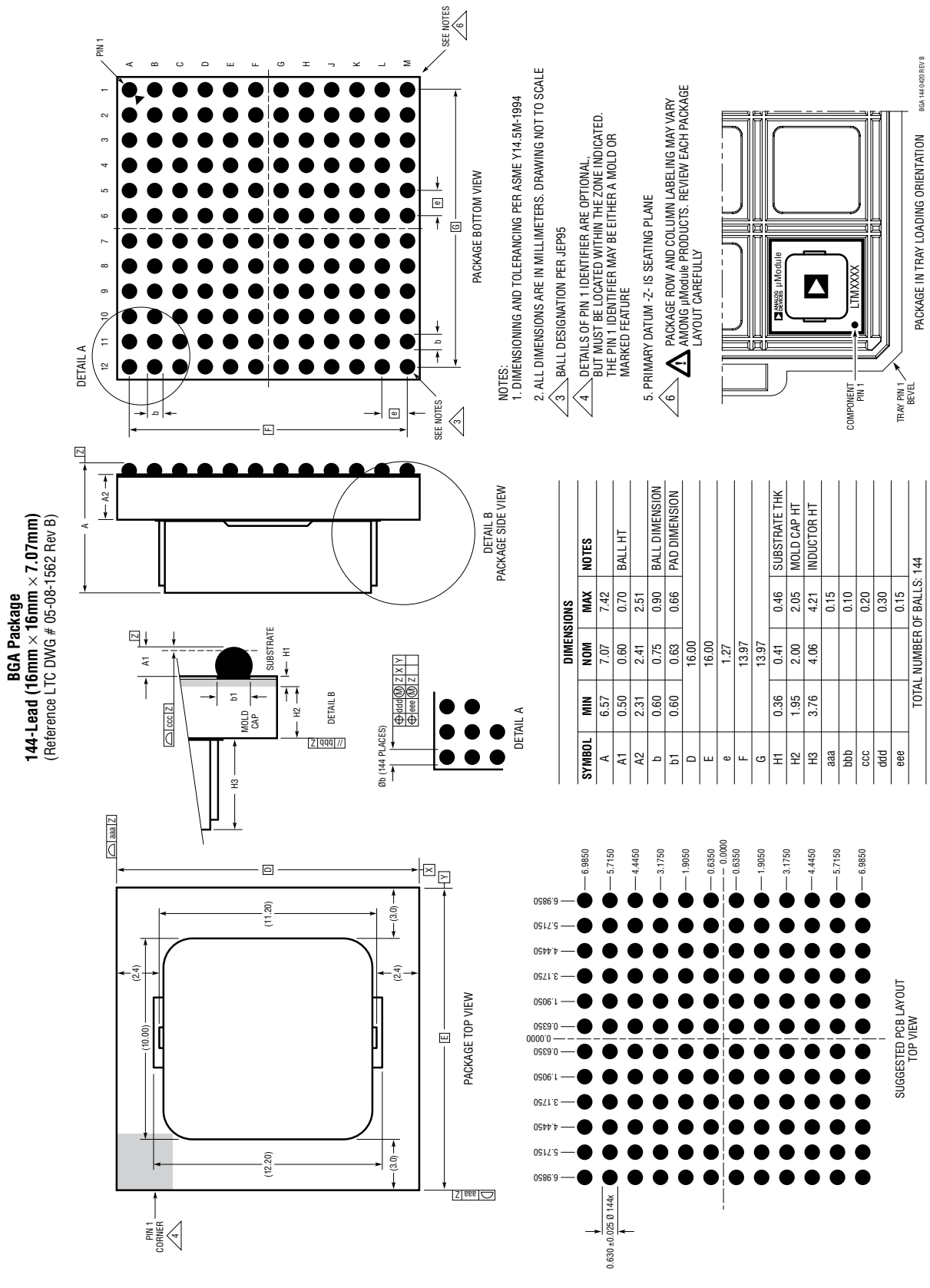
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

LTM4656Y Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	BV_{IN}	B1	BV_{IN}	C1	BV_{IN}	D1	BV_{IN}	E1	GND	F1	$\overline{SHDN}$
A2	BV_{IN}	B2	BV_{IN}	C2	BV_{IN}	D2	BV_{IN}	E2	GND	F2	GND
A3	BV_{IN}	B3	BV_{IN}	C3	BV_{IN}	D3	BV_{IN}	E3	NC	F3	GND
A4	BV_{IN}	B4	BV_{IN}	C4	BV_{IN}	D4	GND	E4	GND	F4	GND
A5	GND	B5	GND	C5	GND	D5	GND	E5	GND	F5	GND
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND	F6	COMP
A7	SENSE1	B7	SENSE1	C7	SENSE1	D7	GND	E7	GND	F7	SS
A8	SENSE1	B8	SENSE1	C8	SENSE1	D8	GND	E8	V_{FB}	F8	PGOOD
A9	V_{IN}	B9	V_{IN}	C9	V_{IN}	D9	GND	E9	GND	F9	V_{BIAS}
A10	V_{IN}	B10	V_{IN}	C10	V_{IN}	D10	V_{IN}	E10	GND	F10	GND
A11	V_{IN}	B11	V_{IN}	C11	V_{IN}	D11	V_{IN}	E11	GND	F11	GND
A12	V_{IN}	B12	V_{IN}	C12	V_{IN}	D12	V_{IN}	E12	GND	F12	GND

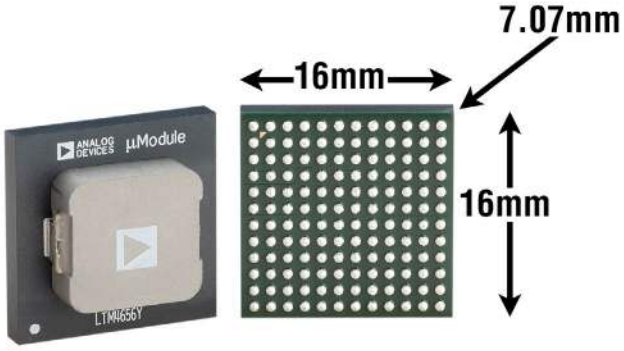
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	V_{OUT}	K1	V_{OUT}	L1	V_{OUT}	M1	V_{OUT}
G2	GND	H2	UV	J2	V_{OUT}	K2	V_{OUT}	L2	V_{OUT}	M2	V_{OUT}
G3	GND	H3	$\overline{FLT}$	J3	V_{OUT}	K3	V_{OUT}	L3	V_{OUT}	M3	V_{OUT}
G4	TMR	H4	$TEMP^{+}$	J4	V_{OUT}	K4	V_{OUT}	L4	V_{OUT}	M4	V_{OUT}
G5	GND	H5	$TEMP^{-}$	J5	V_{OUT}	K5	V_{OUT}	L5	V_{OUT}	M5	V_{OUT}
G6	MODE_PLLIN	H6	FREQ	J6	V_{OUT}	K6	V_{OUT}	L6	V_{OUT}	M6	V_{OUT}
G7	GND	H7	RUN	J7	GND	K7	GND	L7	GND	M7	GND
G8	GND	H8	GND	J8	GND	K8	GND	L8	GND	M8	GND
G9	$INTV_{CC}$	H9	GND	J9	GND	K9	GND	L9	GND	M9	GND
G10	GND	H10	GND	J10	GND	K10	GND	L10	GND	M10	GND
G11	GND	H11	GND	J11	GND	K11	GND	L11	GND	M11	GND
G12	GND	H12	GND	J12	SW	K12	SW	L12	GND	M12	GND

PACKAGE DESCRIPTION

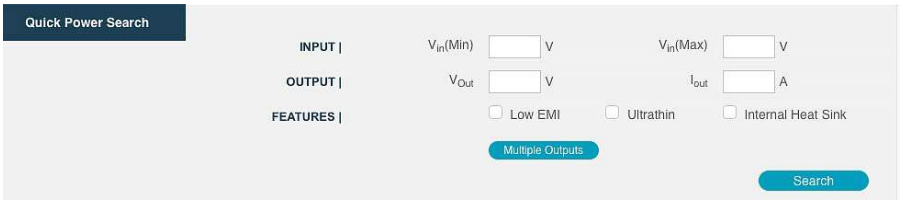


DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	6.57	7.07	7.42	
A1	0.50	0.60	0.70	BALL HT
A2	2.31	2.41	2.51	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		16.00		
E		16.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.36	0.41	0.46	SUBSTRATE THK
H2	1.95	2.00	2.05	MOLD CAP HT
H3	3.76	4.06	4.21	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 144				

PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4661	$5.5V_{IN}$, $15V_{OUT}$, 4A Boost µModule Regulator.	$1.8V \le V_{IN} \le 5.5V$, $2.5V \le V_{OUT} \le 15V$. 6.25mm × 6.25mm × 2.42mm BGA.
LTM4605	$20V_{IN}$, $20V_{OUT}$, 12A Buck-Boost µModule Regulator. External Inductor.	$4.5V \le V_{IN} \le 20V$, $0.8V \le V_{OUT} \le 16V$. 15mm × 15mm × 2.82mm LGA.
LTM4607	$36V_{IN}$, $24V_{OUT}$, 10A Buck-Boost µModule Regulator. External Inductor.	$4.5V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 24V$. 15mm × 15mm × 2.82mm LGA.
LTM4609	$36V_{IN}$, $34V_{OUT}$, 10A Buck-Boost µModule Regulator. External Inductor.	$4.5V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 34V$. 15mm × 15mm × 2.82mm LGA. 15mm × 15mm × 3.42mm BGA.
LTM8054	$36V_{IN}$, $36V_{OUT}$, 5.4A Buck-Boost uModule Regulator. Integrated Inductor.	$5V \le Vin \le 36V$, $1.2V \le V_{OUT} \le 36V$. 11.25mm × 15mm × 3.42mm BGA.
LTM8055	$36V_{IN}$, $36V_{OUT}$, 8.5A Buck-Boost uModule Regulator. Integrated Inductor.	$5V \le V_{IN} \le 36V$, $1.2V \le V_{OUT} \le 36V$. 15mm × 15mm × 4.92mm BGA.
LTM8056	$58V_{IN}$, $48V_{OUT}$, 5.4A Buck-Boost uModule Regulator. Integrated Inductor.	$5V \le V_{IN} \le 58V$, $1.2V \le V_{OUT} \le 48V$. 15mm × 15mm × 4.92mm BGA.