

International IOR Rectifier

- Logic-Level Gate Drive
- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated

• Lead-Free

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	61	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	43	
I_{DM}	Pulsed Drain Current ①⑤	400	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	47	W
	Linear Derating Factor	0.31	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②⑥	390	mJ
I_{AR}	Avalanche Current①⑤	60	A
E_{AR}	Repetitive Avalanche Energy①	4.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	1.2	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

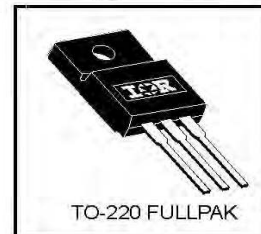
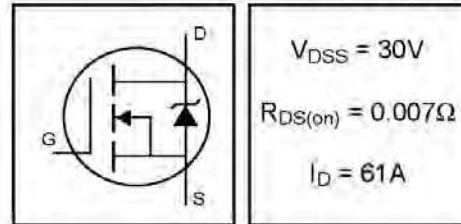
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	65	

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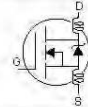
IRL2203NPbF

HEXFET® Power MOSFET



Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.035	—	V/°C	Reference to 25°C , $I_D = 1mA$ ④
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.007	Ω	$V_{GS} = 10V, I_D = 37A$ ④
		—	—	0.01		$V_{GS} = 4.5V, I_D = 31A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	47	—	—	S	$V_{DS} = 25V, I_D = 60A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	110	nC	$I_D = 60A$
Q_{gs}	Gate-to-Source Charge	—	—	31		$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	57		$V_{GS} = 4.5V$, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 15V$
t_r	Rise Time	—	210	—		$I_D = 60A$
$t_{d(off)}$	Turn-Off Delay Time	—	29	—		$R_G = 1.8\Omega, V_{GS} = 4.5V$
t_f	Fall Time	—	54	—		$R_D = 0.25\Omega$, See Fig. 10 ④⑤
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3500	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1400	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	690	—		$f = 1.0MHz$, See Fig. 5⑥
C	Drain to Sink Capacitance	—	12	—		$f = 1.0MHz$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	61	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	400		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 37A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	94	140	ns	$T_J = 25^\circ\text{C}, I_F = 60A$
Q_{rr}	Reverse Recovery Charge	—	280	410	μC	$di/dt = 100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Specification changes

Rev. #	Parameters	Old spec.	New spec.	Comments	Revision Date
1	$V_{GS(th)}$ (Max.)	2.5V	No spec.	Removed $V_{GS(th)}$ Max. Specification	11/1/96
1	V_{GS} (Max.)	± 20	± 16	Decrease V_{GS} Max. Specification	11/1/96

Notes:

- ① Repetitive rating: pulse width limited by max. junction temperature. (See fig. 11)
 ② $V_{DD} = 15V$, starting $T_J = 25^\circ\text{C}$, $L = 220\mu H$
 $R_G = 25\Omega$, $I_{AS} = 60A$. (See Figure 12)

- ③ $I_{SD} \leq 60A$, $di/dt \leq 140A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

- ⑤ $t = 60s$, $f = 60Hz$

- ⑥ Uses IRL2203N data and test conditions

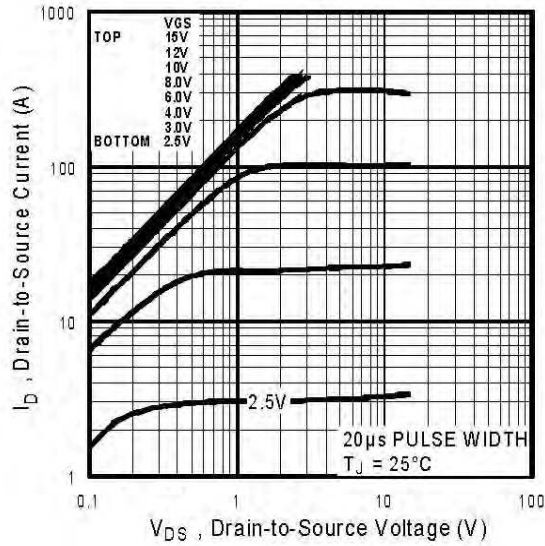


Fig 1. Typical Output Characteristics

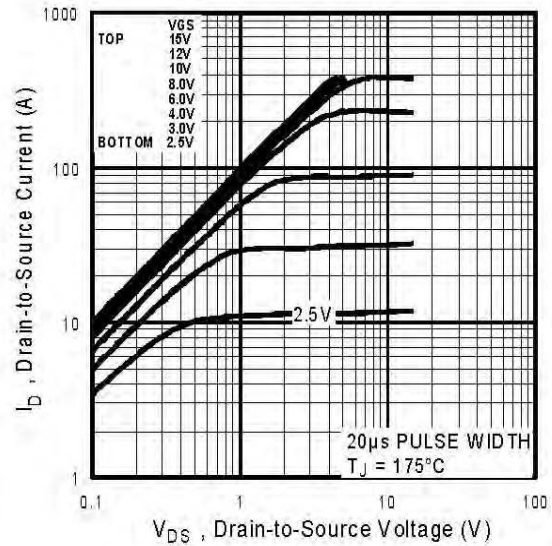


Fig 2. Typical Output Characteristics

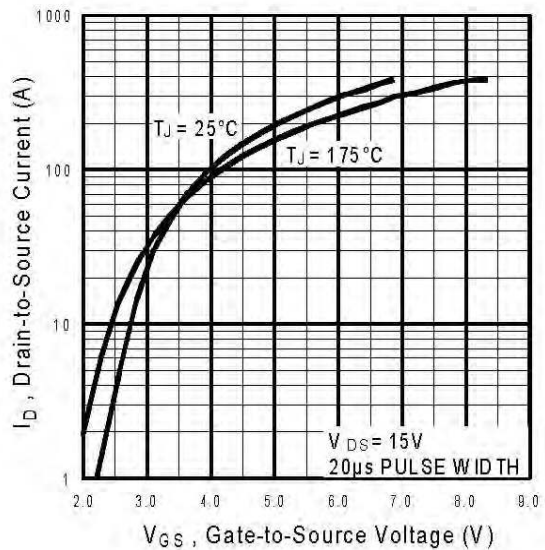


Fig 3. Typical Transfer Characteristics

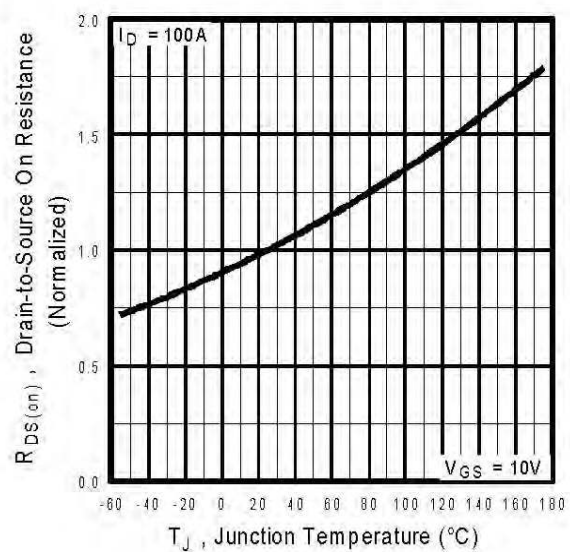


Fig 4. Normalized On-Resistance Vs. Temperature

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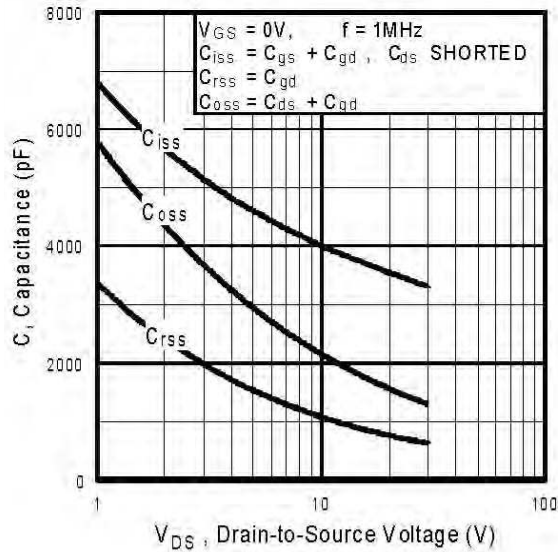


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

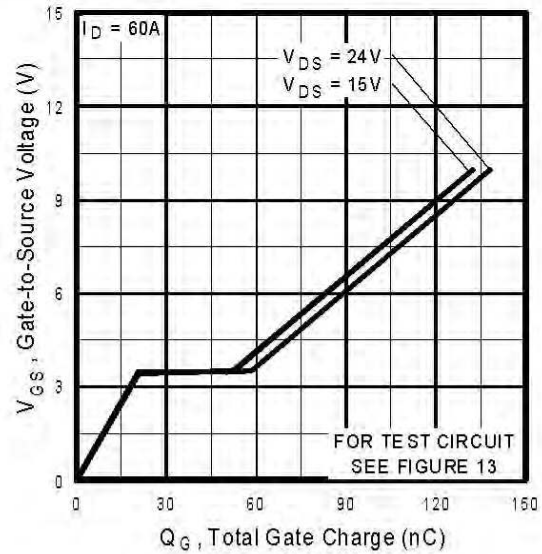


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

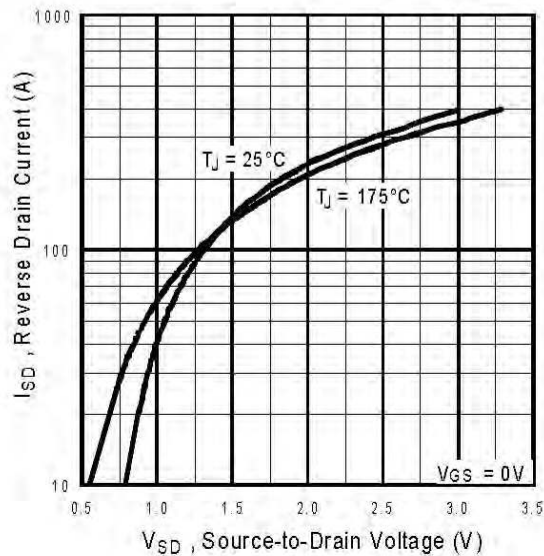


Fig 7. Typical Source-Drain Diode Forward Voltage

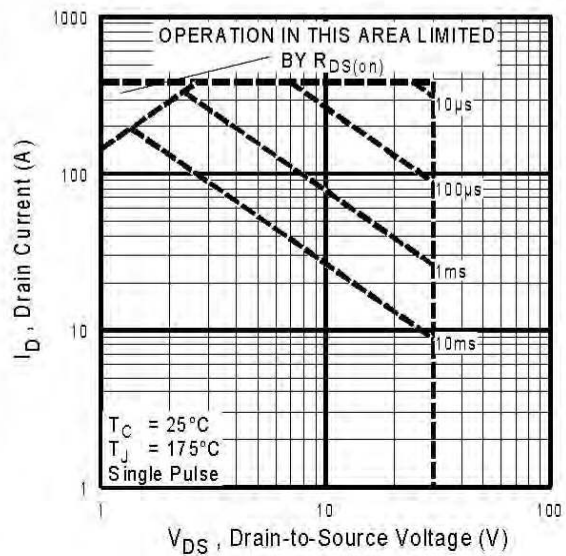


Fig 8. Maximum Safe Operating Area

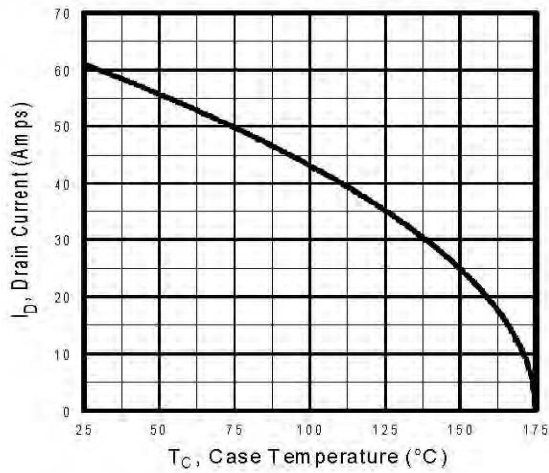


Fig 9. Maximum Drain Current Vs. Case Temperature

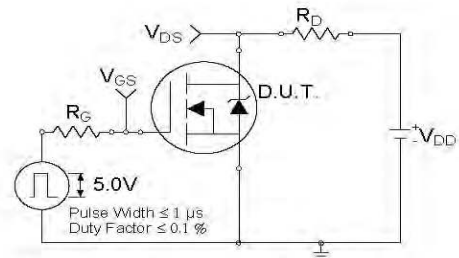


Fig 10a. Switching Time Test Circuit

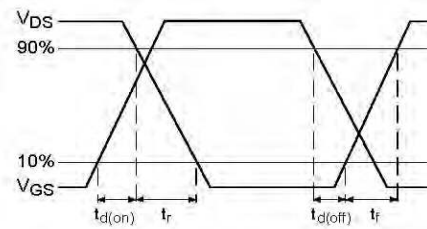


Fig 10b. Switching Time Waveforms

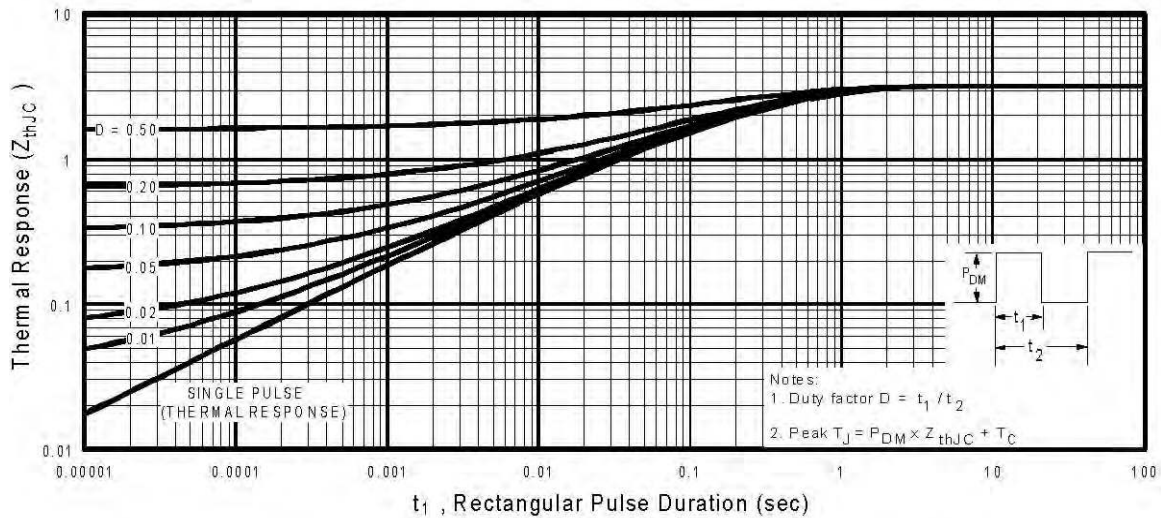


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

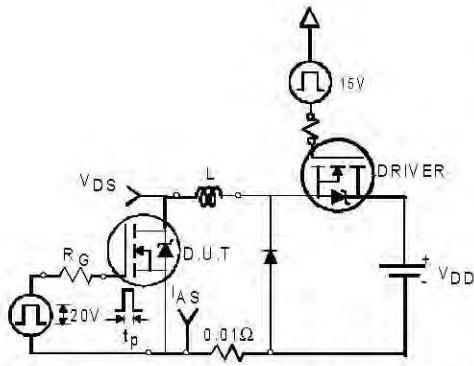


Fig 12a. Unclamped Inductive Test Circuit

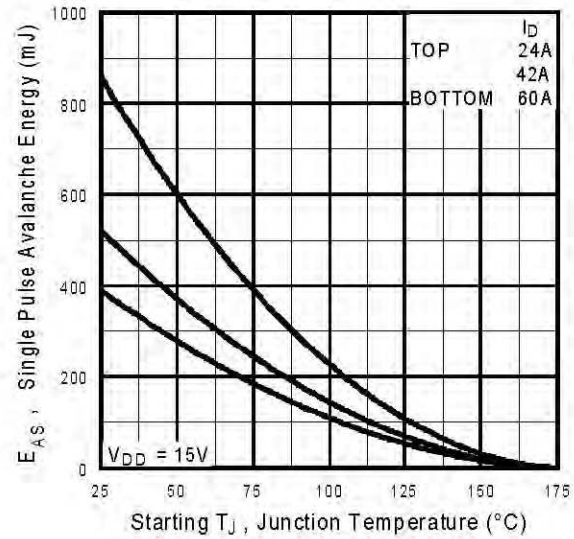


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

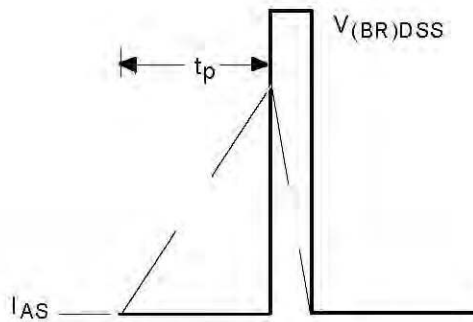


Fig 12b. Unclamped Inductive Waveforms

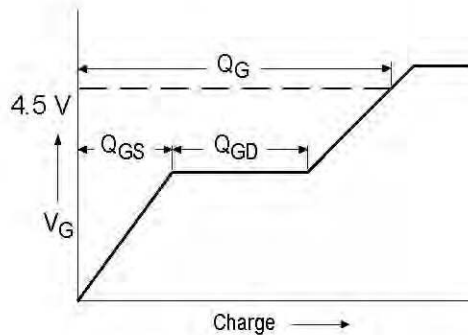


Fig 13a. Basic Gate Charge Waveform

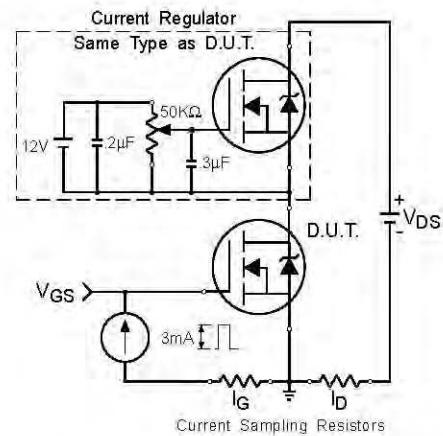
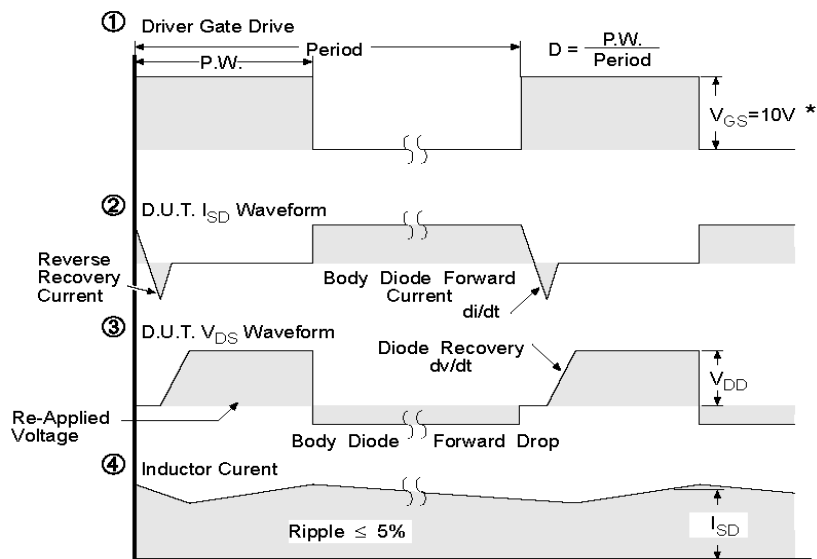
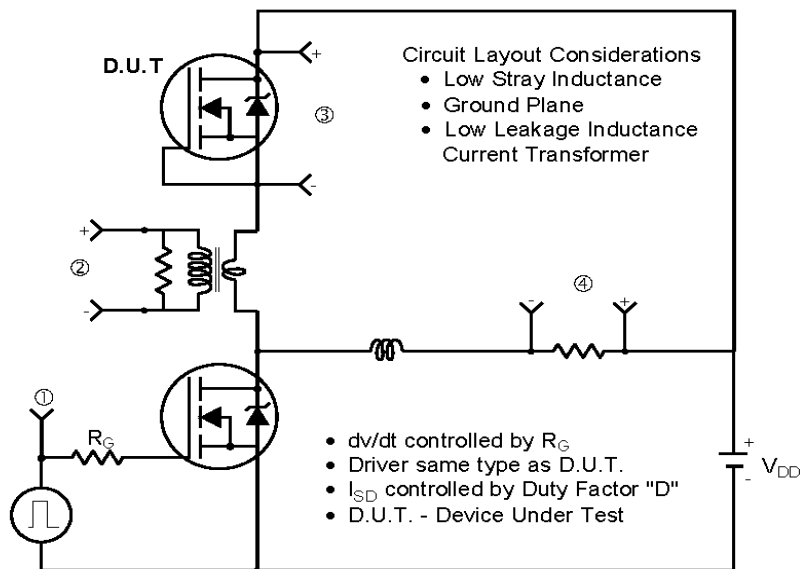


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

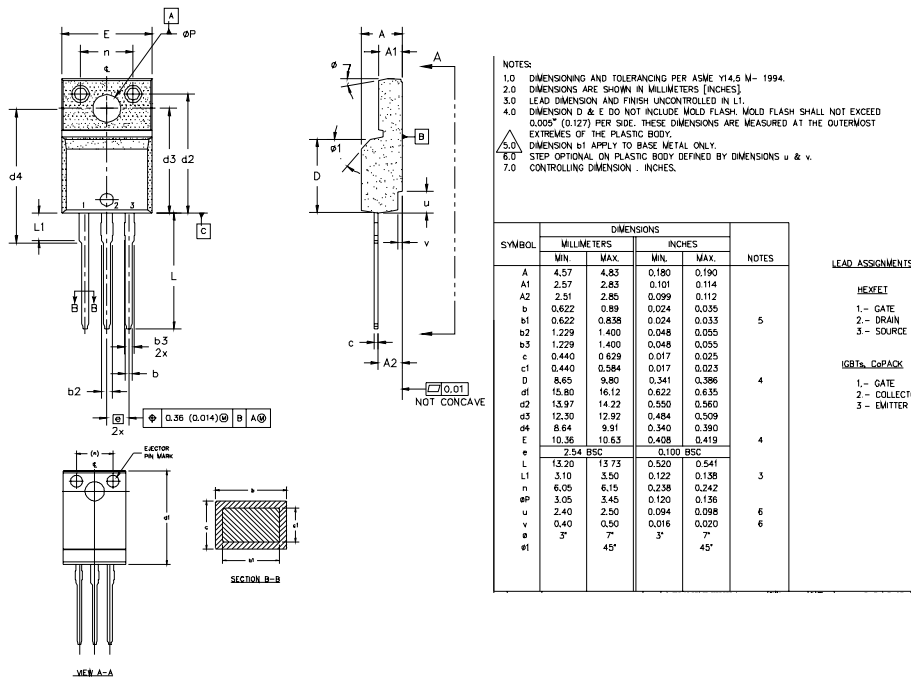
Fig 14. For N-Channel HEXFETS

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TO-220 Full-Pak Package Outline

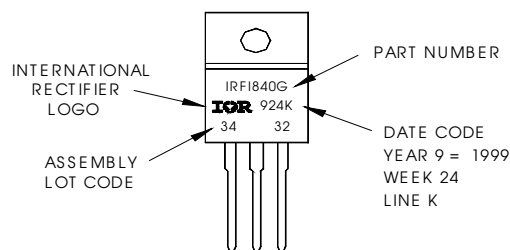
Dimensions are shown in millimeters (inches)



TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

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Note: For the most current drawings please refer to the IR website at:
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