Product Brief
June 2008
Revision 1.2

WPC8765L / WPC8769L Mobile Embedded Controller with SPI™ Flash Interface and MC-Compliant CIR Port (Revisions A4 and A5)

General Description

The Nuvoton WPC8765L and WPC8769L are highly integrated embedded controllers (EC) with an embedded RISC core and integrated advanced functions. They are targeted for a wide range of portable applications.

The WPC8765L/WPC8769L incorporate the CompactRISC® CR16CPlus core (a high-performance 16-bit RISC processor), on-chip ROM and RAM memories, system support functions and a Flash Interface Unit (FIU) that interfaces directly with external SPI flash memory devices.

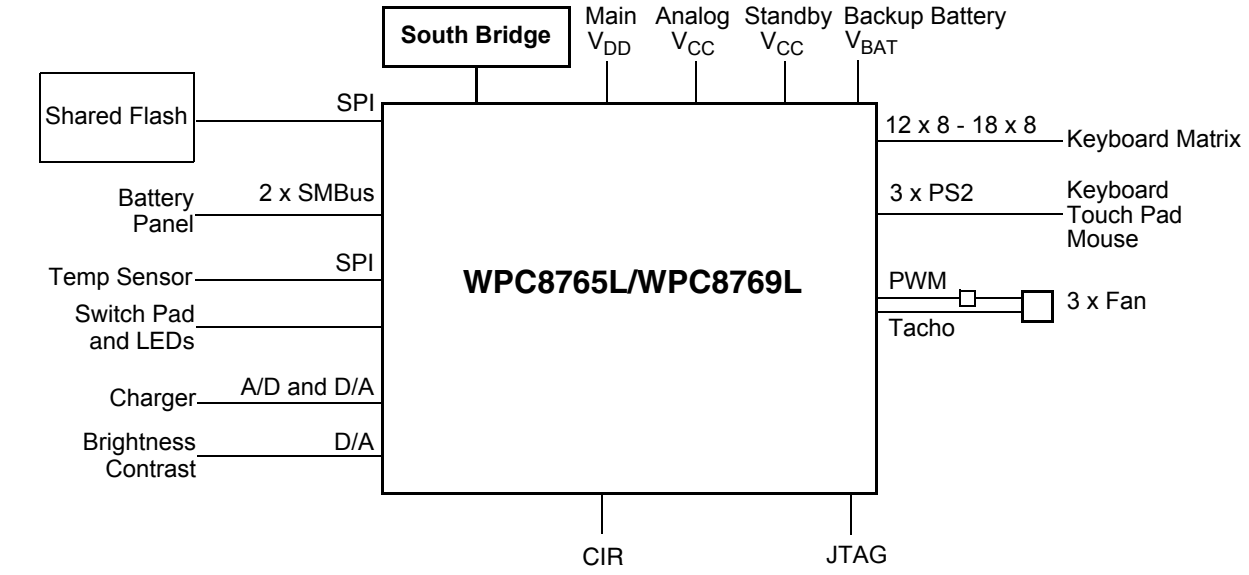
System support functions include: watchdog, PWM, timers, interrupt control, General-Purpose I/O (GPIO) with internal keyboard matrix scanning, PS/2® interface, SMBus® interface, UART, SPI™, high-accuracy analog-to-digital (ADC) and digital-to-analog (DAC) converters for battery charging, system control, system health monitoring and analog controls, and a SensorPath™ interface.

The WPC8765L/WPC8769L interface with the host via an LPC interface.The WPC8765L/WPC8769L are PC01 and ACPI compliant, and offer a single-chip solution for the most commonly used notebook PC I/O peripherals.

Outstanding Features

- Shared BIOS flash memory
- Support for SPI flash memories
- Flash page programing support
- MC-compliant Consumer Infrared (CIR) Port
- High-accuracy, high-speed ADC
- Up to 88 GPIO ports (including keyboard scanning) with a variety of wake-up events
- 16-bit RISC core, with up to 4 Mbytes of external address space, running at up to 25 MHz
- 128-pin LQFP package

System Block Diagram



Device-Specific Information

The following table shows the main differences between Revisions A4 and A5 of the WPC8765L and WPC8769L device.

Feature	Revision A4		Revision A5
	WPC8765L	WPC8769L	WPC8769LA0
ADC Resolution	10 bit	8 bit	8 bit
PWM Outputs	3		8

Features

Embedded Controller Features

- Processing Unit
  - CompactRISC CR16CPlus 16-bit embedded RISC processor core (the "core")
  - Up to 4 Mbytes of external address space
- Internal Memory
  - 1 Kbyte of ROM
  - 4 Kbytes of on-chip RAM
  - All memory types can hold both code and data
- Flash Interface Unit (FIU)
  - Up to 4 Mbytes of code and data
  - Hardware-protected boot zone block protection
  - SPI External Memory
    - ❏ Up to 32 Mbits
    - ❏ Fast Read mode
    - ❏ Page programing support
    - ❏ Configurable clock rate
  - Field upgradeable
- Shared Memory Controller (SHM)
  - Supports BIOS (flash) memory sharing with PC host
  - Supports host-controlled code download and update
  - Memory access protection

LPC System Interface

- Based on Intel's *LPC Interface Specification Revision 1.1*, August 2002
- Four optional 8-bit DMA channels
- I/O, Memory and 8-bit Firmware Memory read and write cycles, Firmware Memory writes may insert wait cycles
- Bootable Memory Support
- Base Address (BADDR1-0) straps to determine the base address of the index-data register pair
  - Alternate base address configurable by the core
- $\overline{\text{LPCPD}}$ and $\overline{\text{CLKRUN}}$ support

Embedded Controller System Features

- Host Interface
  - Comprises host interface channels, typically used for KBC and ACPI Private or Shared EC channels
  - 8042 KBC-standard interface (legacy 60h, 64h)
  - Two PM interface ports (legacy 62h, 66h; 68h, 6Ch)
  - ACPI EC with either Shared or Private interface through the PM interface
  - Two Mailbox areas for host-core communication, up to 4 Kbytes each; maximum 4 Kbytes total
  - Generates IRQ, SMI and SCI
  - Provides IRQ1 and IRQ12 support
  - Provides Fast Gate A20 and Fast Host reset via firmware
- Interrupt Control Unit (ICU)
  - 31 maskable vectored interrupts (of which eight are external)
  - General-purpose external interrupt inputs through MIWU
  - Enable and pending indication for each interrupt
  - Non-maskable interrupt input
- Multi-Input Wake-Up (MIWU)
  - Up to 40 wake-up or interrupt inputs
  - Generates wake-up event to PMC (Power Management Controller)
  - Generates interrupts to ICU
  - User-selectable trigger conditions
- Internal Keyboard Matrix Scanning
  - Up to 18 open-collector outputs (at least 12)
  - Eight Schmitt inputs with internal pull-ups
- General-Purpose I/O (GPIO) Ports
  - 64 port pins
  - I/O pins individually configured as input or output
  - Configurable internal pull-up / pull-down resistors
  - Outputs individually configured as push-pull or open-drain
  - Two echo inputs with wake-enabled interrupts
  - Additional 12 GPIOs with wake-enabled interrupts
  - Four GPIOs capable of 20 mA sink current
  - Seven GPIOs are accessible to the host
  - Optional low-cost external GPIO expansion through the SensorPath interface
- PS/2 Interface
  - Three external ports: can be used for keyboard, mouse and an additional pointing device
  - Byte-level handling via hardware accelerator

Features (Continued)

- Two SMBus (SMB) Interface Modules; each module:
  - Is Intel SMBus, Philips I²C® and ACCESS.bus compatible
  - Is SMBus master and slave
  - Supports up to two simultaneous slave addresses
  - Supports polling- and interrupt-controlled operations
  - Generates a wake-up signal on detection of a Start condition while in Idle mode
  - Supports an optional internal pull-up on SDA and SCL pins
- Core Universal Asynchronous Receiver-Transmitter (CR_UART) Module
  - A full-duplex UART channel
  - Programmable baud rate
  - Data transfer via interrupt or polling
- Two 16-bit Multi-Function Timer (MFT16) Modules; each module has:
  - Two 16-bit timers with a 5-bit prescaler
  - Pulse Width Modulation (PWM), Capture and Timer/Counter modes
  - Capture inputs with programmable edge detection
  - An interrupt on compare match
- Two Pulse Width Modulation (PWM) Modules
  - Group A_PWM: two outputs in Rev. A4; four outputs in Rev. A5
  - Group B_PWM: one output in Rev. A4; four outputs in Rev. A5
- Serial Peripheral Interface (SPI) Module
  - Bus master
  - 8-bit interface
  - Up to 10 MHz data clock rate
  - Clock can be selected to be high or low in Idle mode
  - Clock polarity can be selected for normal (sample on rising edge) or alternate (sample on falling edge)
- Timer and Watchdog (TWD)
  - 16-bit periodic interrupt timer with 30 μs resolution and 5-bit prescaler for system tick and periodic wake-up tasks
  - 8-bit watchdog timer with enable/disable
  - "Watchdog occurred" flag
  - Two watchdog reset options: warm or cold
- SensorPath™ Bus Interface
  - Single Wire bus master
  - Supports up to seven slave devices
  - x1, x4 SensorPath clock rate support
- Analog-to-Digital Converter (ADC)
  - Six channels, with 8/10-bit resolution (10-bit resolution **only in WPC8765L**)
  - 125 μs conversion time
  - External voltage reference
- Digital-to-Analog Converter (DAC)
  - Four channels, 8-bit resolution
  - 1 μs conversion time for 50 pF load
  - Full output range from AGND to AVCC
- Development Support
  - Interface to debugger via Nexus 5001 interface
    - ❏ Physical connection using JTAG
    - ❏ On-board Debug mode with eight hardware breakpoints
    - ❏ Embedded memory programing via JTAG with content read protection
- Core Access to Host Modules
  - Enabled via lock mechanism

Host Function Features

- Mobile System Wake-Up Control (MSWC)
  - Software-controlled off events
  - Event routing to IRQ, $\overline{\text{SMI}}$ or $\overline{\text{PWUREQ}}$
- Host- or Core-Controlled CEIR (Consumer Electronic IR) Receiver
  - Supports RC-5, RC-6 and NEC protocols
  - Wake-up on a pre-configured message
- Infrared Port
  - Supports IR learning and emitting
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - HP-SIR
  - ASK-IR option of SHARP-IR
  - DASK-IR option of SHARP-IR
  - Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
- Serial Port (SP2)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud
- Supports *Microsoft® Advanced Power Management (APM) Specifications Revision 1.2*, February 1996
  - Generates the System Management Interrupt (SMI)
- PC01 Rev 1.0 and ACPI 3.0 Compliant
  - PnP configuration register structure
  - Flexible resource allocation for all logical devices
    - ❏ Relocatable base address
    - ❏ 15 IRQ routing options
    - ❏ Four optional 8-bit DMA channels (where applicable)

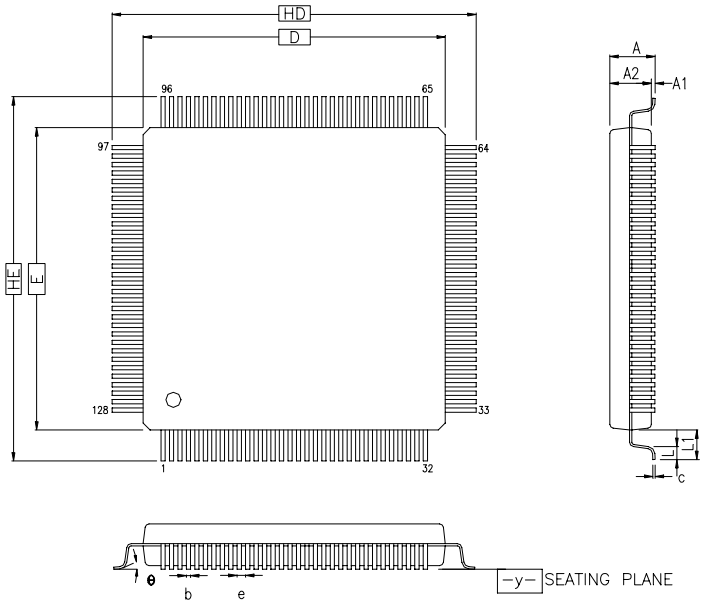
Features (Continued)

Clocking, Supply and Package Information

- Strap Input-Controlled Operating Modes:
  - Shared BIOS memory mode
  - TRI-STATE® mode
  - Development mode
- Clocks
  - Single 32.768 KHz crystal oscillator
  - On-chip high-frequency clock generators
  - Either 32.768 KHz or CR16CPlus clock out
- Testability
  - XOR-tree structure includes all device pins (except supply, A/D, D/A, and crystal oscillator pins), selected at power-up by strap inputs
  - TRI-STATE device pins, selected at power-up by strap input ($\overline{TRIS}$)
- Power Supply
  - 3.3V supply operation
  - 5V tolerance and back-drive protection on all pins (except crystal oscillator, A/D, D/A, LPC bus, and SPI flash pins)
  - Separate supply for host I/F (V_{DD}) and EC functions (V_{CC})
  - Backup battery input for wake-up configuration
  - Reduced power consumption capability
  - Software- or hardware-switched power modes:
    - Active mode
    - Active mode executing WAIT
    - Idle
    - Deep Idle
    - Suspend
    - Power Off, for oscillator only, from the backup battery
  - Automatic wake-up on system events
- Package Options
  - 128-pin LQFP package

Physical Dimensions

Control dimensions are in millimeters



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

128-Pin Low-Profile Plastic Quad Flatpack (LQFP)
Order Number: WPC8765LDG / WPC8769LDG for Rev. A4, WPC8769LA0DG for Rev. A5

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