QUALITY
SEMICONDUCTOR, INC.

3.3V SYNC DRAM PLL Clock Driver

QS5920A

FEATURES/BENEFITS

- Intel PC100/Spread Spectrum compliant
- 11 outputs
- Balanced Drive Outputs ±12mA
- Synchronous output enable ($\overline{sOE}$) control for SDRAM power down mode
- External feedback, internal loop filter
- Low skew guaranteed between outputs
- Supports 33MHz to 100MHz SDRAMs
- JEDEC compatible LVTTL
- 3.0V to 3.6V supply voltage
- Industrial temperature range
- Inputs are 5V tolerant
- Available in 16- and 24-pin QSOP packages

DESCRIPTION

The QS5920A is a high-performance, low skew, low jitter, multiple output phase-locked loop clock driver which is suitable for PC-100 spread spectrum clock systems. It provides precise phase and frequency alignment of its clock outputs to an externally applied clock input signal. The QS5920A has been specially designed to interface with high speed SDRAM applications in the range of 33MHz to 100MHz and includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. The synchronous output enable ($\overline{sOE}$) control sets all outputs except QFB (which may be used to maintain phase lock) LOW on a subsequent negative clock transition: partial output clock pulses are not produced.

Figure 1. Logic Block Diagram

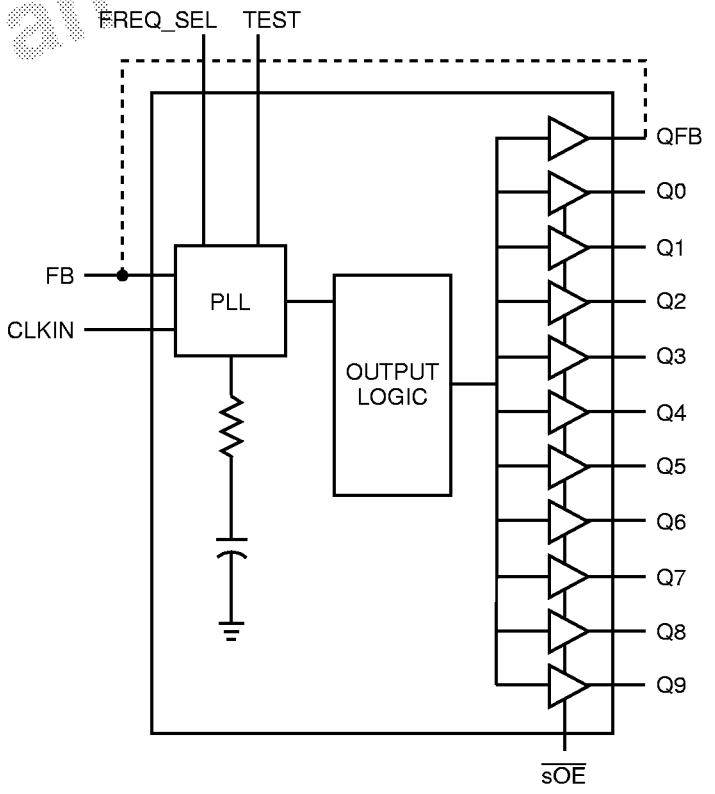


Figure 2. Pin Configuration (All Pins Top View)

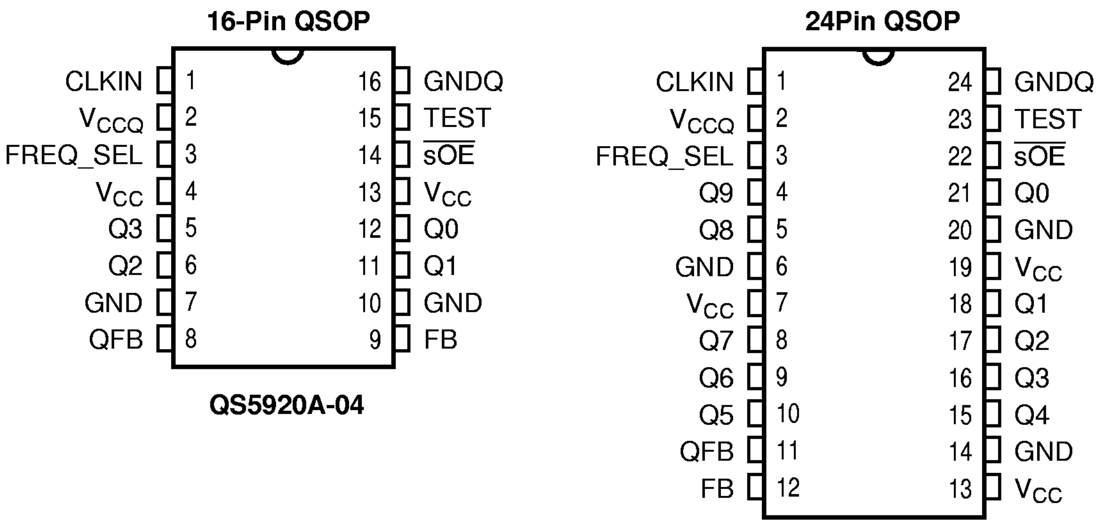


Table 1. Pin Description

Pin Name	I/O	Functional Description
CLKIN	I	Clock input
Q0..Q9	O	Clock outputs
FB	I	PLL feedback input normally connected to QFB by user. May be connected to any output if $\overline{sOE}$ is strapped low.
QFB	O	Dedicated clock output for the FB pin (non-disable)
$\overline{sOE}$	I	Synchronous output enable. Asserted LOW for normal operation. When asserted HIGH, clock outputs (except QFB) are forced LOW.
TEST	I	When LOW, PLL is in normal operation. When HIGH, it disables PLL and opens DC bypass. CLKIN goes to all outputs.
FREQ_SEL(1)	I	VCO frequency select. For optimizing the VCO operating frequency. Set LOW for input frequencies within 33MHz to 75MHz, and HIGH for 66MHz to 100MHz.
V_{CC}	—	Power supply for output buffers
V_{CCQ}	—	Power supply (quiet) for PLL
GND	—	Ground supply for output buffers
GNDQ	—	Ground supply (quiet) for PLL

Note:
1. If this input is switched, the function and timing of the outputs may glitch, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Output Voltage V_{OUT}	–0.5V to V_{CC} + 0.5V
DC Input Voltage V_{IN}	–0.5V to 7.0V
DC Input Diode Current with $V_I < 0$	–20mA
Maximum Power Dissipation At T_A = 85°C,	0.55W
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

Pins	QSOP		Units
	Typ	Max	
C_{IN}	5	7	pF

Note: Capacitance is characterized but not tested.

Table 4. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power Supply Voltage	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 5. DC Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Condition	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for inputs	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for inputs			0.8	V
V_{IC}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		–0.7	–1.2	V
V_{OH}	Output HIGH Voltage (Q0:9, QFB)	V_{CC} = Min., I_{OH} = –12mA V_{CC} = Min., I_{OH} = –8mA V_{CC} = Min., I_{OH} = –100µA	2.0 2.4 2.8			V
V_{OL}	Output LOW Voltage (Q0:9, QFB)	V_{CC} = Min., I_{OL} = 12mA V_{CC} = Min., I_{OL} = 8mA V_{CC} = Min., I_{OL} = 100µA			0.5 0.4 0.2	V
$\lvert I_{IN} \rvert$	Input Leakage Current	V_{CC} = Max., 0 ≤ V_{IN} ≤ V_{CC}			1	µA

Note:

1. Typical values indicate V_{CC} = 3.3V and T_A = 25°C.

Table 6. Power Supply Characteristics

Symbol	Parameter	Test Conditions	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., TEST = High, CLKIN = Low $\overline{sOE}$ = Low, All outputs unloaded	15	30	mA
ΔI_{CC}	Power Supply Current Per Input HIGH(1)	V_{CC} = Max., V_{IN} = 3.0V	1.0	30	µA
I_{CCD}	Dynamic Power Supply Current Per Output(1)	V_{CC} = Max., C_L = 0pF	55	90	µA/ MHz
I_C	Total Power Supply Current(1)	V_{CC} = 3.3V, f_{CLKIN} = 50MHz(2)	70		mA
		V_{CC} = 3.3V, f_{CLKIN} = 100MHz(2)	130		

Notes:

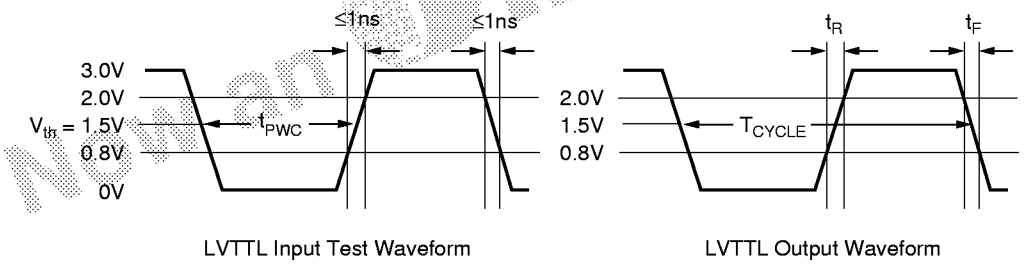
1. Guaranteed by characterization but not production tested.
2. For 11 outputs each loaded with 15pF.

Table 7. Switching Characteristics Over Operating Range

Symbol	Description	Min	Max	Unit
t_{PWC}	Input clock pulse, high or low(1)	2.5	—	ns
f_{CLKIN}	Input frequency	33	100	MHz
t_{PD}	CLKIN input to FB delay, 100MHz(1)	–250	250	ps
t_{SK1}	Output - Output skew, all outputs, same transition,100MHz(1,5)	—	200	ps
t_J	Cycle to cycle jitter, 100MHz(1)	–100	100	ps
$t_{J\ (SSC)}$	Spread Spectrum Clock induced skew, 100MHz(1,3)	–200	200	ps
t_{PW}	Output duty cycle distortion(1,2)	45	55	%
t_{OPW}	Output pulse width distortion(1,2)	$T_{CYCLE}/2 - 0.65$	$T_{CYCLE}/2 + 0.65$	ns
t_{LOCK}	CLKIN to phase lock	0.1	0.5	ms
t_R,t_F	Output rise and fall times (0.8V to 2.0V)(1)	—	1.6	ns
t_{DEV}	Skew between two outputs of different devices(1,4)	—	1.00	ns

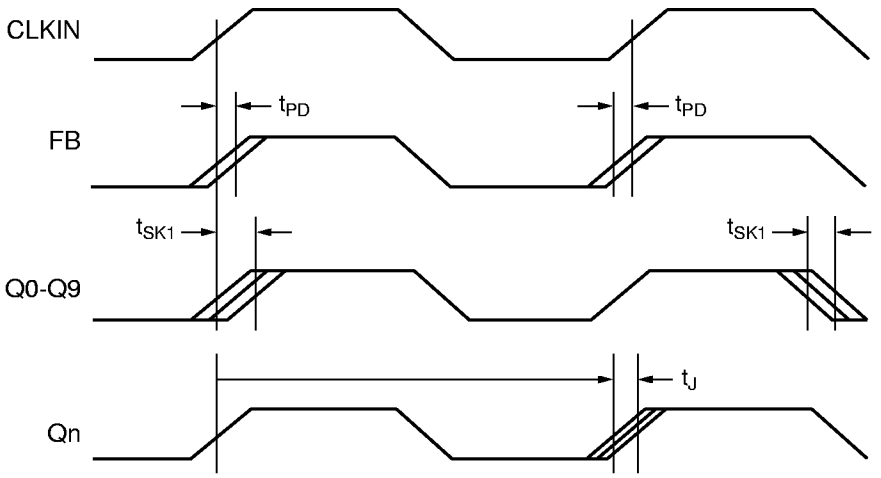
Notes:
1. This parameter is guaranteed by design and verified during production by statistical correlation.
2. Output signal is nominally 50% duty cycle: maximum error is ±5% of the period or 0.65ns, whichever is the greater.
3. Spread spectrum clock induced skew is measured under PC-100 conditions of 30kHz to 50kHz modulation with peak deviation of –0.5%.
4. t_{DEV} applies to any device operating under the same conditions (V_{CC}, ambient temperature, package, air flow, etc.)
5. All outputs with 15pF Load.

Figure 3. Waveforms



LVTTL Input Test Waveform — LVTTL Output Waveform

Figure 4. AC Timing Diagram



Ordering Information