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FAIRCHILD SEMICONDUCTOR®

January 2014

FDD1600N10ALZ

N-Channel PowerTrench® MOSFET

100 V, 6.8 A, 160 mΩ

Features

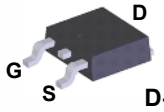
- $R_{DS(on)}$ = 124 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 3.4 A
- $R_{DS(on)}$ = 175 mΩ (Typ.) @ V_{GS} = 5 V, I_D = 2.1 A
- Low Gate Charge (Typ.2.78 nC)
- Low C_{rss} (Typ. 2.04 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Description

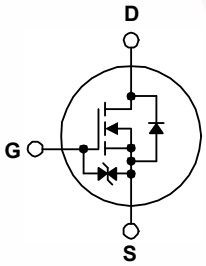
This N-Channel MOSFET is produced using Fairchld Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance and maintain superior switching performance.

Application

- Consumer Appliances
- LED TV and Monitor
- Synchronous Rectification
- Uninterruptible Power Supply
- Micro Solar Inverter



D-PAK



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FDD1600N10ALZ	Unit
V_{DSS}	Drain to Source Voltage			100	V
V_{GSS}	Gate to Source Voltage			±20	V
I_D	Drain Current	- Continuous (T_C = 25°C)		6.8	A
		- Continuous (T_C = 100°C)		4.3	
I_{DM}	Drain Current	- Pulsed	(Note 1)	13.6	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	5.08	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)		14.9	W
		- Derate Above 25°C		0.12	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FDD1600N10ALZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	8.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	87	

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD1600N10ALZ	1600N10ALZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.1	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_C = 125°C	-	-	500	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.4	-	2.8	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 3.4 A	-	124	160	mΩ
		V_{GS} = 5 V, I_D = 2.1 A	-	175	375	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 6.8 A	-	19.6	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	-	169	225	pF
C_{oss}	Output Capacitance		-	43	55	pF
C_{rss}	Reverse Transfer Capacitance		-	2.04	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		85	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{GS} = 10 V; V_{DD} = 50 V, I_D = 6.8 A	-	2.78	3.61	nC
$Q_{g(tot)}$	Total Gate Charge at 5V	V_{GS} = 5 V; V_{DD} = 50 V, I_D = 6.8 A		1.5	1.95	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50 V, I_D = 6.8 A (Note 4)	-	0.72	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	0.56	-	nC
$V_{plateau}$	Gate Plateau Volatge		-	4.02	-	V
Q_{sync}	Total Gate Charge Sync.	V_{DS} = 0 V, I_D = 3.4 A	-	2.5	-	nC
Q_{oss}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V	-	5.2	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz	-	2.1	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 6.8 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	-	7	24	ns
t_r	Turn-On Rise Time		-	2	14	ns
$t_{d(off)}$	Turn-Off Delay Time		-	13	36	ns
t_f	Turn-Off Fall Time		-	2	14	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6.8	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	13.6	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 6.8 A	-	-	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 6.8 A, V_{DS} = 50 V, dI_F/dt = 100 A/μs	-	37	-	ns
Q_{rr}	Reverse Recovery Charge		-	42	-	nC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 1 mH, I_{AS} =3.18 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \le 6.8$ A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

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Typical Performance Characteristics

Figure 1. On-Region Characteristics

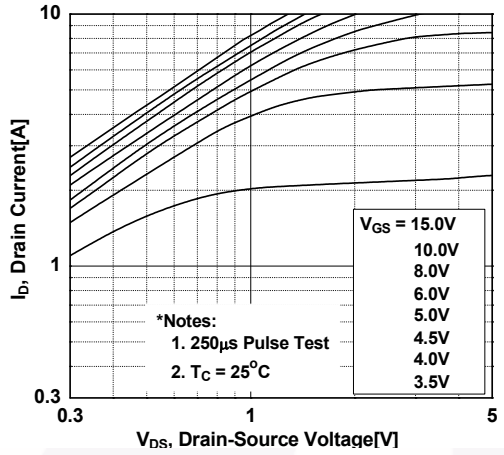


Figure 2. Transfer Characteristics

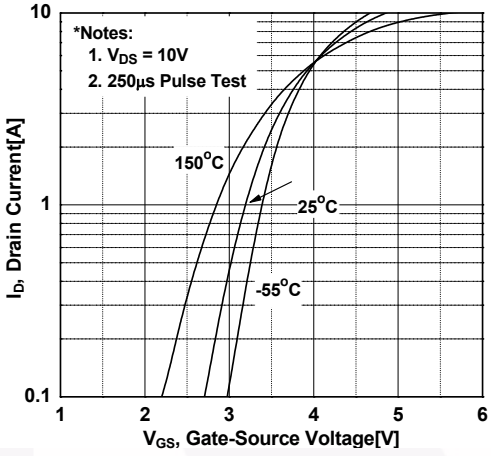


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

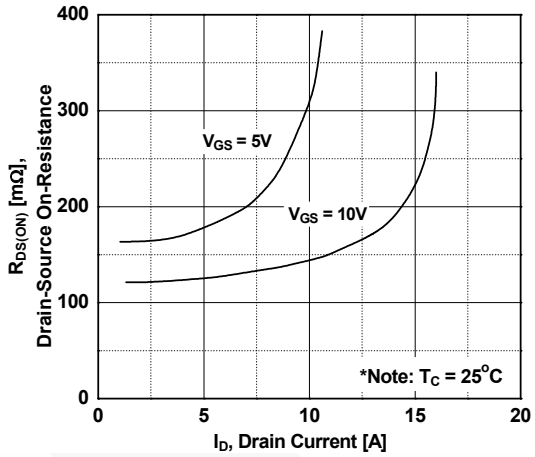


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

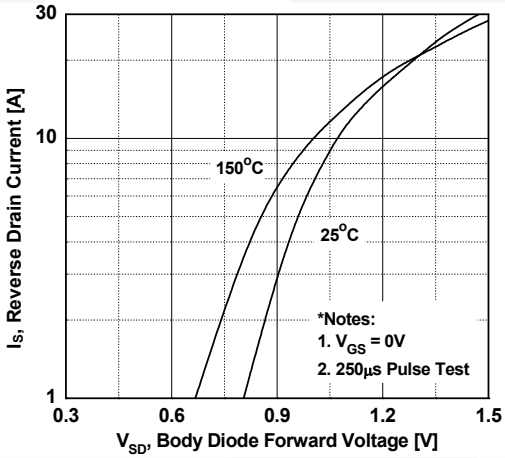


Figure 5. Capacitance Characteristics

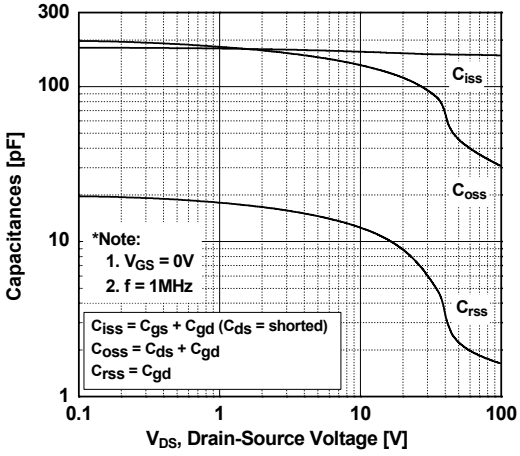
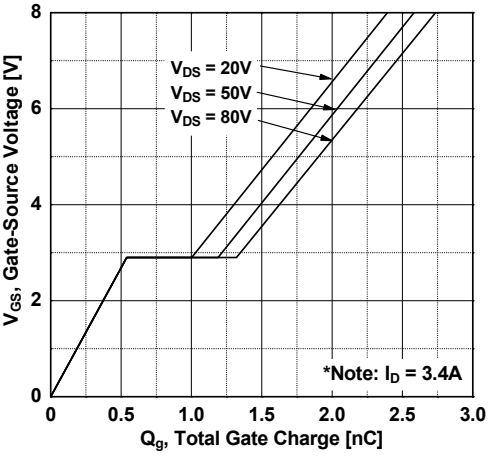


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

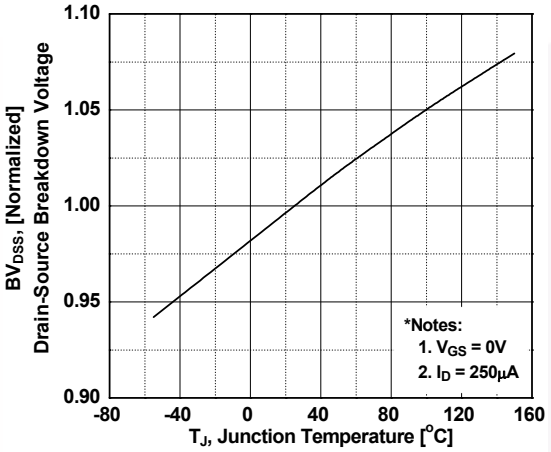


Figure 8. On-Resistance Variation vs. Temperature

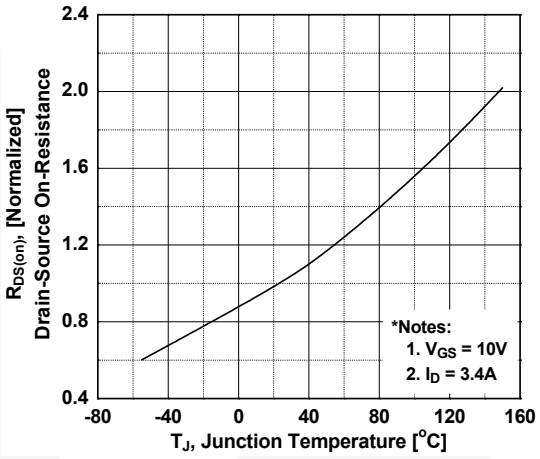


Figure 9. Maximum Safe Operating Area

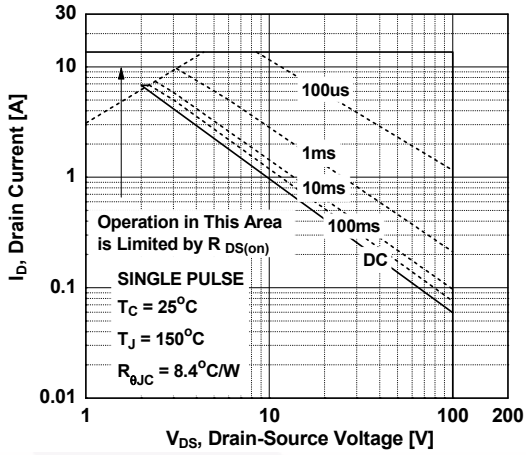


Figure 10. Maximum Drain Current vs. Case Temperature

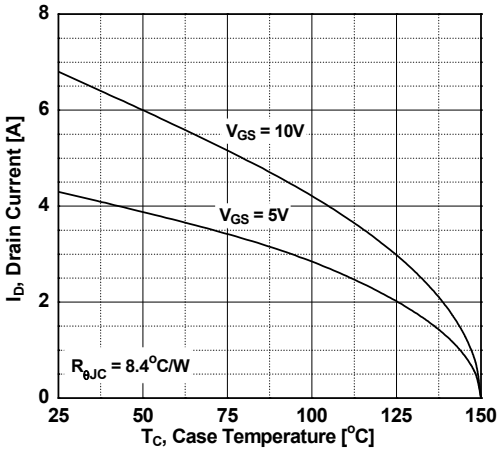


Figure 11. Eoss vs. Drain to Source Voltage

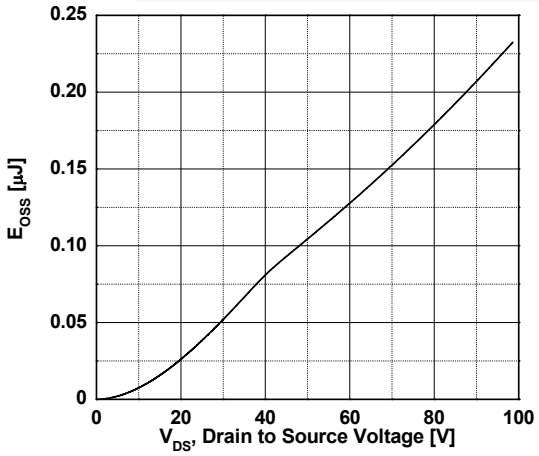
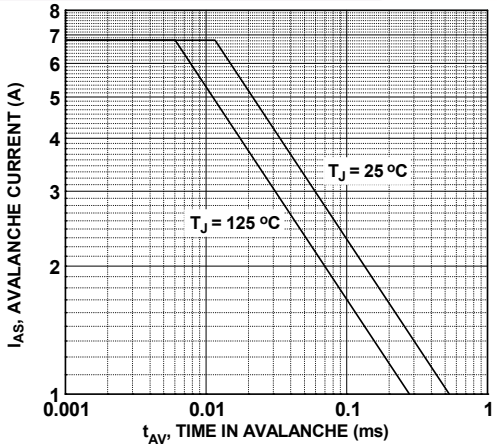
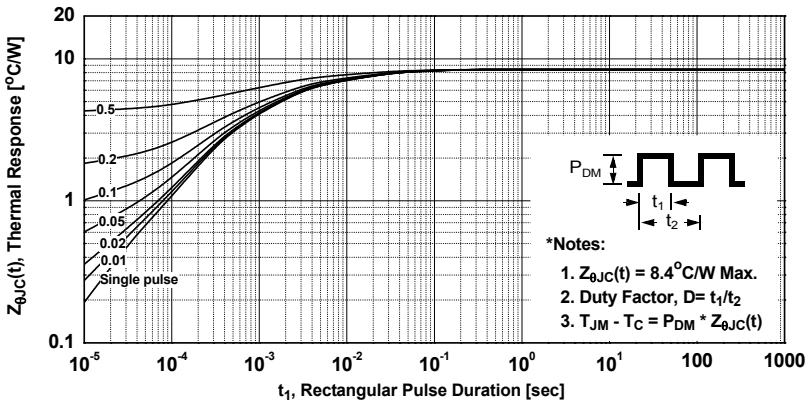


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve



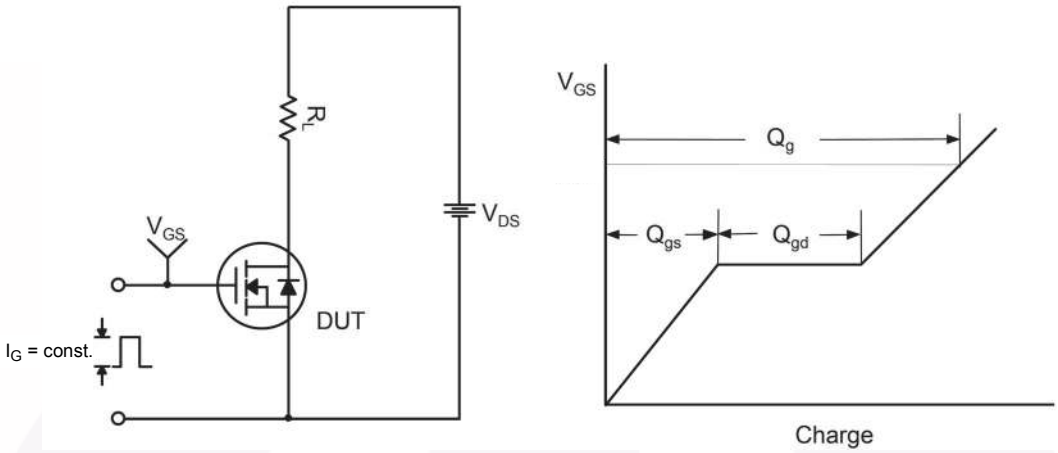


Figure 14. Gate Charge Test Circuit & Waveform

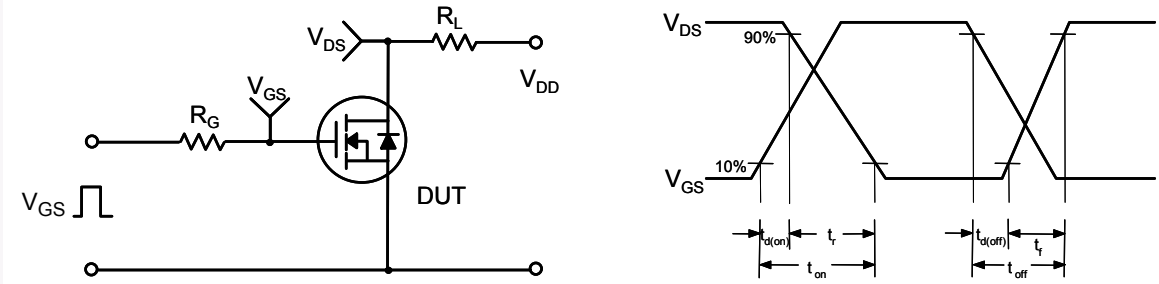


Figure 15. Resistive Switching Test Circuit & Waveforms

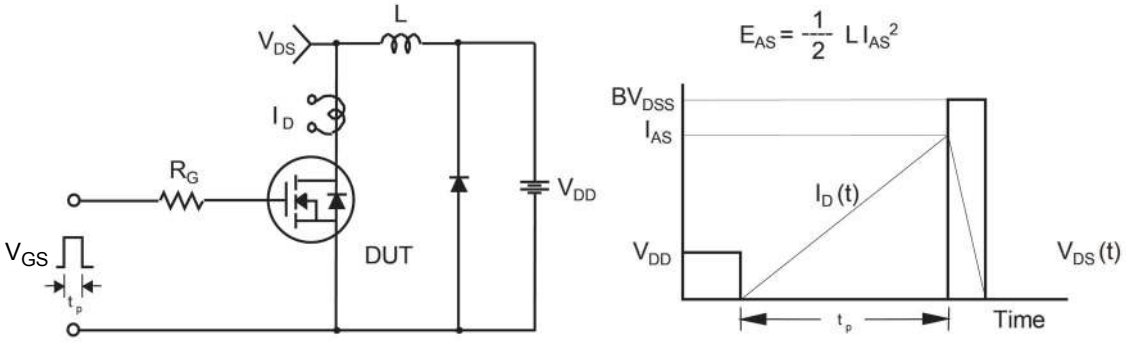


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

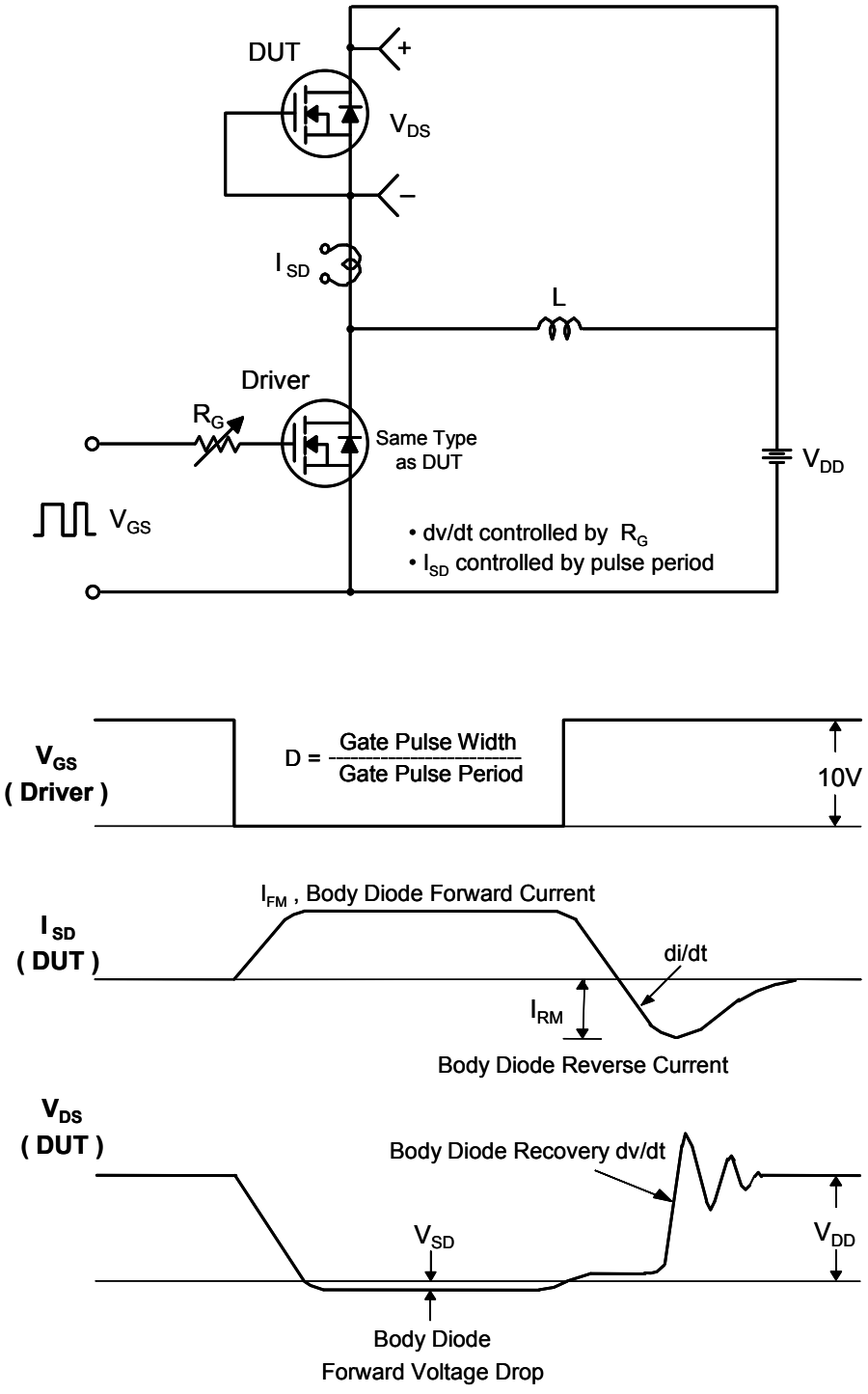
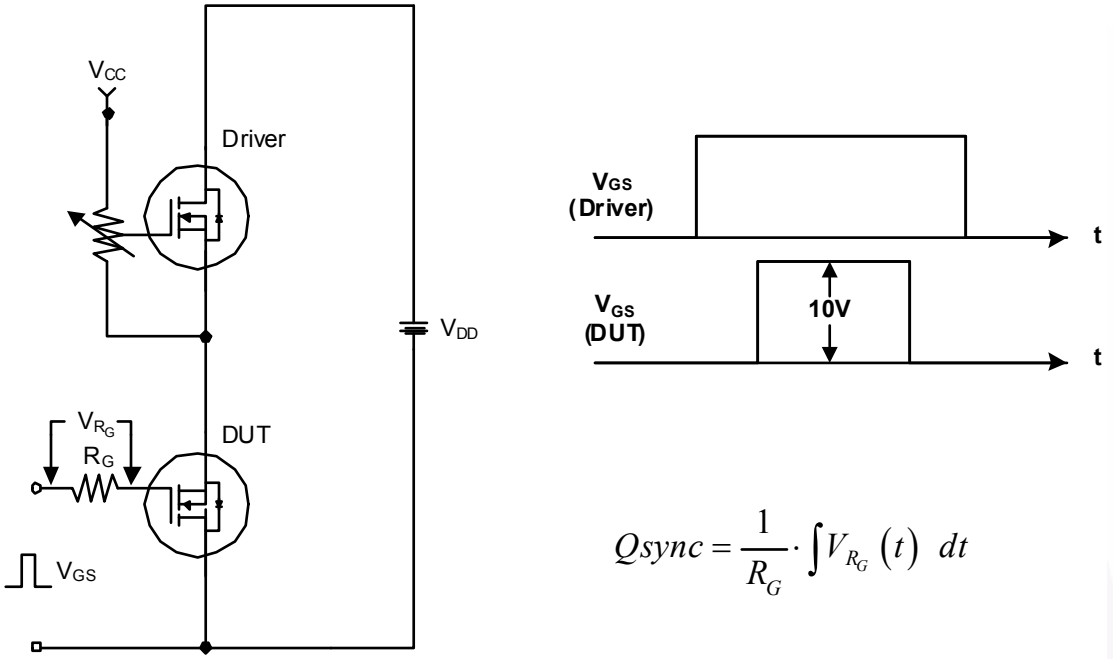


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms



$$Qsync = \frac{1}{R_G} \cdot \int V_{R_G}(t)\ dt$$

Figure 18. Total Gate Charge Qsync. Test Circuit & Waveforms

Mechanical Dimensions

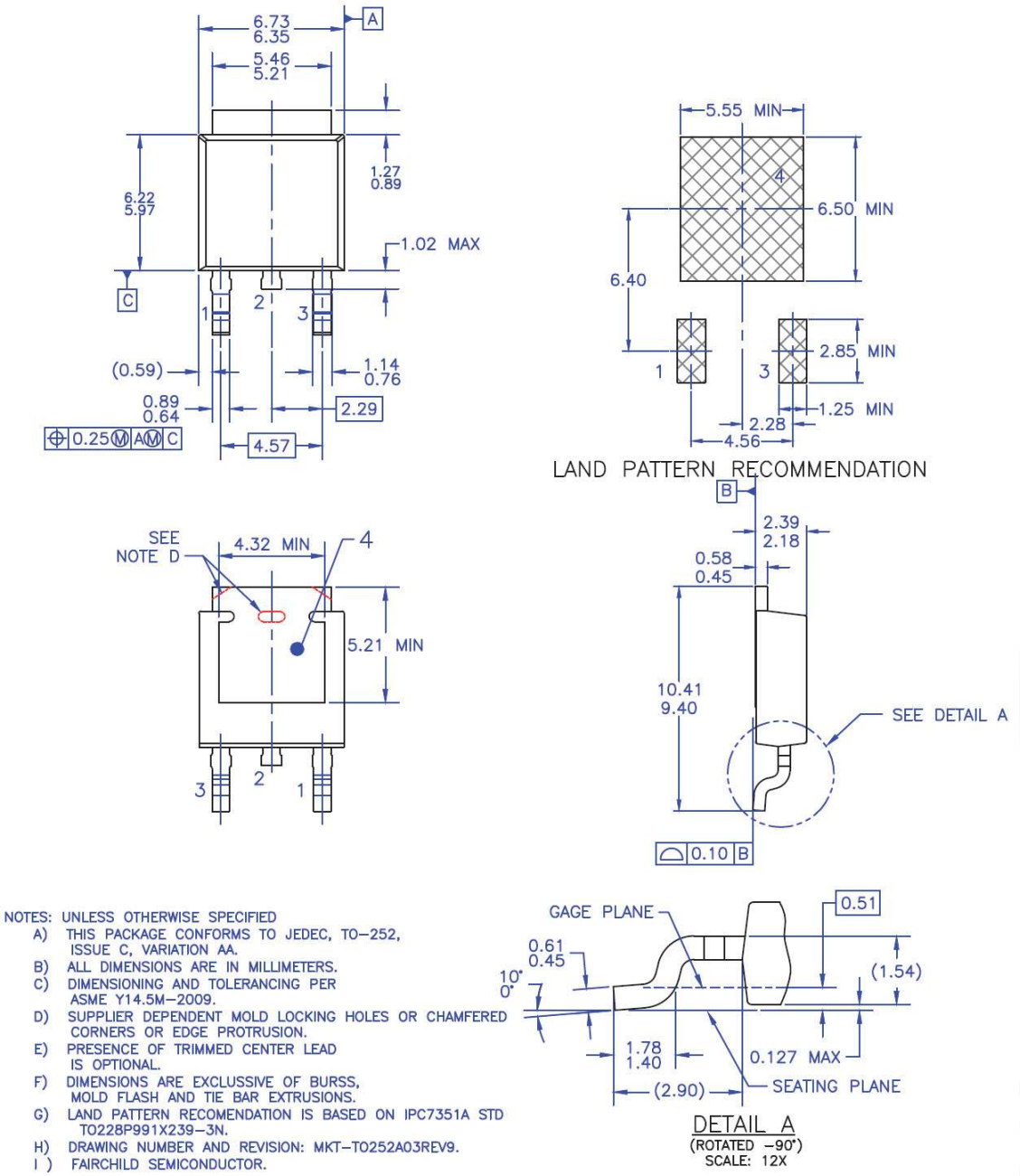


Figure 19. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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