



## Power MOSFET, 180 A



SOT-227

### FEATURES

- Fully isolated package
- Easy to use and parallel
- Very low on-resistance
- Dynamic dV/dt rating
- Fully avalanche rated
- Simple drive requirements
- Low drain to case capacitance
- Low internal inductance
- UL pending
- Compliant to RoHS directive 2002/95/EC



**RoHS**  
COMPLIANT

### PRODUCT SUMMARY

$V_{DSS}$	100 V
$I_D$ DC	180 A
$R_{DS(on)}$	0.0065 $\Omega$
Type	Modules - MOSFET
Package	SOT-227

### DESCRIPTION

5th Generation, high current density Power MOSFETs are paralleled into a compact, high power module providing the best combination of switching, ruggedized design, very low on resistance and cost effectiveness.

The isolated SOT-227 package is preferred for all commercial-industrial applications at power dissipation levels to approximately 500 W. The low thermal resistance and easy connection to the SOT-227 package contribute to its universal acceptance throughout the industry.

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain current at $V_{GS}$ 10 V	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	180	A
		$T_C = 100\text{ }^\circ\text{C}$	120	
Pulsed drain current	$I_{DM}^{(1)}$		720	
Power dissipation	$P_D$	$T_C = 25\text{ }^\circ\text{C}$	480	W
Linear derating factor			2.7	W/ $^\circ\text{C}$
Gate to source voltage	$V_{GS}$		$\pm 20$	V
Single pulse avalanche energy	$E_{AS}^{(2)}$		700	mJ
Avalanche current	$I_{AR}^{(1)}$		180	A
Repetitive avalanche energy	$E_{AR}^{(1)}$		48	mJ
Peak diode recovery dV/dt	dV/dt <sup>(3)</sup>		5.7	V/ns
Operating junction and storage temperature range	$T_J, T_{Stg}$		- 55 to + 150	$^\circ\text{C}$
Insulation withstand voltage (AC-RMS)	$V_{ISO}$		2.5	kV
Mounting torque		M4 screw	1.3	Nm

#### Notes

(1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 8)

(2) Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 43\text{ }\mu\text{H}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 180\text{ A}$  (see fig. 12)

(3)  $I_{SD} \leq 180\text{ A}$ ,  $di/dt \leq 83\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$

# FB180SA10P



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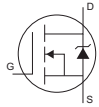
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THERMAL RESISTANCE				
PARAMETER	SYMBOL	TYP.	MAX.	UNITS
Junction to case	$R_{thJC}$	-	0.26	°C/W
Case to sink, flat, greased surface	$R_{thCS}$	0.05	-	

ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.093	-	V/°C
Static drain to source on-resistance	$R_{DS(on)}^{(1)}$	$V_{GS} = 10\text{ V}, I_D = 180\text{ A}$	-	0.0065	-	$\Omega$
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Forward transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}, I_D = 180\text{ A}$	93	-	-	S
Drain to source leakage current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	$\mu\text{A}$
Gate to source forward leakage	$I_{GSS}$	$V_{GS} = 20\text{ V}$ $V_{GS} = -20\text{ V}$	-	-	200	
Total gate charge	$Q_g$	$I_D = 180\text{ A}$ $V_{DS} = 80\text{ V}$ $V_{GS} = 10.0\text{ V}$ ; see fig. 6 and 13 <sup>(1)</sup>	-	250	380	nC
Gate to source charge	$Q_{gs}$		-	40	60	
Gate to drain ("Miller") charge	$Q_{gd}$		-	110	165	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{ V}$ $I_D = 180\text{ A}$ $R_g = 2.0\text{ }\Omega$ (internal) $R_D = 0.27\text{ }\Omega$ , see fig. 10 <sup>(1)</sup>	-	45	-	ns
Rise time	$t_r$		-	351	-	
Turn-off delay time	$t_{d(off)}$		-	181	-	
Fall time	$t_f$		-	335	-	
Internal source inductance	$L_S$	Between lead, and center of die contact	-	5.0	-	nH
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$ , see fig. 5	-	10 700	-	pF
Output capacitance	$C_{oss}$		-	2800	-	
Reverse transfer capacitance	$C_{rss}$		-	1300	-	

**Note**

<sup>(1)</sup> Pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$

SOURCE-DRAIN RATINGS AND CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous source current (body diode)	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	180	A
Pulsed source current (body diode)	$I_{SM}^{(1)}$		-	-	720	
Diode forward voltage	$V_{SD}^{(2)}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 180\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V
Reverse recovery time	$t_{rr}^{(2)}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 180\text{ A}; di/dt = 100\text{ A}/\mu\text{s}$	-	300	450	ns
Reverse recovery charge	$Q_{rr}$		-	2.6	3.9	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

**Notes**

<sup>(1)</sup> Repetitive rating; pulse width limited by maximum junction temperature (see fig. 8)

<sup>(2)</sup> Pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$

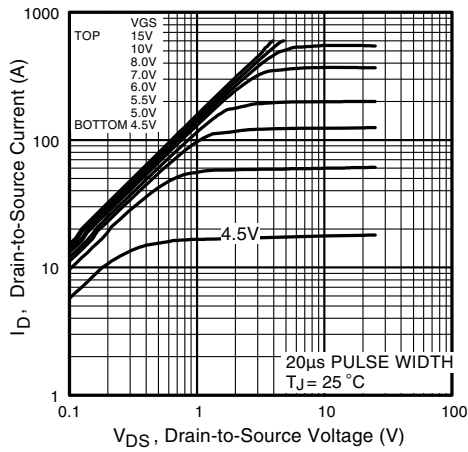


Fig. 1 - Typical Output Characteristics

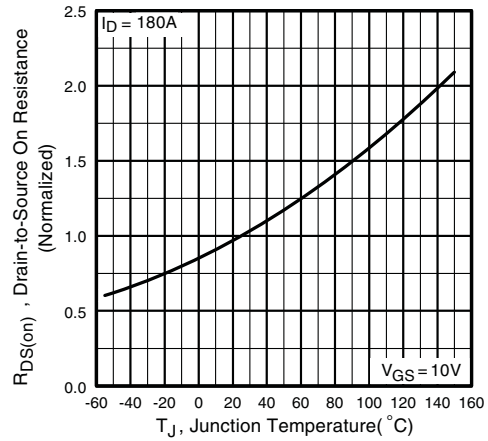


Fig. 4 - Normalized On-Resistance vs. Temperature

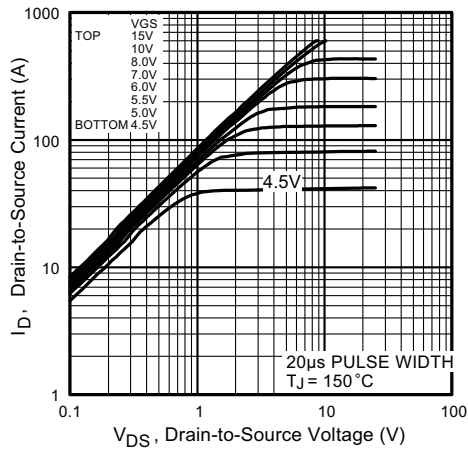


Fig. 2 - Typical Output Characteristics

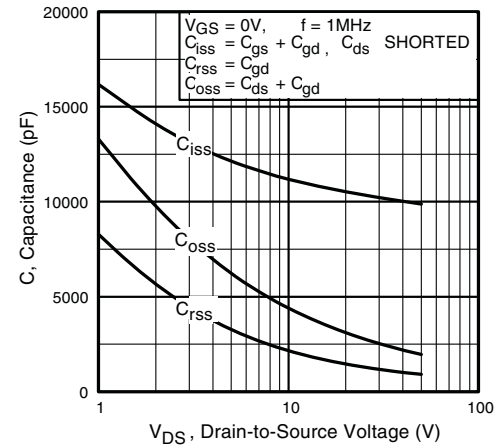


Fig. 5 - Typical Capacitance vs. Drain to Source Voltage

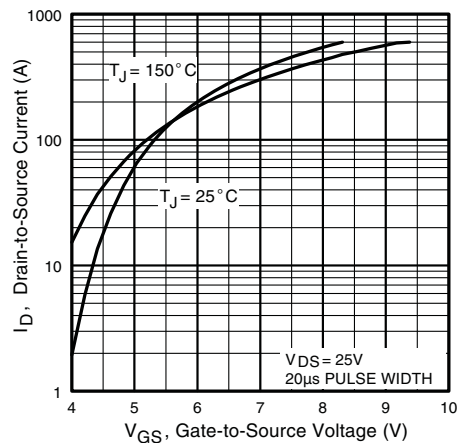


Fig. 3 - Typical Transfer Characteristics

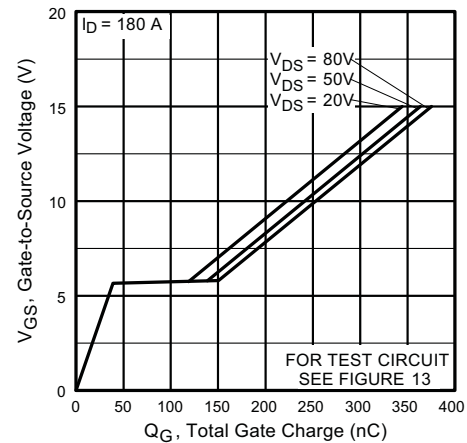


Fig. 6 - Typical Gate Charge vs. Gate to Source Voltage

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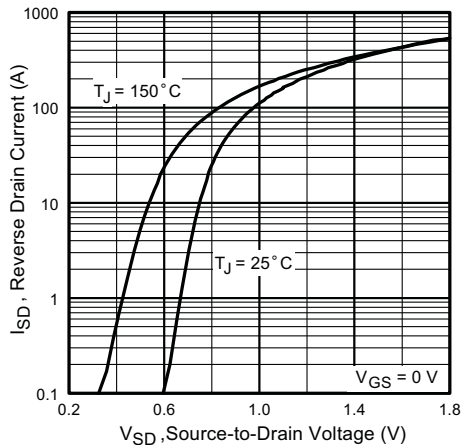


Fig. 7 - Typical Source Drain Diode Forward Voltage

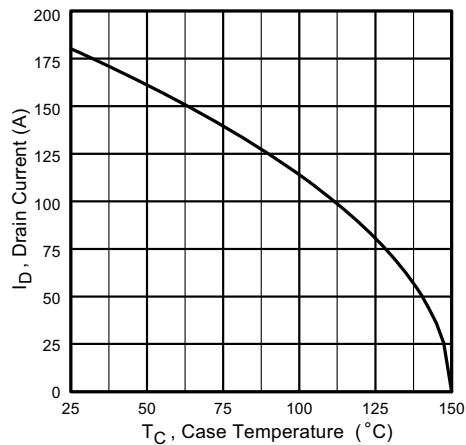


Fig. 9 - Maximum Drain Current vs. Case Temperature

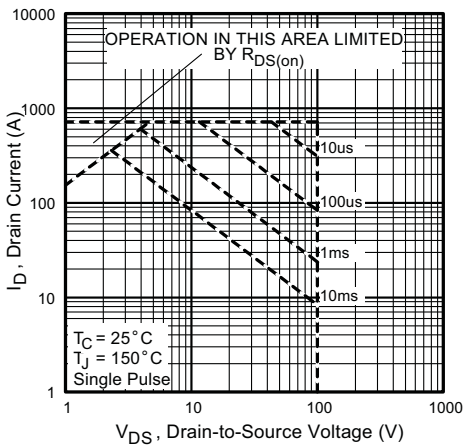


Fig. 8 - Maximum Safe Operating Area

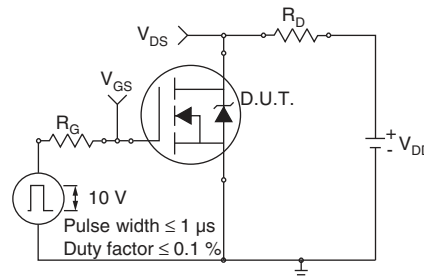


Fig. 10a - Switching Time Test Circuit

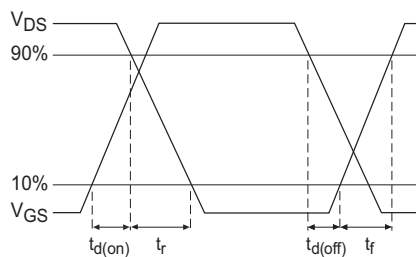


Fig. 10b - Switching Time Waveforms

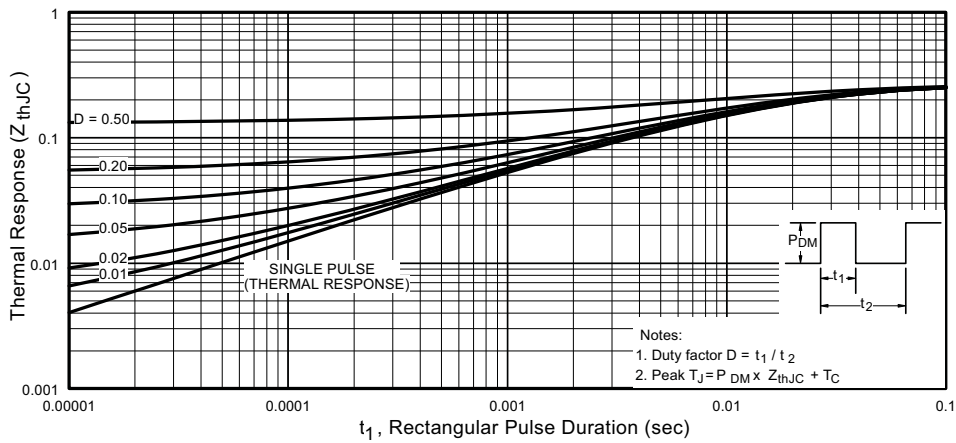


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction to Case

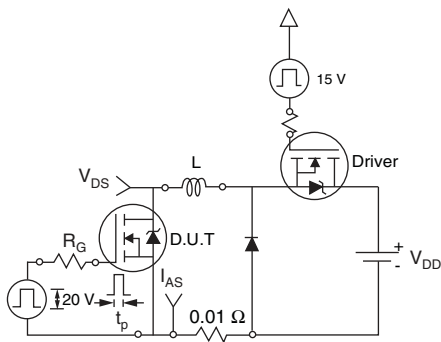


Fig. 12a - Unclamped Inductive Test Circuit

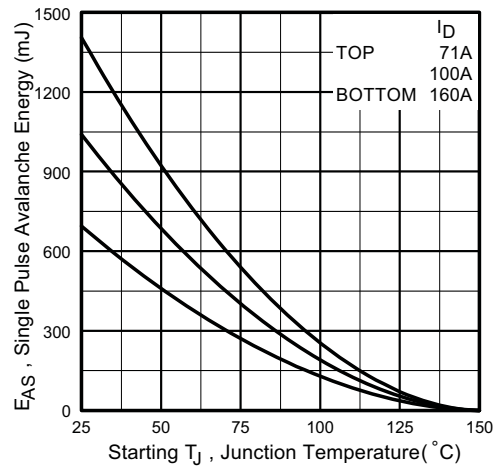


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

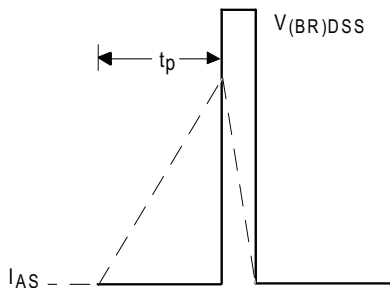


Fig. 12b - Unclamped Inductive Waveforms

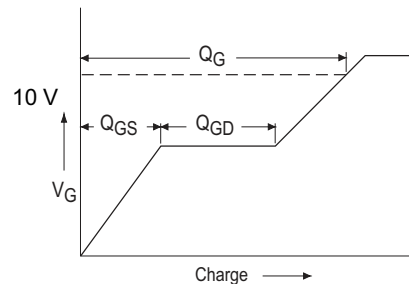


Fig. 13a - Basic Gate Charge Waveform

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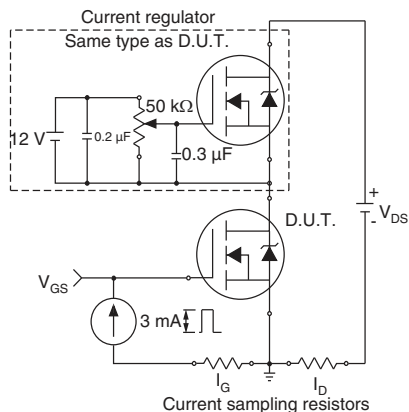


Fig. 13b - Gate Charge Test Circuit

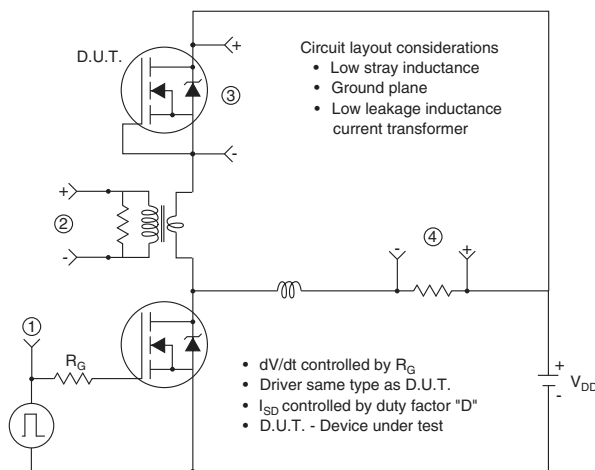
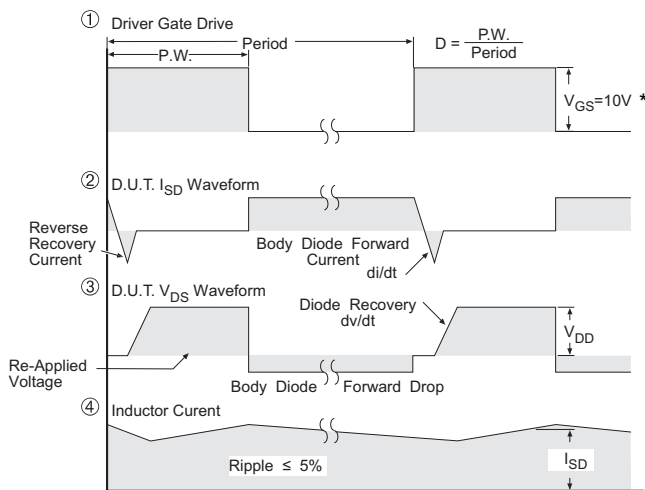


Fig. 13c - Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

Fig. 14 - For N-Channel Power MOSFETs



**ORDERING INFORMATION TABLE**

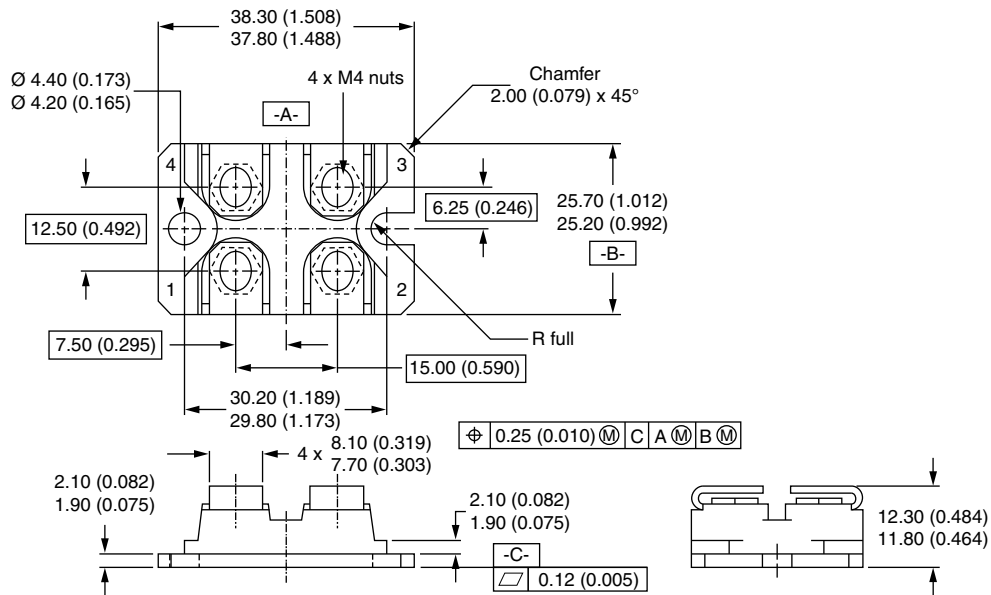
Device code	<b>F</b>	<b>B</b>	<b>180</b>	<b>S</b>	<b>A</b>	<b>10</b>	<b>P</b>														
	①	②	③	④	⑤	⑥	⑦														
	<b>1</b>	-	Power MOSFET	<b>2</b>	-	Generation 5 MOSFET silicon DBC construction	<b>3</b>	-	Current rating (180 = 180 A)	<b>4</b>	-	Single switch	<b>5</b>	-	SOT-227	<b>6</b>	-	Voltage rating (10 = 100 V)	<b>7</b>	-	P = Lead (Pb)-free

CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Single switch no diode	S	 

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95036">www.vishay.com/doc?95036</a>
Packaging information	<a href="http://www.vishay.com/doc?95037">www.vishay.com/doc?95037</a>

## SOT-227

**DIMENSIONS** in millimeters (inches)



**Notes**

- Dimensioning and tolerancing per ANSI Y14.5M-1982
- Controlling dimension: millimeter





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