

SUPER LOW OPERATING CURRENT AND LOW OFFSET VOLTAGE TINY SINGLE CMOS COMPARATOR

■ GENERAL DESCRIPTION

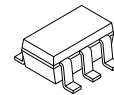
The NJU7116 is a super low operating current and low offset voltage tiny single CMOS comparator with CMOS output.

The operating current is $1\mu\text{A}$ (typ), and the operating of 1.8V to 3.6V.

The input offset voltage is lower than 2.5mV (max).

Furthermore, the NJU7116 is packaged with very small SOT-23-5 DFN6-G1; therefore it can be especially applied to battery operated portable items.

■ PACKAGE OUTLINE



NJU7116F

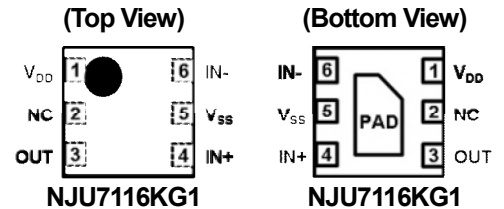
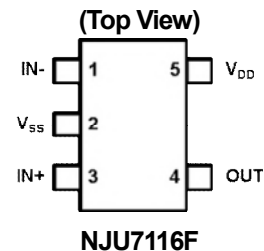


NJU7116KG1

■ FEATURES

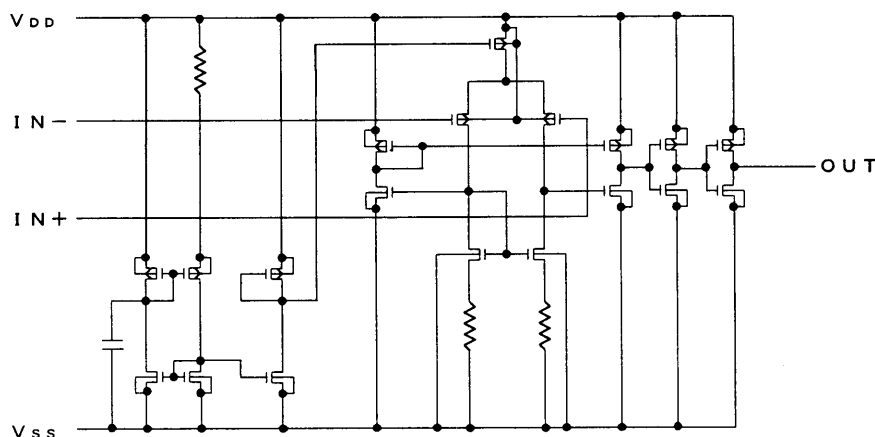
- Super Low Operating Current ($I_{DD}=1.0\mu\text{A}$ typ.)
- Single Power Supply ($V_{DD}=1.8$ to 3.6V)
- Low Offset Voltage ($V_{IO}=2.5\text{mV}$ max.@ 3.0V)
- Low Bias Current ($I_B=1\text{pA}$ typ.)
- CMOS (Push-pull) Output
- Package Outline SOT-23-5, DFN6-G1
- CMOS Technology

■ PIN CONFIGURATION



The NC pin and the PAD should connect with a VSS terminal.

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{DD}	7	V
Differential Input Voltage	V _{ID}	± 7 (note1)	V
Common Mode Input Voltage	V _{IC}	-0.3 to 7(note1)	V
Power Dissipation	P _D	390 (note 3) / 520 (note 4) 260 (note 5) / 950 (note 6)	mW
Operating Temperature Range	T _{opr}	-40 to +105	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C

(note1) For supply voltage less than 7V, the absolute maximum rating is equal to the supply voltage.

(note2) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

(note3) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layers, FR-4) mounting

(note4) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 4layers, FR-4) mounting

(note5) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(note6) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)

(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

(note7) The NC pin and the PAD should connect with a VSS terminal.

(note8) The NC pin is electrically not connected to the die in a package.

(note9) The PAD is electrically connected to the backside of the die. The PAD cannot be used as VSS terminal.

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}=3.0V, R_L=∞)

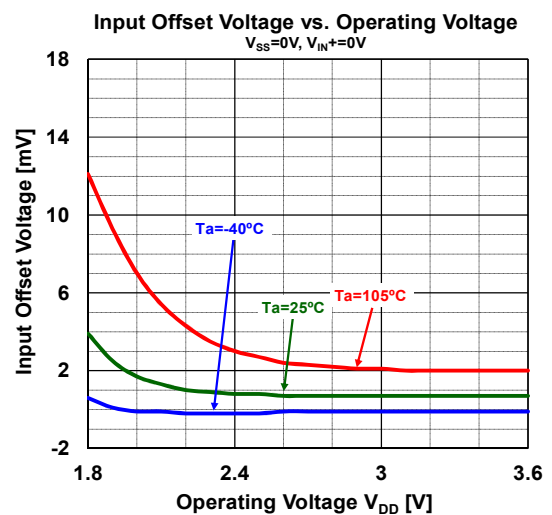
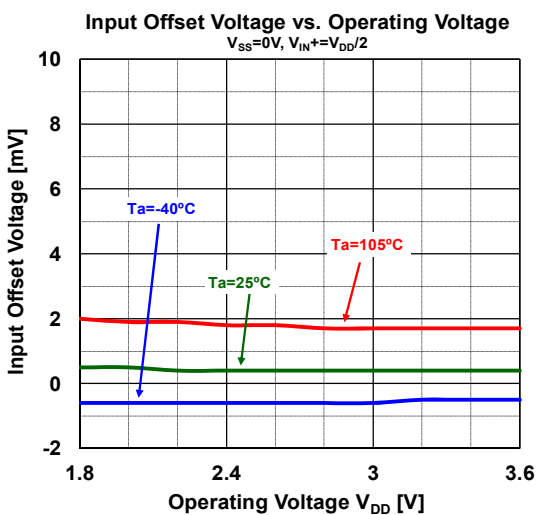
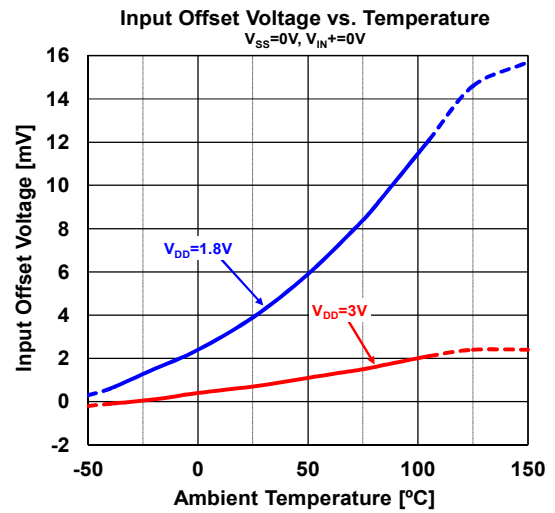
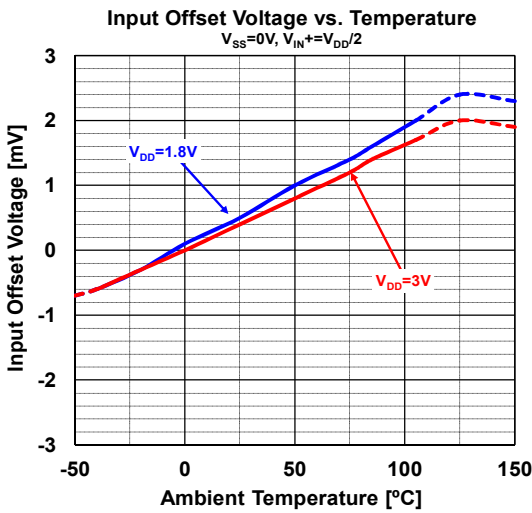
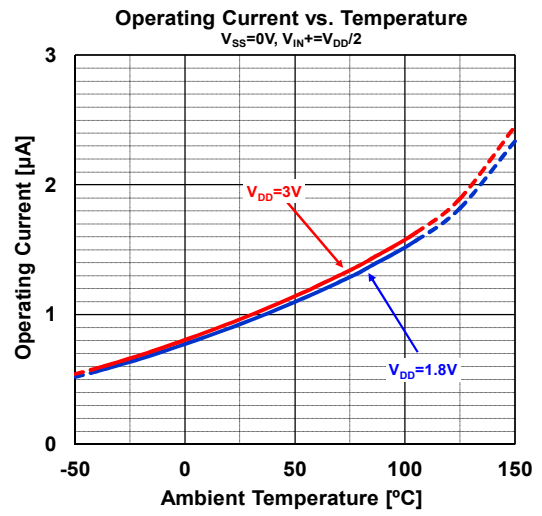
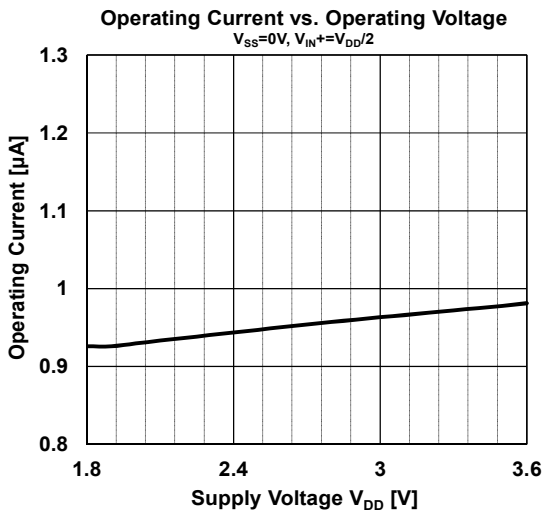
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V _{DD}		1.8	-	3.6	V
Input Offset Voltage	V _{IO}	V _{IN} =1/2V _{DD}	-	-	2.5	mV
Input Offset Current	I _{IO}		-	1	-	pA
Input Bias Current	I _{IB}		-	1	-	pA
Input Common Mode Voltage Range	V _{ICM}		0~2.5	-	-	V
High Level Output Voltage	V _{OH}	I _{OH} =2mA	2.7	-	-	V
Low Level Output Voltage	V _{OL}	I _{OL} =-2mA	-	-	0.3	V
Common Mode Rejection Ratio	CMR	V _{IC} =1/2V _{DD}	50	-	-	dB
Supply Voltage Rejection Ratio	SVR	V _{DD} =1.8~3.6V	50	-	-	dB
Operating Current	I _{DD}	No Load, V _O =0V	-	1	1.5	μA

■ SWITCHING CHARACTERISTICS

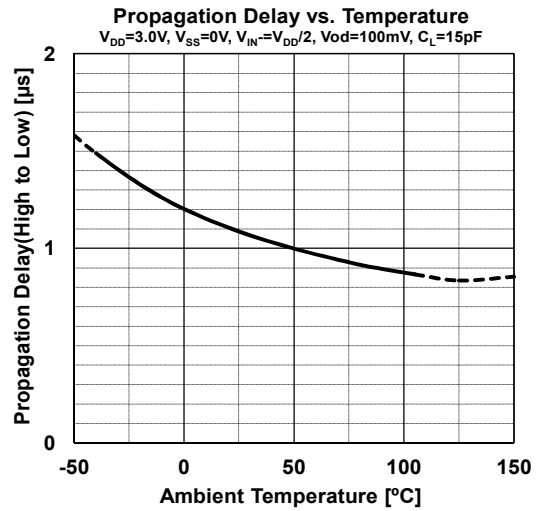
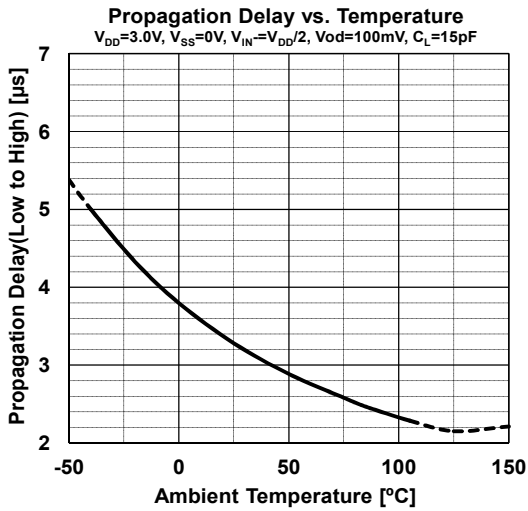
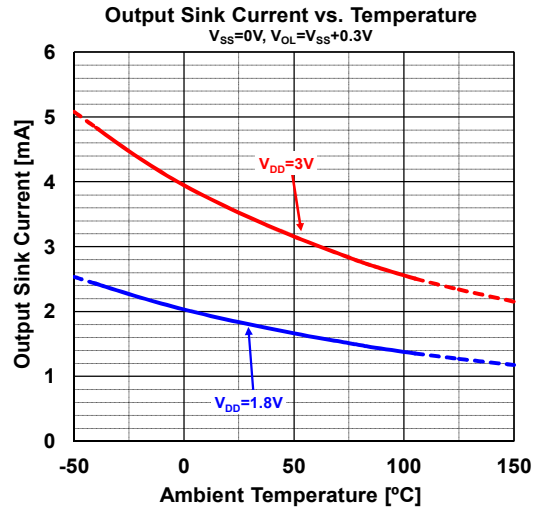
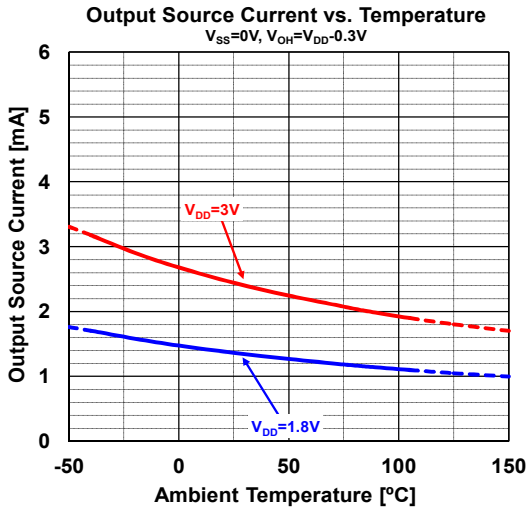
(Ta=25°C, V_{DD}=3.0V, f=1kHz, C_L=15pF)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay High to Low	t _{PHL}	Over Drive=100mV	-	1.2	2.0	μs
		TTL Level Step In.	-	0.37	-	
Propagation Delay Low to High	t _{PLH}	Over Drive=100mV	-	3.3	5.0	μs
		TTL Level Step In.	-	2.6	-	
Propagation Delay Time Lag	t _{PD}	t _{PLH} - t _{PHL}	-	2.1	3.0	μs
Output Signal Falling Time	t _{THL}	Over Drive=100mV	-	15	-	ns
Output Signal Rising Time	t _{TLH}	Over Drive=100mV	-	40	-	ns

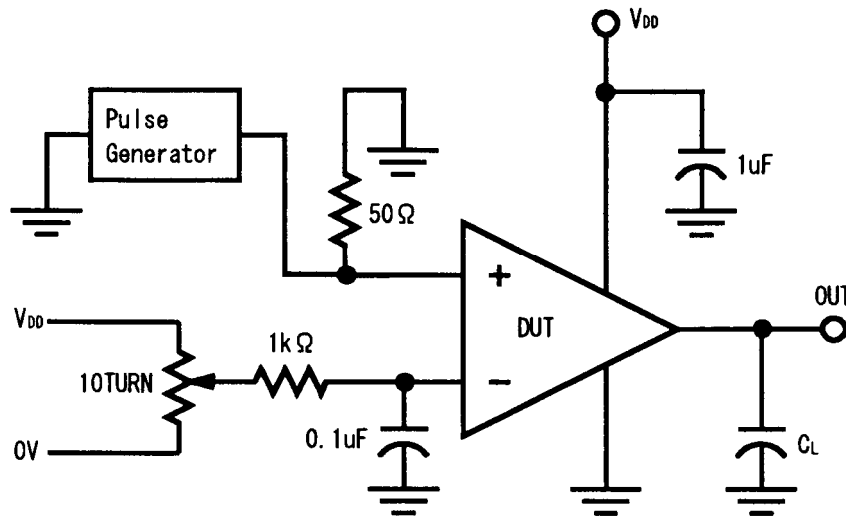
TYPICAL CHARACTERISTICS



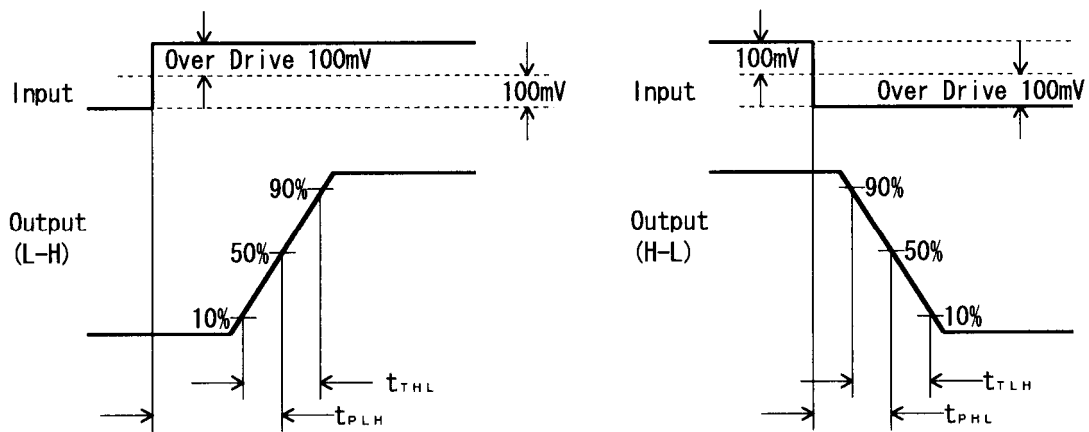
■ TYPICAL CHARACTERISTICS



■ SWITCHING CHARACTERISTICS MEASUREMENT CIRCUIT

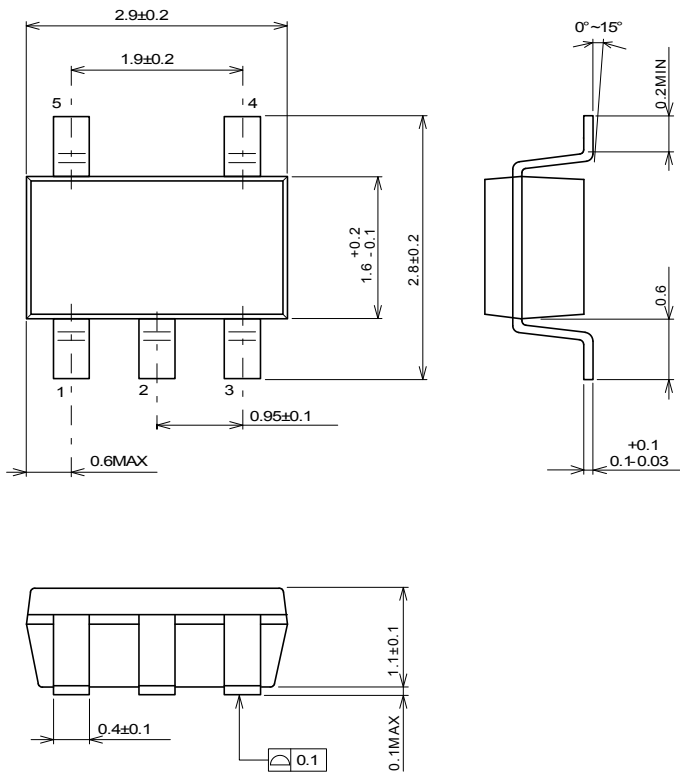


■ TIMING WAVEFORM



NJU7116

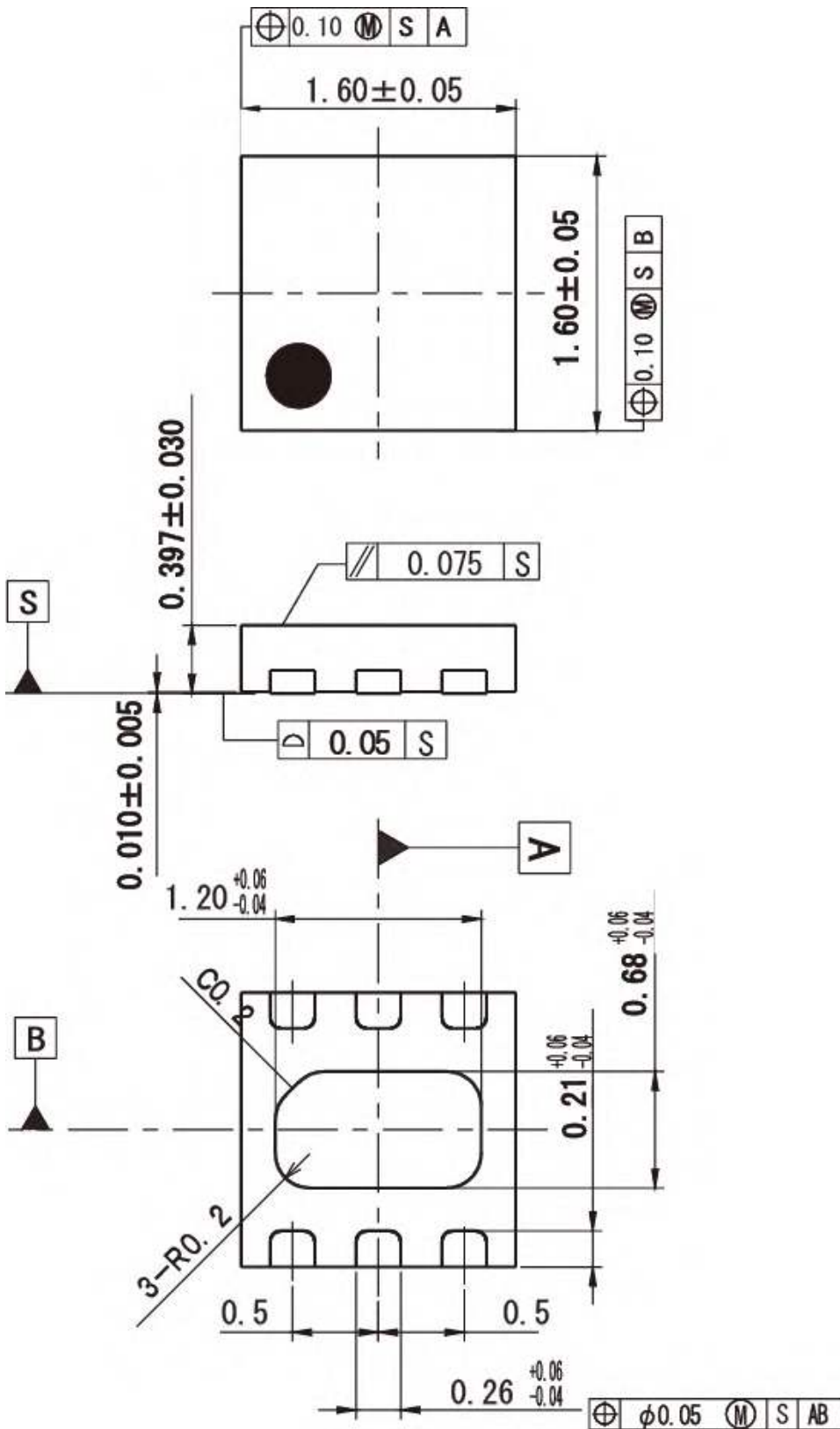
■ PACKAGE DIMENSIONS



Unit: mm

SOT-23-5 Package

■ PACKAGE DIMENSIONS



Unit: mm

DFN6-G1 Package

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