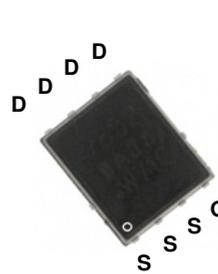
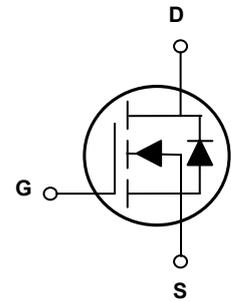


Main Product Characteristics

$V_{(BR)DSS}$	100V
$R_{DS(ON)}$	7m Ω
I_D	80A



PPAK 5X6



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for high efficiency switch mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery



Description

The GSFP1080 utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supply and a wide variety of other applications.

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Max.	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, @Steady-State ($T_A=25^\circ\text{C}$)	I_D	80	A
Continuous Drain Current, @Steady-State ($T_A=100^\circ\text{C}$)		58	A
Pulsed Drain Current ¹	I_{DM}	320	A
Power Dissipation($T_A=25^\circ\text{C}$)	P_D	105	W
Derating Factor($T_A=25^\circ\text{C}$)		0.84	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ⁴	E_{AS}	387	mJ
Junction-to-Case Thermal Resistance @Steady-State	$R_{\theta JC}$	1.19	$^\circ\text{C}/\text{W}$
Operating Junction Temperature Range	T_J	-55 To +150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 To +150	$^\circ\text{C}$

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
		$T_J=125^\circ\text{C}$	-	-	50	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS}=+20V$	-	-	100	nA
		$V_{GS}=-20V$	-	-	-100	
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$	-	6.4	7	m Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.0	4.0	V
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=40A$	-	60	-	S
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V, F=1.0\text{MHz}$	-	3070	-	μF
Output Capacitance	C_{oss}		-	290	-	
Reverse Transfer Capacitance	C_{rss}		-	23	-	
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=40A, V_{GS}=10V$	-	53	-	nC
Gate-Source Charge	Q_{gs}		-	18	-	
Gate-to-Drain("Miller") Charge	Q_{gd}		-	16	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=50V, I_D=40A, R_L=1.3\Omega, V_{GS}=10V, R_{GEN}=1.6\Omega$	-	15	-	nS
Rise Time	t_r		-	10	-	
Turn-Off Delay Time	$t_{d(off)}$		-	34	-	
Fall Time	t_f		-	8	-	
Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode) ²	I_S	MOSFET symbol showing the integral reverse p-n junction diode.	-	-	80	A
Pulsed Source-Drain Current (Body Diode)	I_{SM}		-	-	160	A
Diode Forward Voltage	V_{SD}	$I_S=40A, V_{GS}=0V$	-	0.88	1.2	V
Reverse Recovery Time	t_{rr}	$T_J=25^\circ\text{C}, I_S=I_F=40A, di/dt=100A/\mu s$	-	60	-	nS
Reverse Recovery Charge	Q_{rr}		-	106	-	nC

Notes

1. Repetitive Rating: pulse width limited by maximum junction temperature.
2. Pulse test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
3. Guaranteed by design
4. E_{AS} condition: $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$.

Typical Electrical and Thermal Characteristic Curves

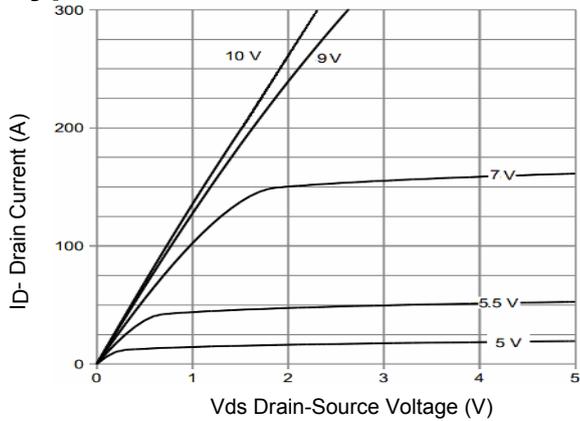


Figure 1. Typical Output Characteristics

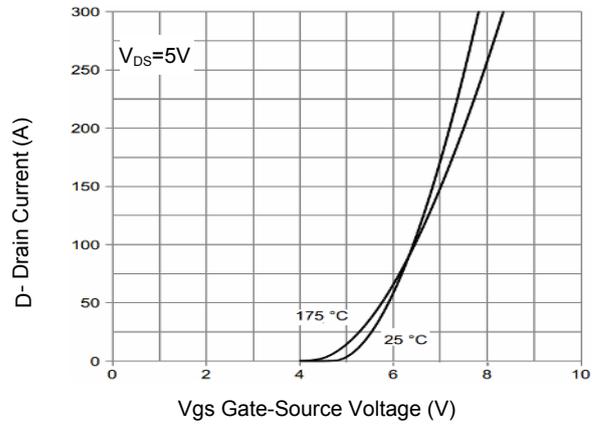


Figure 2. Transfer Characteristics

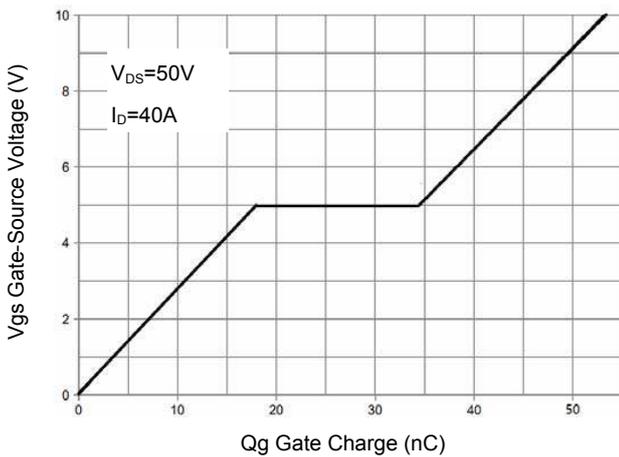


Figure 3. Gate Charge

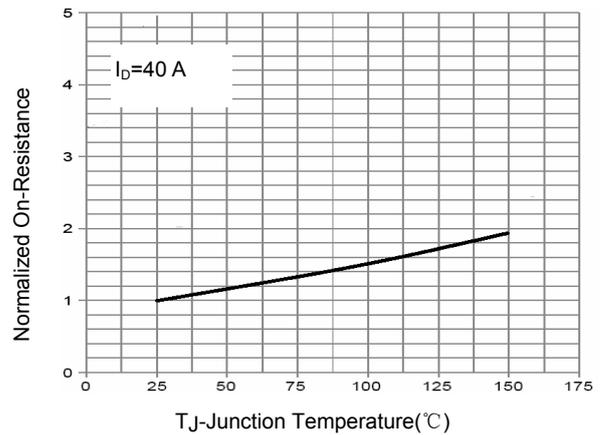


Figure 4. Normalized On-Resistance Vs. Junction Temperature

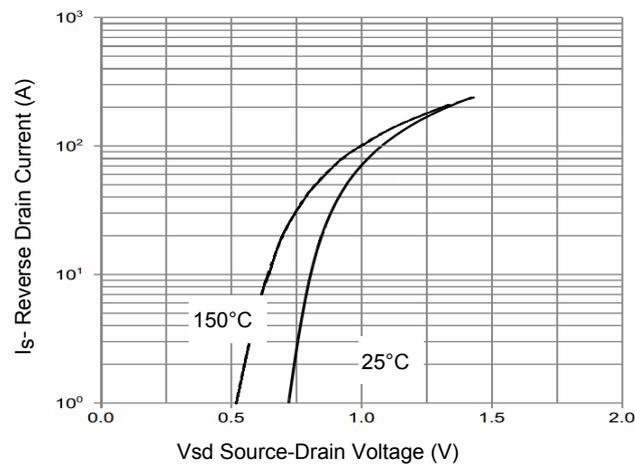


Figure 5. Source-Drain Diodes Forward

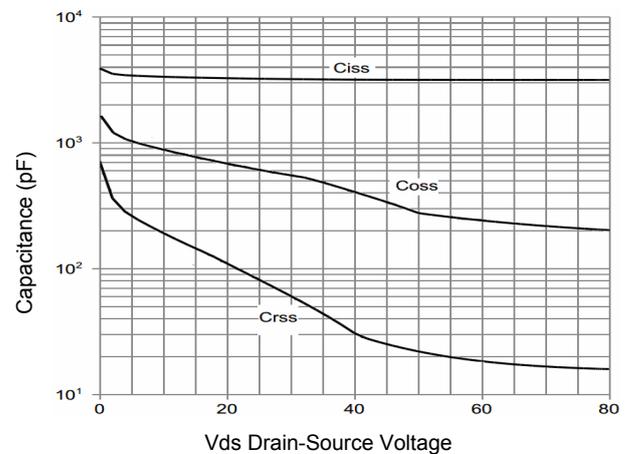


Figure 6. Typical Capacitance vs. Drain-to-Source Voltage

Typical Electrical and Thermal Characteristic Curves

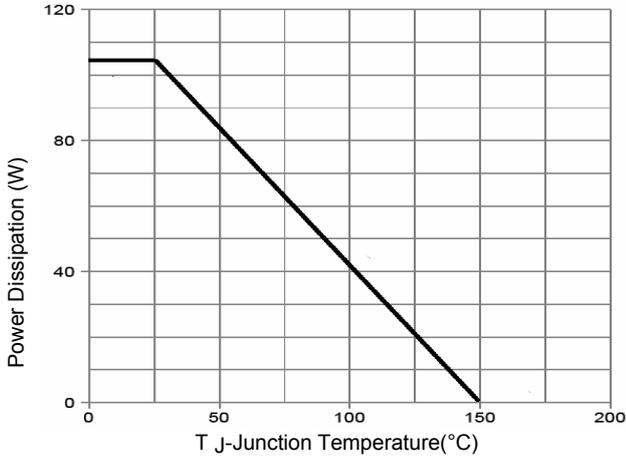


Figure 7. Power Derating

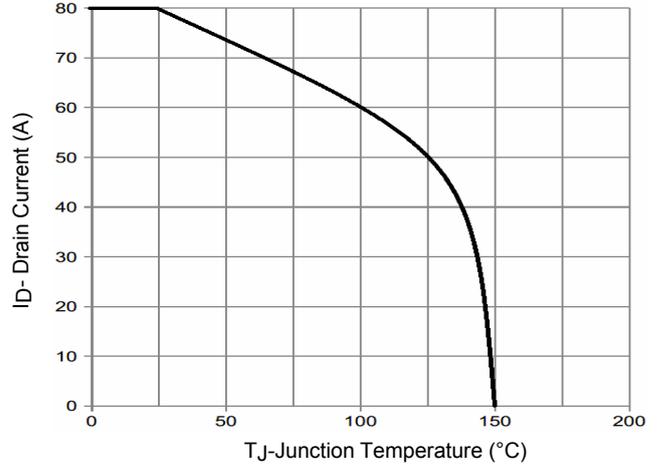


Figure 8. Current Derating

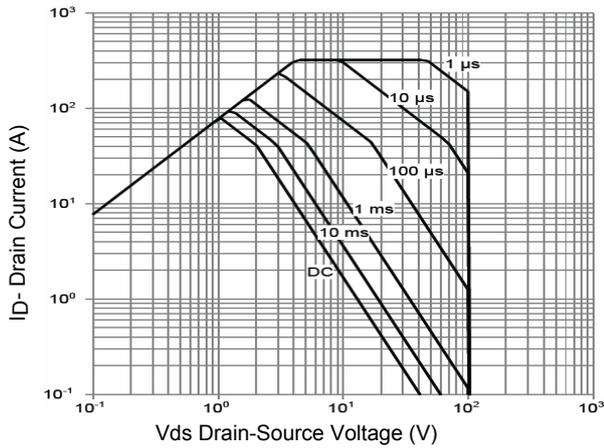


Figure 9. Safe Operation Area

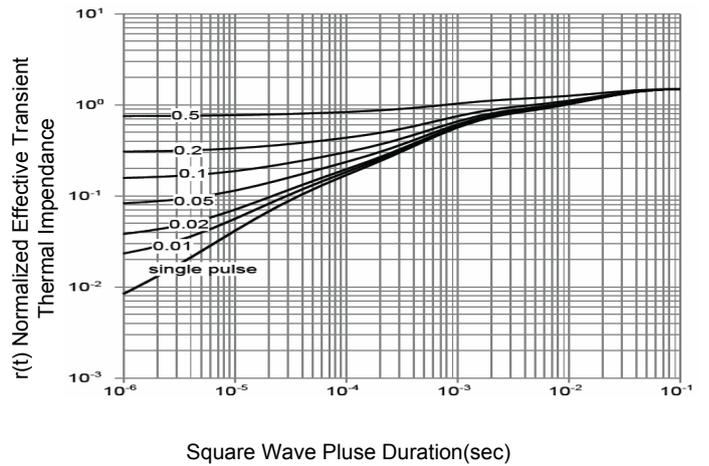


Figure 10. Normalized Maximum Transient Thermal Impedance

Typical Electrical and Thermal Characteristic Curves

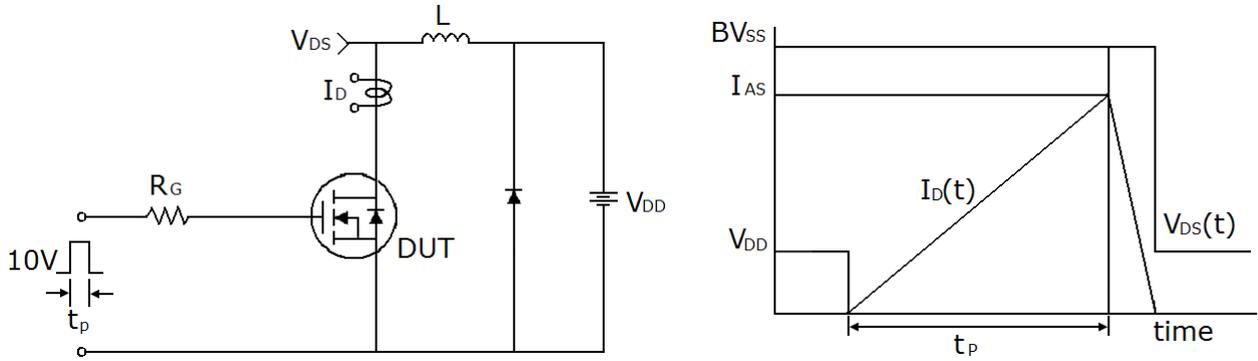


Figure 11. Unclamped Inductive Switching Test Circuit & Waveforms

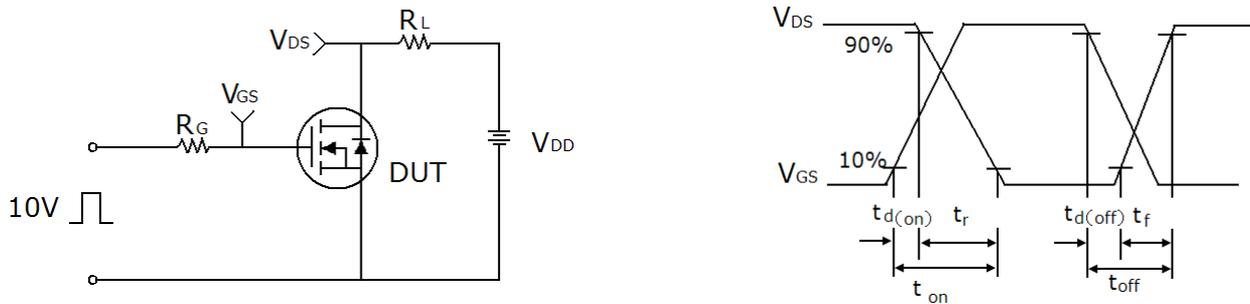


Figure 12. Resistive Switching Test Circuit & Waveforms

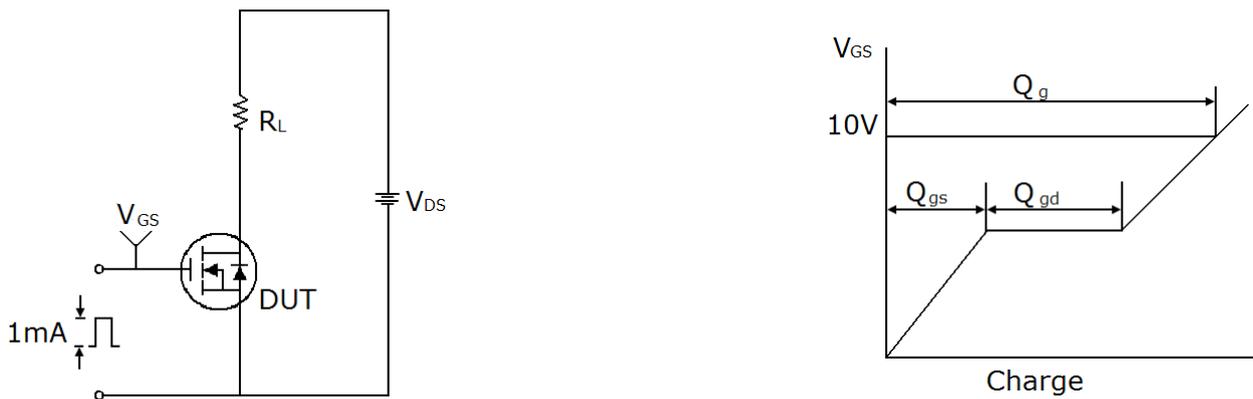
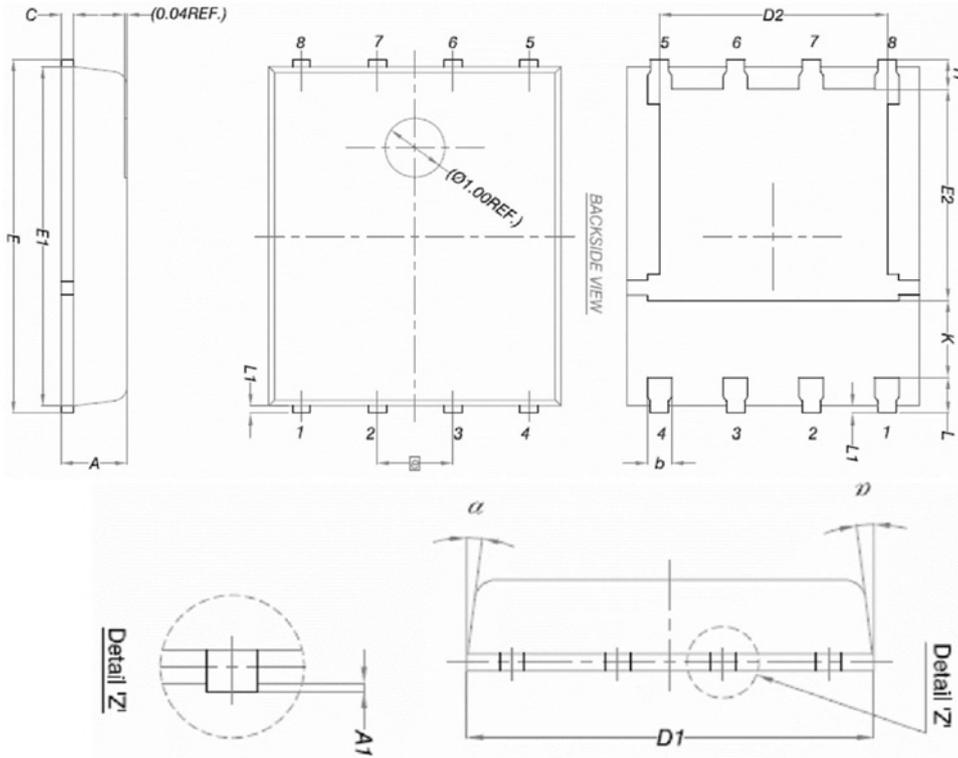


Figure 13. Gate Charge Test Circuit & Waveform

Package Outline Dimensions (PPAK5X6-8L)



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

