TLE6389

Step-Down DC/DC Controller

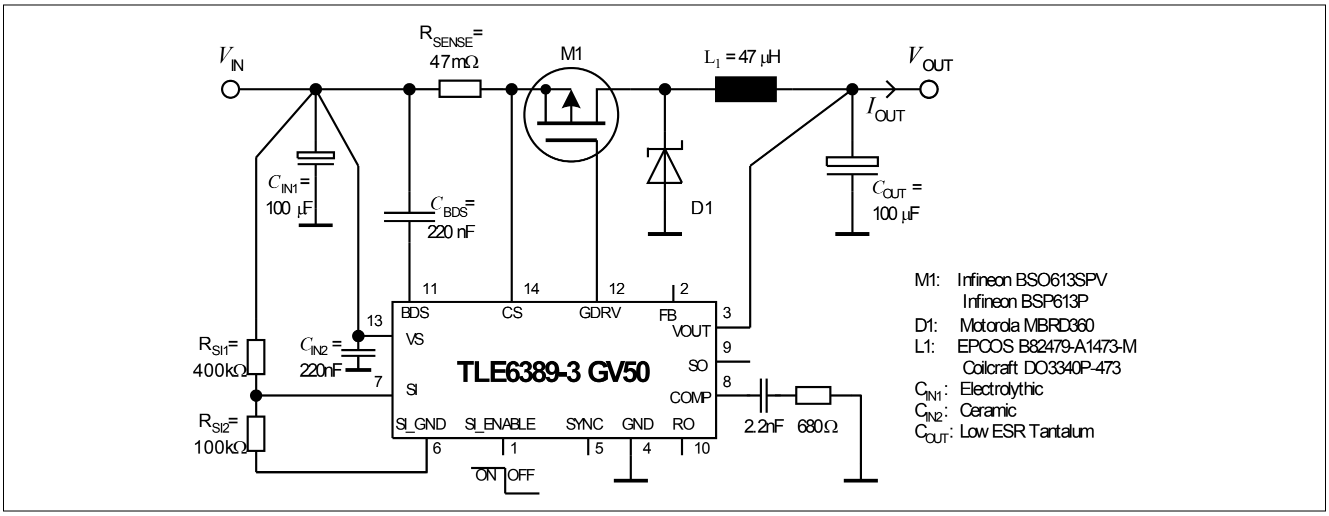
1 Overview

Features

- Input voltage range from < 5V up to 60V
- Output voltage: 5V fixed or adjustable (7V to 15V)
- Output voltage accuracy: 3%
- Output current up to 2.3A
- 100% maximum duty cycle
- Less than 120µA quiescent current at low loads1)
- 2µA max. shutdown current at device off (TLE6389-2GV)
- Fixed 360kHz switching frequency
- Frequency synchronization input for external clocks
- Current Mode control scheme
- Integrated output under voltage Reset circuit
- On chip low battery detector (on chip comparator)
- Automotive temperature range -40°C to 150 °C
- Green Product (RoHS compliant)

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.



Description

The TLE6389 step-down DC-DC switching controllers provide high efficiency over loads ranging from 1mA up to 2.5A. A unique PWM/PFM control scheme operates with up to a 100% duty cycle, resulting in very low dropout voltage. This control scheme eliminates minimum load requirements and reduces the supply current under light loads to 120µA, depending on dimensioning of external components. In addition the adjustable version TLE6389-2GV can be shut down via the Enable input reducing the input current to <2µA. The TLE6389 step-down controllers drive an external P-channel MOSFET, allowing design flexibility for applications up to 12.5W of output power. A high switching frequency and operation in continuous-conduction mode allow the use of tiny surface-mount inductors. Output capacitor requirements are also reduced, minimizing PC board area and system costs. The output voltage is preset at 5V (TLE6389-2GV50 and TLE6389-3GV50) and adjustable for the TLE6389-2GV. The version TLE6389-2GV50 features a reset function with a threshold between 4.5V and 4.8V, including a small hysteresis of typ. 50mV. In the version TLE6389-3GV50 the device incorporates a reset with a typ. 1V hysteresis. Input voltages of all TLE6389 can be up to 60V.

Type	**Package**	**Marking**
TLE6389-2GV	PG-DSO-14	6389-2GV
TLE6389-2GV50	PG-DSO-14	6389-2GV50
TLE6389-3GV50	PG-DSO-14	6389-3GV50

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1.1 Pin Configuration (top view)

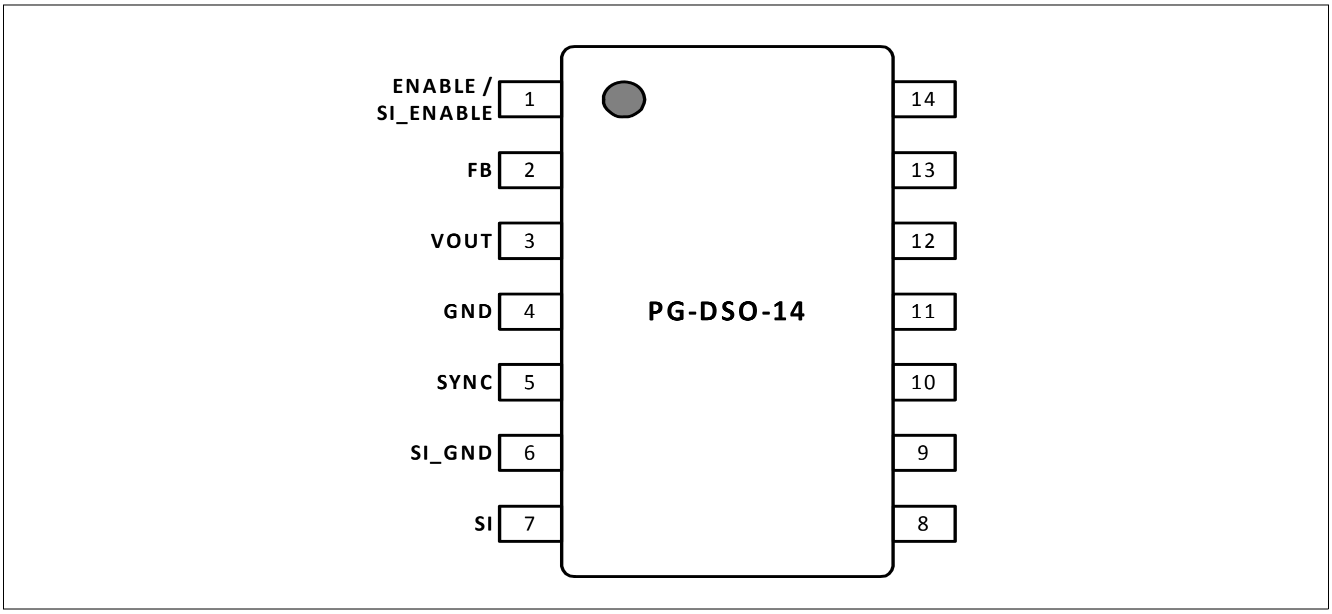


Figure 1 Pin Configuration

1.2 Basic Block Diagram

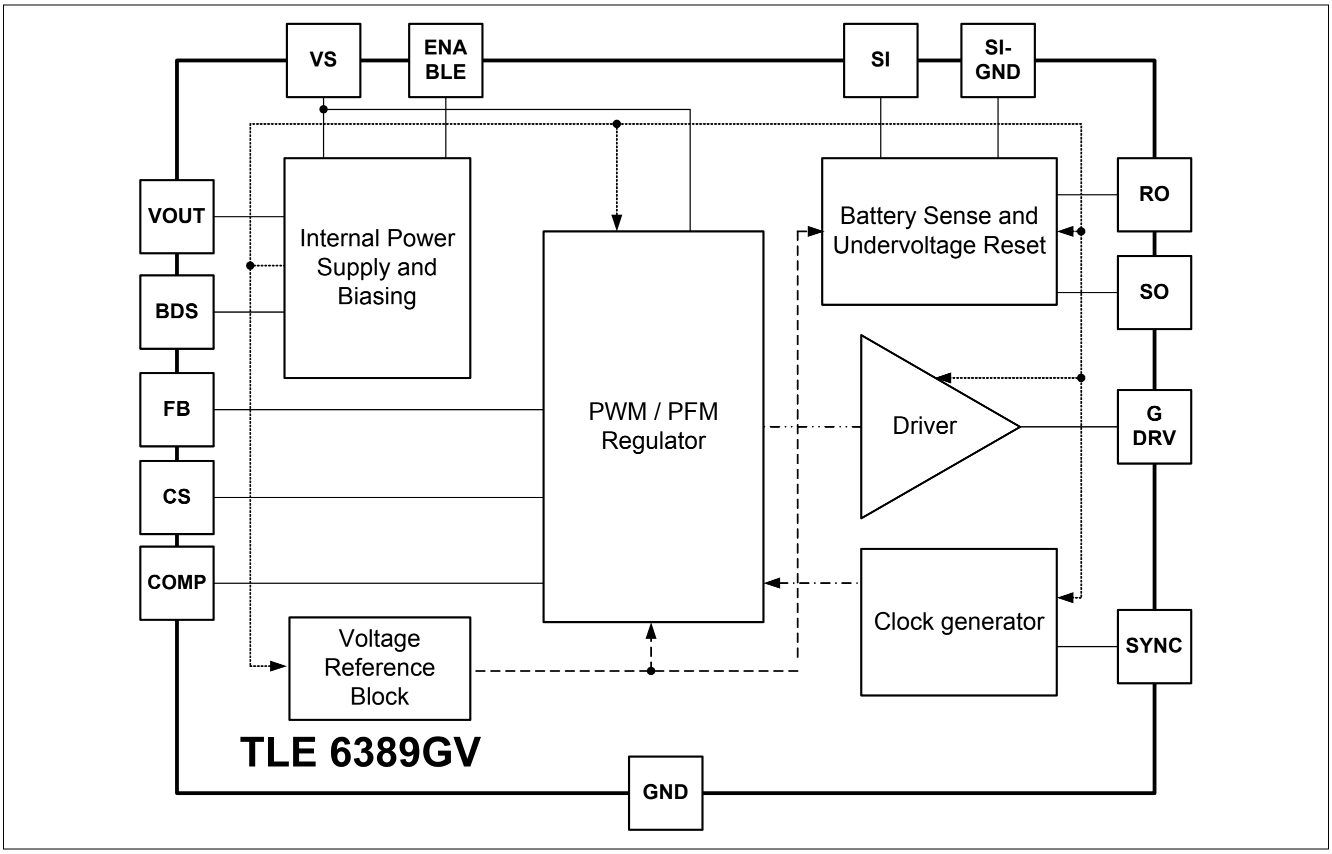


Figure 2 Basic Block Diagram

1.3 Pin Definitions and Functions

Pin No	Symbol	Function
1	ENABLE	**Active-High enable input (only at adjustable version, TLE6389-2GV) for the device.** The device is shut down when ENABLE is driven low. In this shut down-mode the reference, the output and the external MOSFET are turned off. Connect to logic high for normal operation.
1	SI_ENABLE	**Active-High enable input (only at 5V version, TLE6389-2GV50 and TLE6389-3GV50) for SI_GND input.** SI_GND is switched to high impedance when SI_ENABLE is low. High level at SI_ENABLE connects SI_GND to GND with low impedance. SO is undefined when SI_ENABLE is low.
2	FB	**Feedback input.** 1. For adjustable version (-2GV) connect this pin to an external voltage divider from the output to GND (see the determining the output voltage, application section). 2. At the 5V fixed output voltage version (-3GV50 and -2GV50) the FB is connected internally to an on-chip voltage divider. It does not have to be connected externally to the output.
3	VOUT	**Buck output voltage input.** Input for the internal supply. Connect always to the output of the buck converter (output capacitor).
4	GND	**Ground connection.** Analog signal ground.
5	SYNC	**Input for external frequency synchronization.** An external clock signal connected to this pin allows switching frequency synchronization of the device. The internal oscillator is clocked then by the frequency applied at the SYNC input.
6	SI_GND	**SI-Ground input.** Ground connection for SI comparator resistor divider. Depending on SI_ENABLE this input is switched to high impedance or low ohmic to GND.
7	SI	**Sense comparator input.** Input of the low-battery comparator. This input is compared to an internal 1.25V reference where SO gives the result of the comparison. Can be used for any comparison, not necessarily as battery sense.
8	COMP	**Compensation input.** Connect via RC-compensation network to GND.
9	SO	**Sense comparator output.** Open drain output from SI comparator at the adjustable version (TLE6389-2GV), Pull down structure with an internal 20kΩ pull up resistor to VOUT at the 5V version (TLE6389-2GV50 and TLE6389-3GV50).
10	RO	**Reset output.** Open drain output from undervoltage reset comparator at the adjustable version (TLE6389-2GV), Pull down structure with an internal 20kΩ pull up resistor to VOUT at the 5V version (TLE6389-2GV50 and TLE6389-3GV50).
11	BDS	**Buck driver supply input.** Connect a ceramic capacitor between BDS and VS to generate clamped gate-source voltage to supply the driver of the PMOS power stage.
12	GDRV	**Gate drive output.** Connect to the gate of the external P-Channel MOSFET**.** The voltage at GDRV swings between the levels of VS and BDS.

Pin No	Symbol	Function
13	VS	**Device supply input.** Connect a 220nF ceramic cap close to the pin in addition to the low ESR tantalum input capacitance.
14	CS	**Current-sense input.** Connect current-sense resistor between VS and CS. The voltage drop over the sense-resistor determines the peak current flowing in the buck circuit. The external MOSFET is turned off when the peak current is exceeded.

2 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
Device supply input VS						
2.1	Voltage	V_{VS}	-0.3	61	V	–
2.2	Current	I_{VS}	–	–	–	
Current sense input CS						
2.3	Voltage	V_{CS}	-0.3	61	V	$\lvert V_{VS} - V_{CS}\rvert < 0.3V$
2.4	Current	I_{CS}	–	–	–	
Gate drive output GDRV						
2.5	Voltage	V_{GDRV}	– 0.3	61	V	$-0.3V < \lvert V_{VS} - V_{GDRV}\rvert < 6.8V$; $-0.3V < \lvert V_{BDS} - V_{GDRV}\rvert < 6.8V$
2.6	Current	I_{GDRV}	–	–	–	limited internally
Buck driver supply input BDS						
2.7	Voltage	V_{BDS}	– 0.3	61	V	$-0.3V < \lvert V_{VS} - V_{BDS}\rvert < 6.8V$
2.8	Current	I_{BDS}	–	–	–	
Feedback input FB						
2.9	Voltage	V_{FB}	– 0.3	6.8	V	
2.10	Current	I_{FB}	–	–	–	
Enable input SI_ENABLE						
2.11	Voltage	V_{SI_ENABLE}	– 0.3	61	V	TLE6389-2GV50, TLE6389-3GV50
2.12	Current	I_{SI_ENABLE}	–	–	–	
SI-Ground input SI_GND						
2.13	Voltage	V_{SI_GND}	– 0.3	61	V	
2.14	Current	I_{SI_GND}	–	–	–	
Enable input ENABLE						
2.15	Voltage	V_{ENABLE}	– 0.3	61	V	TLE6389-2GV
2.16	Current	I_{ENABLE}	–	–	–	
Sense comparator input SI						
2.17	Voltage	V_{SI}	– 0.3	61	V	
2.18	Current	I_{SI}	–	–	–	
Sense comparator output SO						
2.19	Voltage	V_{SO}	– 0.3	6.8	V	
2.20	Current	I_{SO}	–	–	–	limited internally
Buck output voltage input VOUT						
2.21	Voltage	V_{VOUT}	– 0.3	15	V	TLE6389-2GV
2.22	Voltage	V_{VOUT}	– 0.3	6.8	V	TLE6389-2GV50, TLE6389-3GV50
2.23	Current	I_{VOUT}	–	–	mA	

2 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
Compensation input COMP						
2.24	Voltage	V_{COMP}	– 0.3	6.8	V	
2.25	Current	I_{COMP}	–	–	mA	
Reset output RO						
2.26	Voltage	V_{RO}	– 0.3	6.8	V	
2.27	Current	I_{RO}	–	–	mA	limited internally
Frequency synchronization input SYNC						
2.28	Voltage	V_{SYNC}	– 0.3	6.8	V	
2.29	Current	I_{SYNC}	–	–	mA	
ESD-Protection						
2.30	Electrostatic discharge voltage	V_{ESD}	–1.5	1.5	kV	HBM1), pin VOUT
2.31		V_{ESD}	-2	2	kV	HBM1), all pins except VOUT
2.32		V_{ESDCDM}	–500	500	V	CDM2)
Temperatures						
2.33	Junction temperature	T_j	-40	150	°C	–
2.34	Storage temperature	T_{stg}	-50	150	°C	–

1) ESD susceptibility HBM according to EIA/JESD 22-A 114B.

2) ESD susceptibility CDM according to JESD 22-C101.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3 Operating Range

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
3.1	Supply voltage range	V_{VS}	5	60	V	
3.2	Output voltage adjust range TLE6389-2GV	V_{OUT}	7	15	V	TLE6389-2GV
3.3	Sense Resistor	R_{SENSE}	10	47	mΩ	Calculation see section 7
3.4	PMOS, on+off delay	$t_{on+off\ delay}$	–	t_{min}-300 [1]	ns	$t_{min}= V_{VOUT}/(V_{VS}*f_{SW})$
3.5	Buck driver supply capacitor	C_{BDS}	220	–	nF	
3.6	Buck inductance	L1	47	–	µH	recommended value
3.7	Buck inductance	L1	22	100	µH	
3.8	Buck output capacitor	C_{OUT}	100	–	µF	
3.9	Junction temperature	T_j	– 40	150	°C	
Thermal Resistance						
3.10	Junction ambient	R_{thj-a}	–	140	K/W	Footprint only
3.11	Junction pin	R_{thj-p}	–	50	K/W	–

[1] A too high PMOS on+off delay might cause an instable output voltage

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4 Electrical Characteristics

Table 2 **5V < V_{VS} < 48V; -40°C < T_j < 150°C; All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified**

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Current Consumption[1] TLE6389-2GV50 and TLE6389-3GV50							
4.1	Current consumption of VS	I_{VS}	–	80	150	µA	V_{VS} = 48V; PFM mode;
4.2			–	70	85	µA	V_{VS} = 13.5V; PFM mode; T_j = 25 °C
4.3	Current consumption of SI_ENABLE	I_{SI_ENABLE}	–	9	30	µA	V_{VS} = 48V; V_{SI_ENABLE} = 48V; PFM mode;
4.4	Current consumption of VOUT	I_{VOUT}	–	95	130	µA	V_{SI_ENABLE} = L; V_{VOUT} = 5.5V; V_{VS}=13.5V; PFM mode; T_j = 25°C
4.5			–	140	220	µA	V_{SI_ENABLE} = H; V_{VOUT} = 5.5V; V_{VS} = 13.5V; $V_{SI} > V_{SI,\ high}$; PFM mode;
4.6	Current consumption of SI	I_{SI}	–	0.2	0.5	µA	V_{VS} = 13.5V; V_{SI_ENABLE} = H; V_{SI} = 10V; PFM mode;
Current Consumption[1] TLE6389-2GV (variable)							
4.7	Current consumption of VS	I_{VS}	–	80	150	µA	V_{VS} = 48V; V_{ENABLE} = H; PFM mode; $V_{OUT} \geq$ 7V
4.8	Current consumption of VS		–	70	85	µA	V_{VS} = 13.5V; V_{ENABLE} = H; PFM mode; T_j = 25 °C; $V_{OUT} \geq$ 7V
4.9	Current consumption of VS		–	–	2	µA	V_{ENABLE}=0V; T_j < 105°C
4.10	Current consumption of ENABLE	I_{EN}	–	9	30	µA	V_{VS} = 48V; V_{ENABLE} = H; PFM mode;
4.11	Current consumption of VOUT	I_{VOUT}	–	140	220	µA	V_{OUT} = 8V; V_{VS} = 13.5V; V_{ENABLE} = H; $V_{SI} > V_{SI,\ high}$; PFM mode;
4.12	Current consumption of SI	I_{SI}	–	0.2	0.5	µA	V_{VS} = 13.5V; V_{ENABLE} = H; V_{SI} = 10V; PFM mode; T_j = 25°C
4.13	Current consumption of FB	I_{FB}	–	0.2	0.5	µA	V_{VS} = 13.5V; V_{FB} = 1.25V; V_{ENABLE} = H; PFM mode; T_j = 25°C

4 Electrical Characteristics

Table 2 **5V < V_{VS} < 48V; -40°C < T_j < 150°C; All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified**

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Buck Controller							
4.14	Output voltage	V_{VOUT}	4.85	5.00	5.15	V	TLE6389-2GV50, TLE6389-3GV50; V_{VS}=13.5V& 48V; PWM mode I_{OUT} = 0.5 to 2A; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.15			4.75	5.00	5.25	V	TLE6389-2GV50, TLE6389-3GV50; V_{VS} = 24V;PFM; I_{OUT} = 15mA; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.16			3.8	–	–	V	TLE6389-3GV50; V_{VS} decreasing from 5.8V to 4.2V; I_{LOAD} = 0mA to 500mA; R_{SENSE} = 22mΩ; R_{M1} = 0.4Ω; R_{L1} = 0.1Ω;
4.17	FB threshold voltage	$V_{FB, th}$	1.225	1.25	1.275	V	TLE6389-2GV
4.18	Output voltage	V_{VOUT}	9.7	10.0	10.3	V	TLE6389-2GV; Calibrated divider, see section 7.3; V_{VS} = 13.5V & 48V; I_{OUT} = 0.5 to 2A; PWM Mode; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.19	Output voltage	V_{VOUT}	9.5	10.0	10.5	V	TLE6389-2GV; Calibrated divider, see section 7.3; V_{VS} = 24V; I_{OUT} = 15mA; PFM Mode; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.20	Buck output voltage adjust range	V_{VOUT}	$V_{FB, th}$	–	7	V	TLE6389-2GV, supplied by VS only, complete current to supply the IC drawn from VS, no reset function 2)
4.21	Buck output voltage adjust range	V_{VOUT}	7	–	15	V	TLE6389-2GV, current to supply the IC drawn from VS and VOUT, as specified, 2)

4 Electrical Characteristics

Table 2 5V < V_{VS} < 48V; -40°C < T_j < 150°C; All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.22	Buck output voltage accuracy	V_{VOUT}	0.97*V_{OUT_nom}	–	1.03*V_{OUT_nom}		TLE6389-2GV, PWM mode 2)
4.23	Buck output voltage accuracy	V_{VOUT}	0.95*V_{OUT_nom}	–	1.05*V_{OUT_nom}		TLE6389-2GV, PFM mode 2)
4.24	Line regulation	$\vert \Delta V_{VOUT} \vert$	–	–	35	mV	TLE6389-2GV50, TLE6389-3GV50, V_{VS} = 9V to 16V; I_{OUT} = 1A; R_{SENSE} = 22mΩ; PWM mode
4.25	Line regulation	$\vert \Delta V_{VOUT} \vert$	–	–	50	mV	TLE6389-2GV50, TLE6389-3GV50, V_{VS} = 16V to 32V; I_{OUT} = 1A; R_{SENSE} = 22mΩ; PWM mode
4.26	Line regulation	$\Delta V_{VOUT} / V_{VOUT}$	–	–	2.5	%	TLE6389-2GV, V_{VS} = 12V to 36V; V_{VOUT}=10V I_{OUT} = 1A; R_{SENSE} = 22mΩ; PWM mode
4.27	Load regulation	$\Delta V_{VOUT} / \Delta I_{LOAD}$	–	40	–	mV/A	TLE6389-2GV50, TLE6389-3GV50, I_{OUT} = 0.5A to 2A; V_{VS} = 5.8V & 48V; R_{SENSE} = 22mΩ
4.28			–	8* V_{OUT_nom}/ V	–	mV/A	TLE6389-2GV, I_{OUT} = 0.5 to 2A; V_{VS}= 13.5V & 48V; R_{SENSE} = 22mΩ
4.29	Gate driver, PMOS off	$V_{VS} - V_{GDRV}$	0	–	0.2	V	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF
4.30	Gate driver, PMOS on	$V_{VS} - V_{GDRV}$	6	–	8.2	V	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF 3)
4.31	Gate driver, UV lockout	$V_{VS} - V_{BDS}$	2.75	–	4	V	Decreasing (V_{VS}-V_{BDS}) until GDRV is permanently at VS level

4 Electrical Characteristics

Table 2 **5V < V_{VS} < 48V; -40°C < T_j < 150°C; All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified**

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.32	Gate driver, peak charging current	I_{GDRV}	–	1	–	A	PMOS dependent; 2)
4.33	Gate driver, peak discharging current	I_{GDRV}	–	1	–	A	PMOS dependent; 2)
4.34	Gate driver, gate voltage, rise time	t_r	–	45	60	ns	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF
4.35	Gate driver, gate voltage, fall time	t_f	–	50	65	ns	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF
4.36	Peak current limit threshold voltage	$V_{LIM} = V_{VS} - V_{CS}$	50	70	90	mV	
4.37	Oscillator frequency	f_{OSC}	290	360	420	kHz	PWM mode only
4.38	Maximum duty cycle	d_{MAX}	100	–		%	PWM mode only
4.39	Minimum on time	t_{MIN}	–	220	400	ns	PWM mode only
4.40	SYNC capture range	Δf_{sync}	250	–	530	kHz	PWM mode only
4.41	SYNC trigger level high	$V_{SYNC,h}$	4.0	–	–	V	2)
4.42	SYNC trigger level low		–	–	0.8	V	2)
Reset Generator							
4.43	Reset threshold	$V_{VOUT,\ RT}$	3.5	3.65	3.8	V	TLE6389-3GV50; V_{VOUT} decreasing
4.44			4.5	4.65	4.8	V	TLE6389-3GV50; V_{VOUT} increasing
4.45	Reset headroom	$R_{TV,HEAD}$	80	–	–	mV	TLE6389-2GV50; $V_{OUT}(V_S=6V,$ $I_{LOAD}=1A)$ $-V_{VOUT,RT}$
4.46	Reset threshold	$V_{VOUT,\ RT}$	4.5	4.65	4.8	V	TLE6389-2GV50; V_{VOUT} increasing/decreasing
4.47	Reset threshold hysteresis	$\Delta V_{VOUT,RT}$	–	50	–	mV	TLE6389-2GV50 2)
4.48	Reset threshold	$V_{FB,\ RT}$	–	1.12	–	V	TLE6389-2GV; V_{VOUT} decreasing
4.49			–	1.17	–	V	TLE6389-2GV; V_{VOUT} increasing
4.50	Reset output pull up resistor	R_{RO}	10	20	40	kΩ	TLE6389-2GV50, TLE6389-3GV50; Internally connected to V_{OUT}
4.51	Reset output High voltage	$V_{RO,\ H}$	0.8* V_{VOUT}	–	–	V	TLE6389-2GV50, TLE6389-3GV50; I_{RO}=0mA

4 Electrical Characteristics

Table 2 5V < V_{VS} < 48V; -40°C < T_j < 150°C; All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.52	Reset output Low voltage	$V_{RO,L}$	–	0.2	0.4	V	$I_{RO, L}$=1mA; 2.5V < V_{VOUT} < V_{RT}
4.53	Reset output Low voltage	$V_{RO,L}$	–	0.2	0.4	V	$I_{RO, L}$=0.2mA; 1V < V_{VOUT} < 2.5V
4.54	Reset delay time	t_{rd}	17	21	25	ms	TLE6389-2GV TLE6389-3GV50
4.55	Reset delay time	t_{rd}	70	82	100	ms	TLE6389-2GV50
4.56	Reset reaction time	t_{rr}	–	–	10	µs	2)
Overvoltage Lockout							
4.57	Overvoltage threshold	$V_{VOUT, OV}$	–	V_{OUT_nom}/ V +0.1	–	V	TLE6389-2GV50, TLE6389-3GV50; V_{VOUT} increasing
4.58	Overvoltage threshold	$V_{FB, OV}$	–	V_{FB,th_nom}/ V +0.02	–	V	TLE6389-2GV; V_{VOUT} increasing

4 Electrical Characteristics

Table 2 5V < V_{VS} < 48V; -40°C < T_j < 150°C; All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
ENABLE Input							
4.59	Enable ON-threshold	$V_{ENABLE,ON}$	4.5	–	–	V	
4.60	Enable OFF-threshold	$V_{ENABLE,OFF}$	–	–	0.8	V	
SI_ENABLE Input							
4.61	Enable ON-threshold	$V_{ENABLE,ON}$	4.5	–	–	V	
4.62	Enable OFF-threshold	$V_{ENABLE,OFF}$	–	–	0.8	V	
SI_GND Input							
4.63	Switch ON resistance	R_{SW}	50	100	230	Ω	V_{SI_ENABLE} = 5V; I_{SI_GND} = 3mA;
Battery Voltage Sense							
4.64	Sense threshold	$V_{SI,\ low}$	1.22	1.25	1.28	V	V_{VS} decreasing
4.65	Sense threshold	$V_{SI,\ high}$	–	1.33	–	V	V_{VS} increasing
4.66	Sense threshold hysteresis	$V_{SI,\ hys}$	50	80	120	mV	
4.67	Sense output pull up resistor	R_{SO}	10	20	40	kΩ	TLE6389-2GV50, TLE6389-3GV50; Internally connected to V_{VOUT}
4.68	Sense out output High voltage	$V_{SO,H}$	0.8* V_{VOUT}	–	–	V	$I_{SO,H}$ =0mA
4.69	Sense out output Low voltage	$V_{SO,L}$	–	0.2	0.4	V	$I_{SO,L}$ = 1mA; 2.5V < V_{VOUT}; V_{SI} < 1.13 V
4.70			–	0.4	V_{VOUT}/V	V	I_{SOL}=0.2mA; 1V < V_{VOUT} < 2.5V; V_{SI} < 1.13 V
Thermal Shutdown							
4.71	Thermal shutdown junction temperature	T_{jSD}	150	175	200	°C	2)
4.72	Temperature hysteresis	ΔT	–	30	–	K	2)

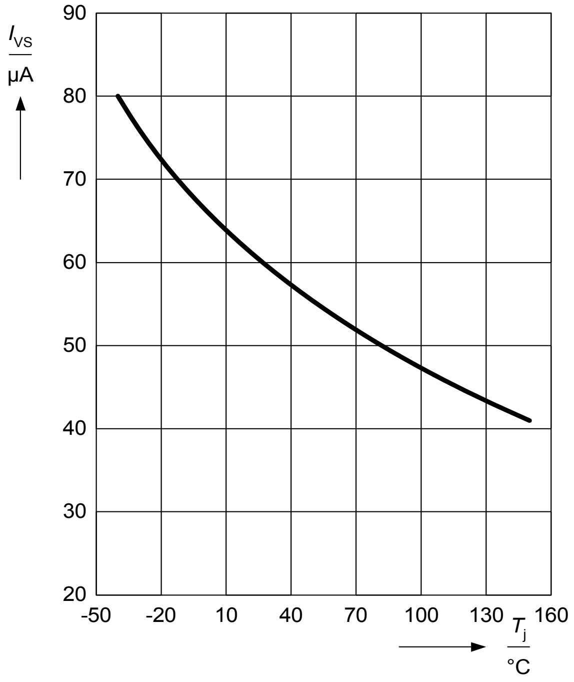
1) The device current measurements for I_{VS} and I_{FB} exclude MOSFET driver currents.

2) Not subject to production test - specified by design

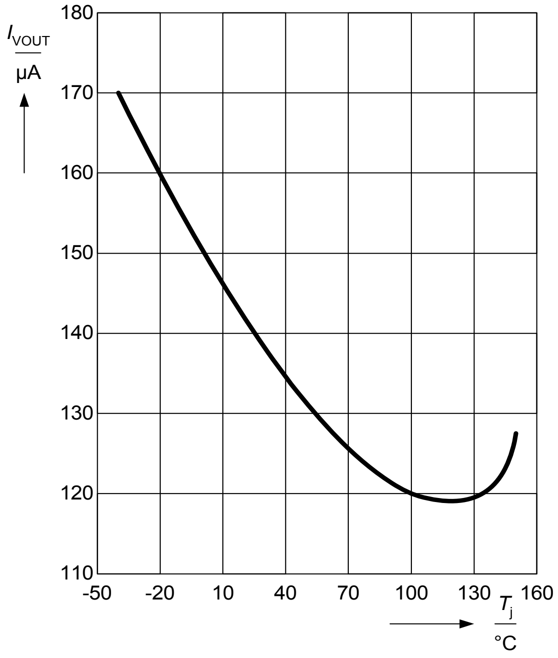
3) For 4V < V_{VS} < 6V: $V_{GDRV} \approx$ 0V.

5 Typical Performance Characteristics

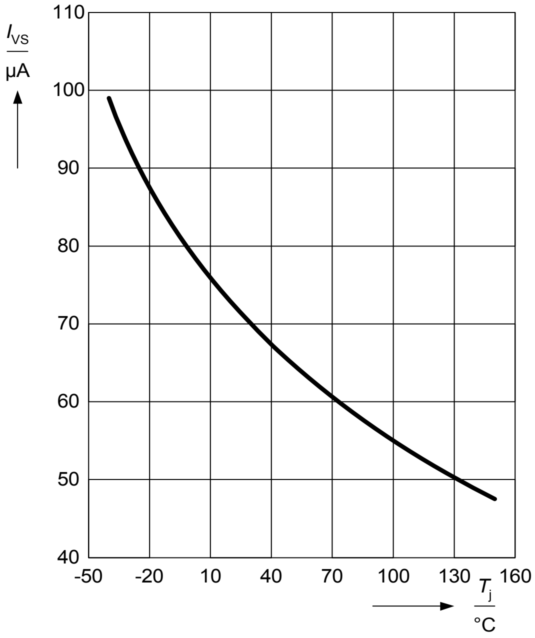
Current consumption I_{VS} vs. temperature T_j at enabled device and V_{VS}=13.5V



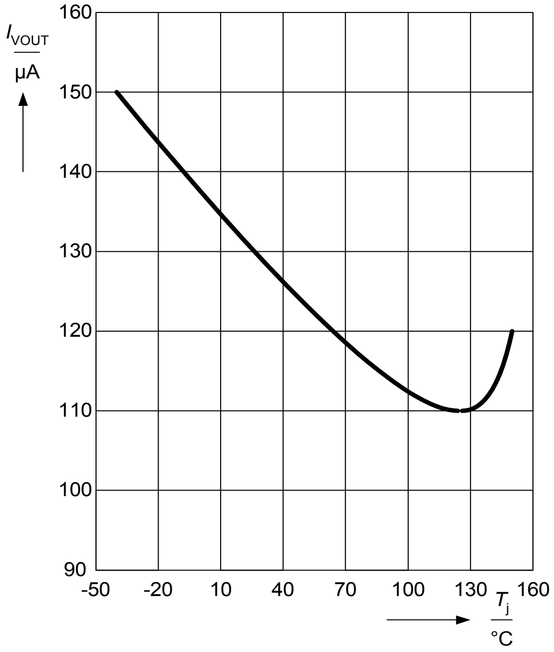
Current consumption I_{VOUT} vs. temperature T_j at enabled device and V_{VOUT}=5.5V



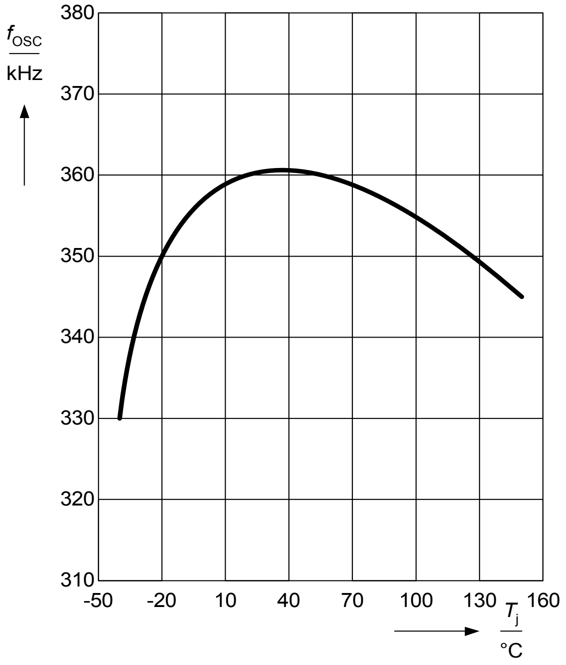
Current consumption I_{VS} vs. temperature T_j at enabled device and V_{VS}=48V



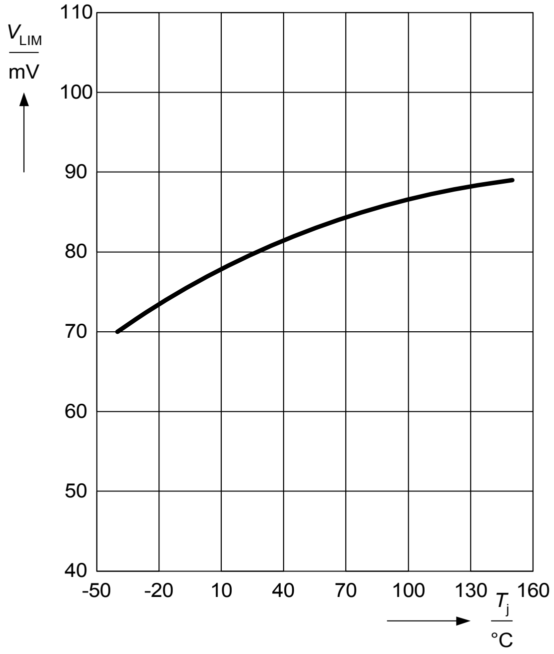
Current consumption I_{VOUT} vs. temperature T_j at enabled device and V_{VOUT}=10V(-2GV)



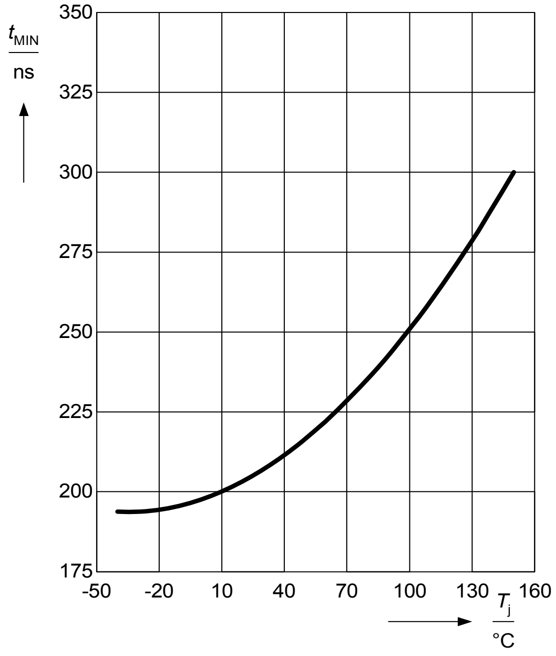
Internal oscillator frequency f_{OSC} vs. temperature T_j



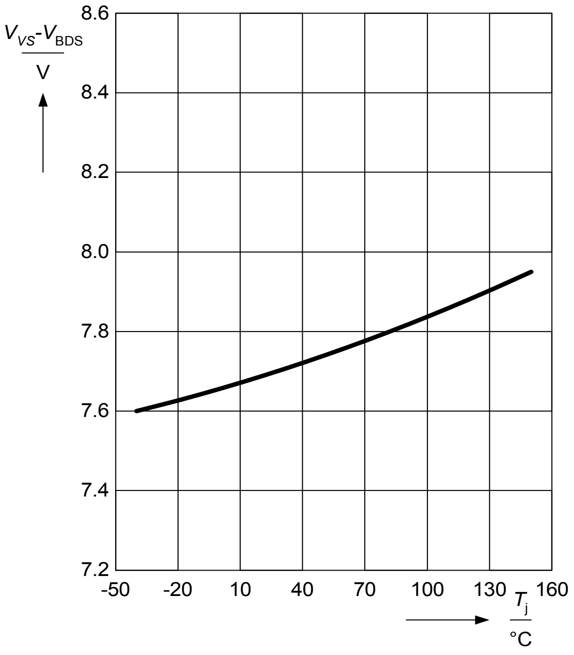
Peak current limit threshold voltage V_{LIM} vs. temperature T_j



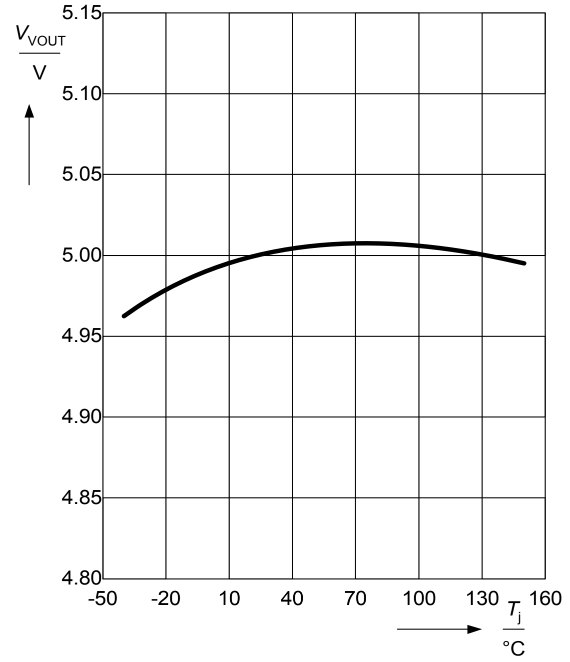
Minimum on time t_{MIN} (blanking) vs. temperature T_j



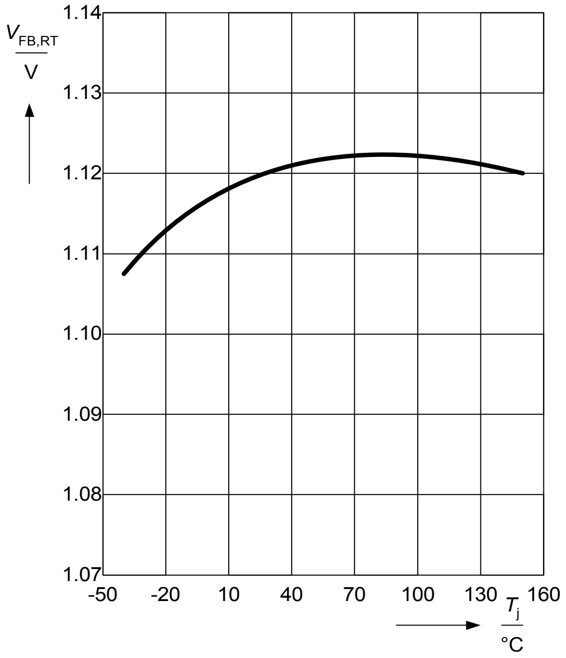
Gate driver supply V_{VS} - V_{BDS} vs. temperature T_j



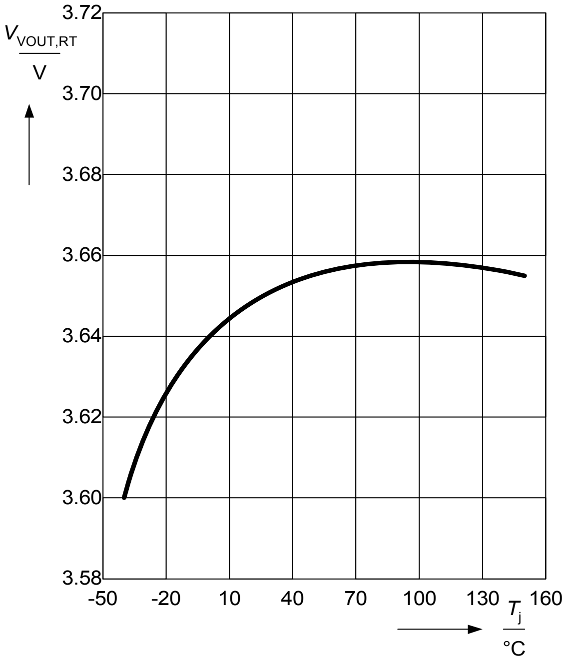
Output voltage V_{VOUT} vs. temperature T_j in PFM mode (V_{VS}=24V,I_{Load}=15mA,-3GV50)



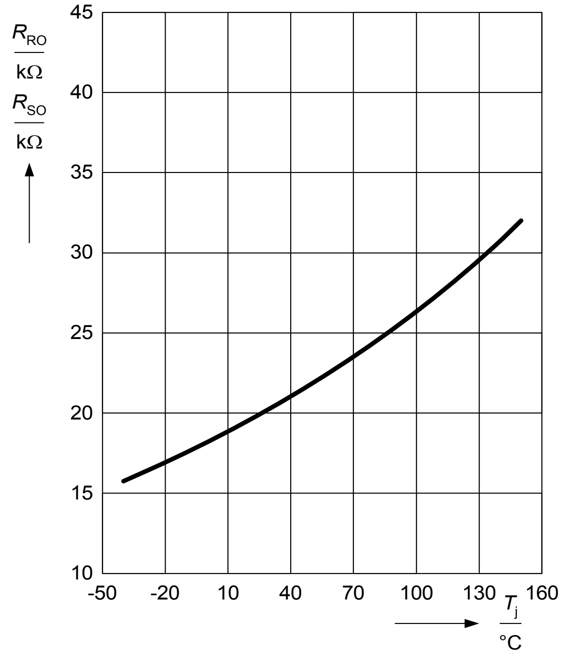
Lower Reset threshold $V_{FB,RT}$ vs. temperature T_j (-2GV)



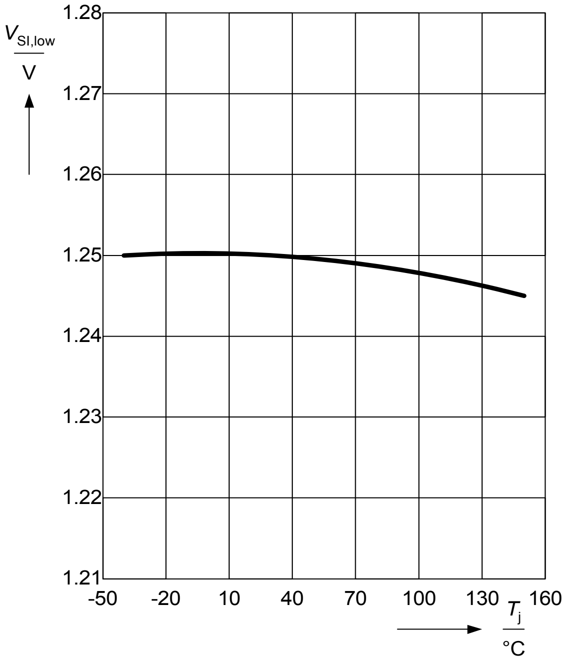
Lower Reset threshold $V_{VOUT,\ RT}$ vs. temperature T_j (-3GV50)



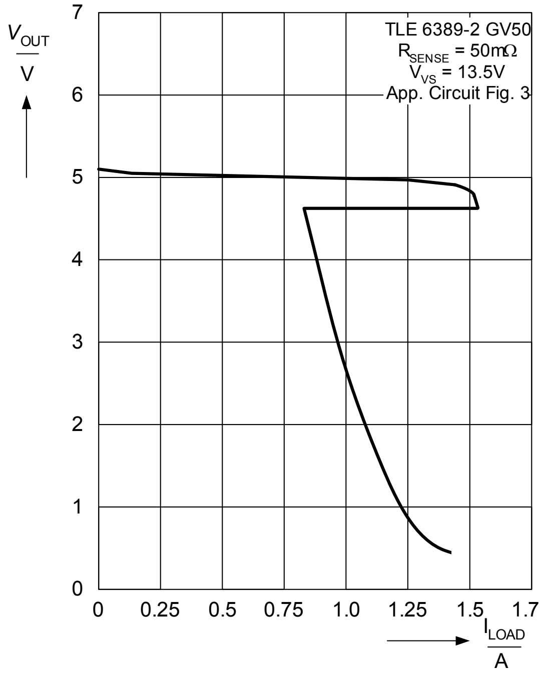
Internal pull up resistors R_{RO} and R_{SO} vs. temperature T_j (-3GV50)



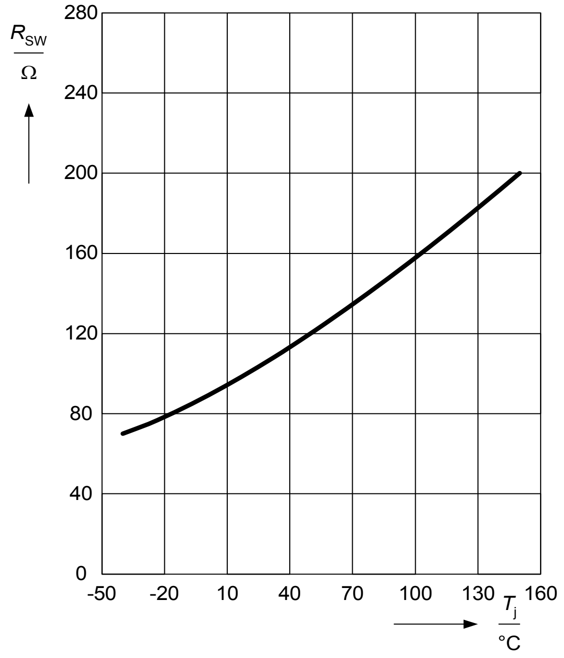
Lower Sense threshold $V_{SI,\ low}$ vs. temperature T_j



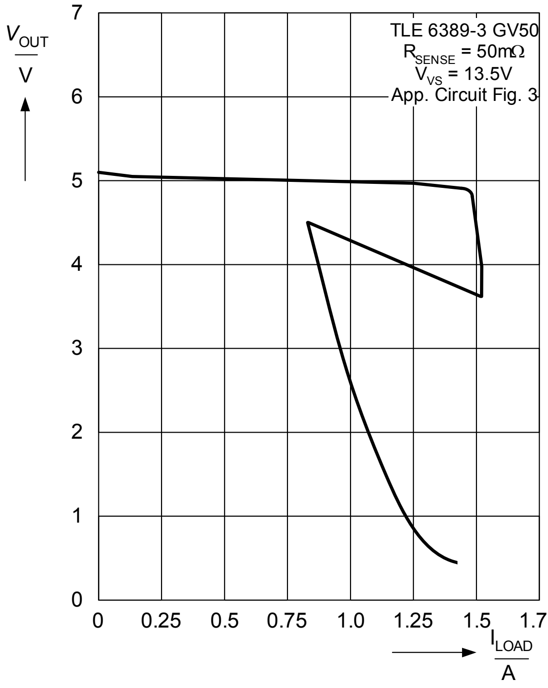
Output Voltage vs. Load Current, TLE6389-2GV50



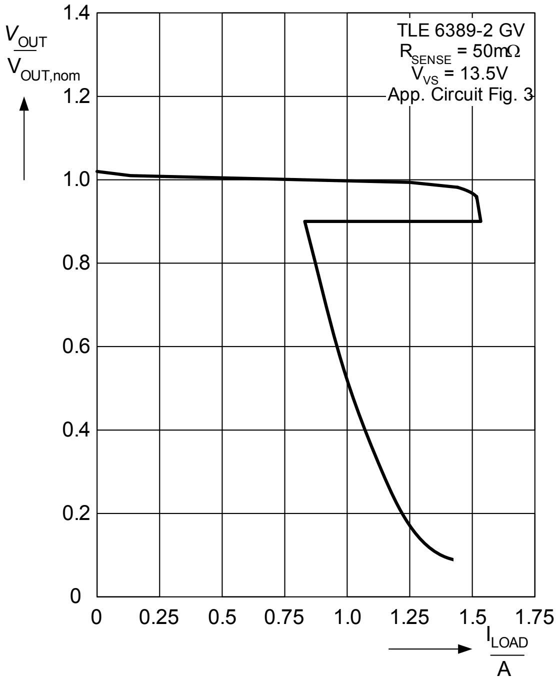
On resistance of SI_GND switch R_{SW} vs. temperature T_j



Output Current vs. Load Current, TLE6389-3GV50



Output Voltage vs Load Current



6 Detailed circuit description

In the following, some internal blocks of the TLE6389 are described in more detail. For the right choice of the external components please refer to the section application information.

6.1 PFM/PWM Step-down regulator

To meet the strict requirements in terms of current consumption demanded by all Body-and 42V PowerNet applications a special PFM (Pulse Frequency Modulation) - PWM (Pulse Width Modulation) control scheme for highest efficiency is implemented in the TLE6389 regulators. Under light load conditions the output voltage is able to increase slightly and at a certain threshold the controller jumps into PFM mode. In this PFM operation the PMOS is triggered with a certain on time (depending on input voltage, output voltage, inductance- and sense resistor value) whenever the buck output voltage decreases to the so called WAKE-threshold. The switching frequency of the step down regulator is determined in the PFM mode by the load current. It increases with increasing load current and turns finally to the fixed PWM frequency at a certain load current depending on the input voltage, current sense resistor and inductance. The diagram below shows the buck regulation circuit of the TLE6389.

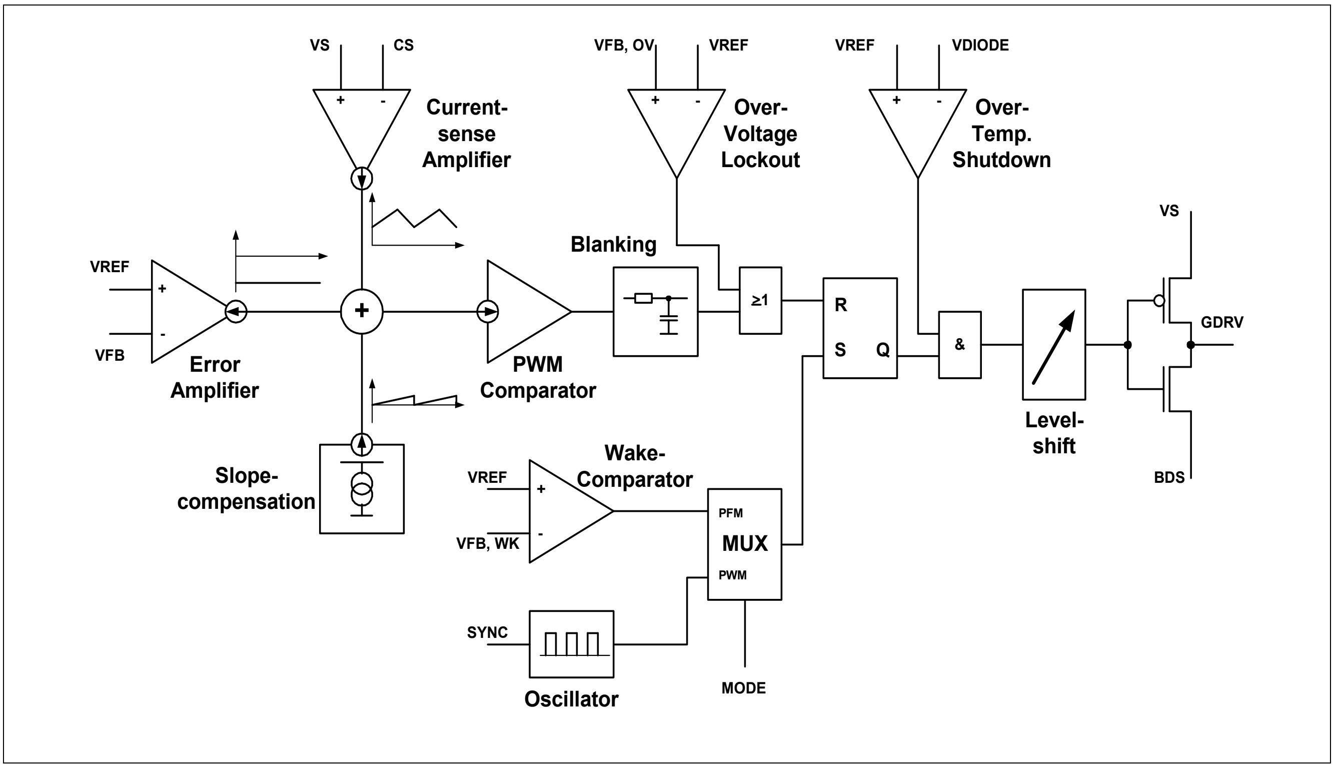


Figure 3 Buck control scheme

The TLE6389 uses a slope-compensated peak current mode PWM control scheme in which the feedback or output voltage of the step down circuit and the peak current of the current through the PMOS are compared to form the OFF signal for the external PMOS. The ON-trigger is set periodically by the internal oscillator when acting in PWM mode and is given by the output of the WAKE-comparator when operating in PFM mode. The Multiplexer (MUX) is switched by the output of the MODE-detector which distinguishes between PFM and PWM by tracking the output voltage (goto PFM) and by tracking the gate trigger frequency (goto PWM). In PFM mode the peak current limit is reduced to prevent overshoots at the output of the buck regulator. In order to avoid a gate turn off signal due to the current peak caused by the parasitic capacitance of the catch diode the blanking filter is necessary. The blanking time is set internally to 200ns and determines (together with the PMOS turn on and turn off delay) the minimum duty cycle of the device. In addition to the PFM/PWM regulation scheme an overvoltage lockout and thermal protection are implemented to guarantee safe operation of the device and of the supplied application circuit.

6.2 Battery voltage sense

To detect undervoltage conditions at the battery a sense comparator block is available within the TLE6389. The voltage at the SI input is compared to an internal reference of typ. 1.25V. The output of the comparator drives a NMOS structure giving a low signal at SO as soon as the voltage at SI decreases below this threshold. In the 5V fixed version an internal pull up resistor is connected from the drain of the NMOS to the output of the buck converter, in the variable version SO is open drain.

The sense in voltage divider can be switched to high impedance by a low signal at the SI_ENABLE to avoid high current consumption to GND (TLE6389-2GV50 and TLE6389-3GV50 only).

Of course the sense comparator can be used for any input voltage and does not have to be used for the battery voltage sense only.

6.3 Undervoltage Reset

The output voltage is monitored continuously by the internal undervoltage reset comparator. As soon as the output voltage decreases below the thresholds given in the characteristics the NPN structure pulls RO low (latched). In the 5V fixed version an internal pull up resistor is connected from the collector of the NPN to the output of the buck converter, in the variable version RO is open collector.

At power up RO is kept low until the output voltage has reached its reset threshold and stayed above this threshold for the power on reset delay time.

7 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

7.1 General

The TLE6389 step-down DC-DC controllers are designed primarily for use in Automotive applications where high input voltage range requirements have to be met. Using an external P-MOSFET and current-sense resistor allows design flexibility and the improved efficiencies associated with high-performance P-channel MOSFETs. The unique, peak current-limited, PWM/PFM control scheme gives these devices excellent efficiency over wide load ranges, while drawing around 100µA current from the battery under no load condition. This wide dynamic range optimizes the TLE6389 for automotive applications, where load currents can vary considerably as individual circuit blocks are turned on and off to conserve energy. Operation to a 100% duty cycle allows the lowest possible dropout voltage, maintaining operation during cold cranking. High switching frequencies and a simple circuit topology minimize PC board area and component costs.

7.2 Typical application circuits

Note: These are very simplified examples of an application circuit. The function must be verified in the real application

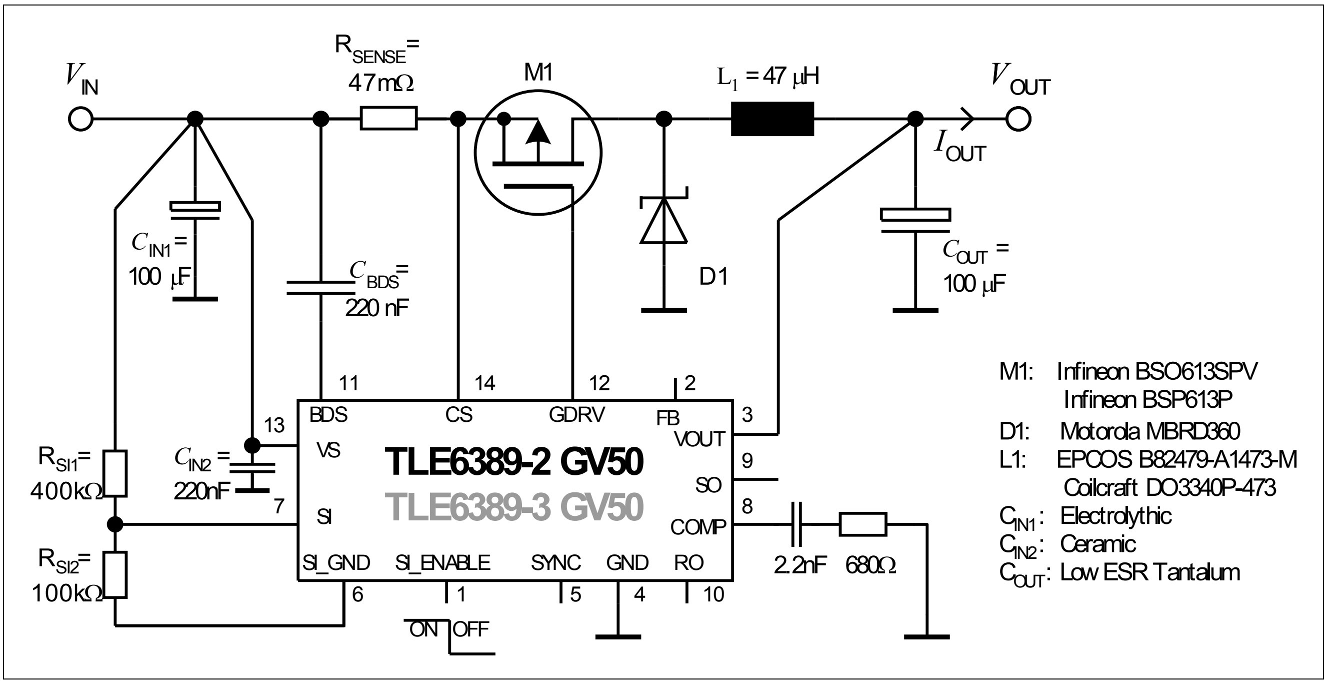


Figure 4 Application circuit TLE6389-2GV50 and TLE6389-3GV50

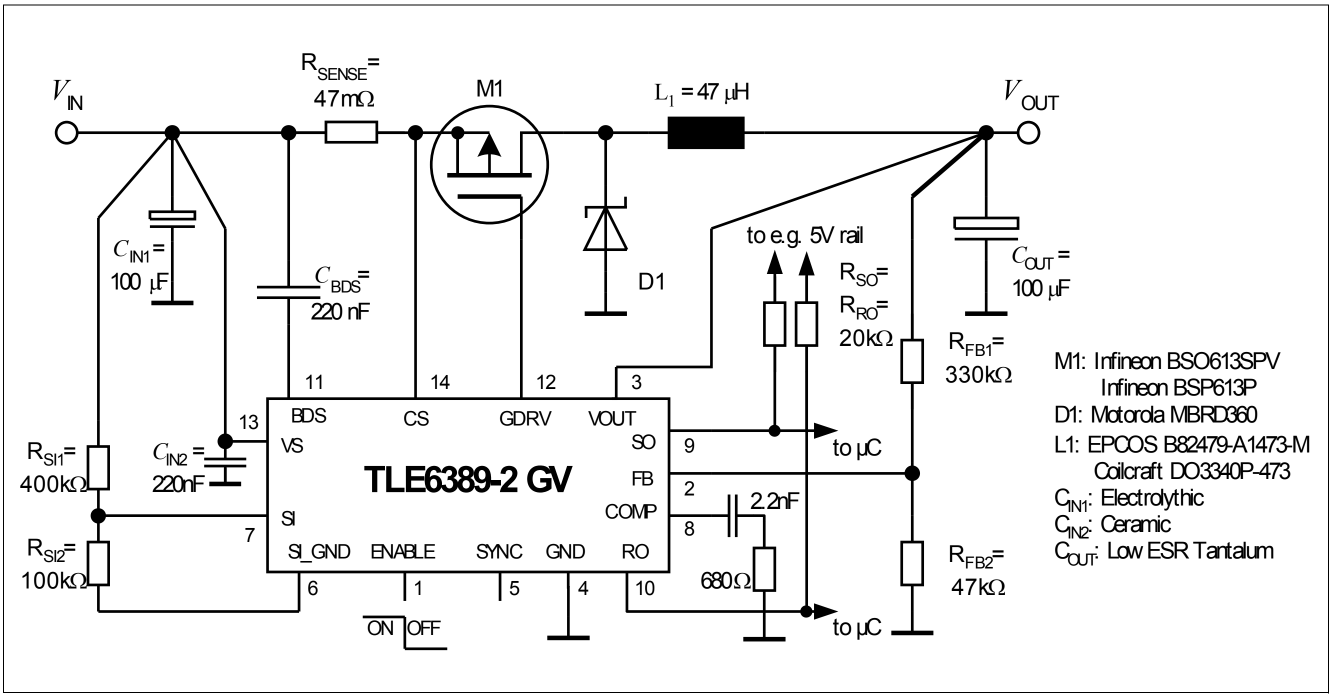


Figure 5 Application circuit TLE6389-2GV

7.3 Output voltage at adjustable version - feedback divider

The output voltage is sensed either by an internal voltage divider connected to the VOUT pin (TLE6389-2GV50 and TLE6389-3GV50, fixed 5V versions) or an external divider from the Buck output voltage to the FB pin (TLE6389-2GV, adjustable version). Pin VOUT has to be connected always to the Buck converter output regardless of the selected output voltage for the -2GV version.

To determine the resistors of the feedback divider for the desired output voltage V_{OUT} at the TLE6389-2GV select R_{FB2} between 5kΩ and 500kΩ and obtain R_{FB1} with the following formula:

$$R_{FB1} = R_{FB2} \cdot \left(\frac{V_{OUT}}{V_{FB,\,th}} - 1\right)$$

V_{FB} is the threshold of the error amplifier with its value of typical 1.25V which shows that the output voltage can be adjusted in a range from 1.25V to 15V. However the integrated Reset function will only be operational if the output voltage level is adjusted to >7V.
Also the current consumption will be increased in PFM mode in the range between
1.25V and 7V.

7.4 SI_Enable

Connecting SI_ENABLE to 5V causes SI_GND to have low impedance. Thus the SI comparator is in operation and can be used to monitor the battery voltage. SO output signal is valid. Connecting SI_ENABLE to GND causes SI_GND to have high impedance. Thus the SI comparator is not able to monitor the battery voltage. SO output signal is invalid.

7.5 Battery sense comparator - voltage divider

The formula to calculate the resistor divider for the sense comparator is basically the same as for the feedback divider in section before. With the selected resistor R_{SI2}, the desired threshold of the input voltage $V_{IN,\,UV}$ and the lower sense threshold $V_{SI,\,low}$ the resistor R_{SI1} is given to:

$$R_{SI1} = R_{SI2} \cdot \left(\frac{V_{IN,\,UV}}{V_{SI,\,low}} - 1\right)$$

For high accuracy and low ohmic resistor divider values the On-resistance of the SI_GND NMOS (typ. 100Ω) has to be added to R_{SI2}.

7.6 Undervoltage reset - delay time

The diagram below shows the typical behavior of the reset output in dependency on the input voltage V_{IN}, the output voltage V_{VOUT} or V_{FB}.

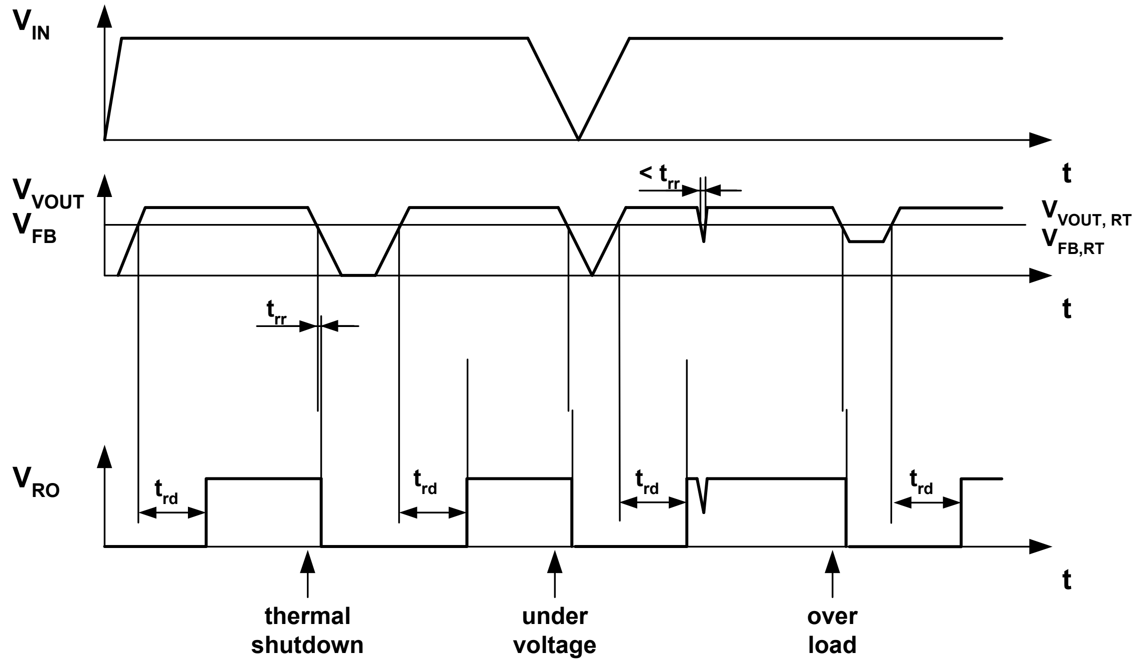


Figure 6 Reset timing

7.7 100% duty-cycle operation and dropout

The TLE6389 operates with a duty cycle up to 100%. This feature allows to operate with the lowest possible drop voltage at low battery voltage as it occurs at cold cranking. The MOSFET is turned on continuously when the supply voltage approaches the output voltage level, conventional switching regulators with less than 100% duty cycle would fail in that case.

The drop- or dropout voltage is defined as the difference between the input and output voltage levels when the input is low enough to drop the output out of regulation. Dropout depends on the MOSFET drain-to-source on-resistance, the current-sense resistor and the inductor series resistance. It is proportional to the load current:

$$V_{drop} = I_{LOAD} \cdot (R_{DS(ON)PMOS} + R_{SENSE} + R_{INDUCTANCE})$$

7.8 SYNC Input and Frequency Control

The TLE6389's internal oscillator is set for a fixed PWM switching frequency of 360kHz or can be synchronized to an external clock at the SYNC pin. When the internal clock is used SYNC has to be connected to GND. SYNC is a negative-edge triggered input that allows synchronization to an external frequency ranging between 270kHz and 530kHz. When SYNC is clocked by an external signal, the converter operates in PWM mode until the load current drops below the PWM to PFM threshold. Thereafter the converter continues operation in PFM mode.

7.9 Shutdown Mode

Connecting ENABLE to GND places the TLE6389-2GV in shutdown mode. In shutdown, the reference, control circuitry, external switching MOSFET, and the oscillator are turned off and the output falls to 0V. Connect ENABLE to voltages higher than 4.5V for normal operation. As this input operates analog the voltage applied at this pin should have a slope of 0.5V/3µs to avoid undefined states within the device.

7.10 Buck converter circuit

A typical choice of external components for the buck converter circuit is given in figure 4 and 5. For basic operation of the buck converter the input capacitors C_{IN1}, C_{IN2}, the driver supply capacitor C_{BDS}, the sense resistor R_{SENSE}, the PMOS device, the catch diode D1, the inductance L1 and the output capacitor C_{OUT} are necessary. In addition for low electromagnetic emission a Pi-filter at the input and/or a small resistor in the path between GDRV and the gate of the PMOS may be necessary.

7.10.1 Buck inductance (L1) selection in terms of ripple current:

The internal PWM/PFM control loop includes a slope compensation for stable operation in PWM mode. This slope compensation is optimized for inductance values of 47µH and Sense resistor values of 47mΩ for the 5V output voltage versions. When choosing an inductance different from 47µH the Sense resistor has to be changed also:

$$\frac{R_{SENSE}}{L1} = (0{,}5 \ldots 1{,}0) \times 10^{3} \frac{\Omega}{H}$$

Increasing this ratio above 1000 Ω/H may result in sub harmonic oscillations as well-known for peak current mode regulators without integrated slope compensation.

To achieve the same effect of slope compensation in the adjustable voltage version also the inductance in µH is given by

$$\left(2{,}0 \times 10^{-4} \cdot \frac{H}{V\Omega} \cdot V_{OUT} \cdot R_{SENSE}\right) < L1 < \left(4{,}0 \times 10^{-4} \cdot \frac{H}{V\Omega} \cdot V_{OUT} \cdot R_{SENSE}\right)$$

The inductance value determines together with the input voltage, the output voltage and the switching frequency the current ripple which occurs during normal operation of the step down converter. This current ripple is important for the all over ripple at the output of the switching converter.

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{f_{SW} \cdot V_{IN} \cdot L1}$$

In this equation f_{sw} is the actual switching frequency of the device, given either by the internal oscillator or by an external source connected to the SYNC pin. When picking finally the inductance of a certain supplier (Epcos, Coilcraft etc.) the saturation current has to be considered. The saturation current value of the desired inductance has to be higher than the maximum peak current which can appear in the actual application.

7.10.2 Determining the current limit

The peak current which the buck converter is able to provide is determined by the peak current limit threshold voltage V_{LIM} and the sense resistor R_{SENSE}. With a maximum peak current given by the application ($I_{PEAK, PWM}=I_{LOAD}+0.5\Delta I$) the sense resistor is calculated to

$$R_{SENSE} = \frac{V_{LIM}}{2 \cdot I_{PEAK, PWM}}$$

The equation above takes account for the foldback characteristic of the current limit as shown in the Fig. 'Output Voltage vs. Load Current' on page 24/25 by introducing a factor of 2. It must be assured by correct dimensioning of R_{SENSE} that the load current doesn't reach the foldback part of the characteristic curve.

7.10.3 PFM and PWM thresholds

The crossover thresholds PFM to PWM and vice versa strongly depend on the input voltage V_{IN}, the Buck converter inductance L1, the sense resistor value R_{SENSE} and the turn on and turn off delays of the external PMOS.

7.10.4 Buck output capacitor (C_{OUT}) selection:

The choice of the output capacitor effects straight to the minimum achievable ripple which is seen at the output of the buck converter. In continuous conduction mode the ripple of the output voltage can be estimated by the following equation:

$$V_{Ripple} = \Delta I \cdot \left(R_{ESRCOUT} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}}\right)$$

From the formula it is recognized that the ESR has a big influence in the total ripple at the output, so low ESR tantalum capacitors are recommended for the application.

One other important thing to note are the requirements for the resonant frequency of the output LC-combination. The choice of the components L and C have to meet also the specified range given in section 3 otherwise instabilities of the regulation loop might occur.

7.10.5 Input capacitor (C_{IN1}) selection:

At high load currents, where the current through the inductance flows continuously, the input capacitor is exposed to a square wave current with its duty cycle V_{OUT}/V_I. To prevent a high ripple to the battery line a capacitor with low ESR should be used. The maximum RMS current which the capacitor has to withstand is calculated to:

$$I_{RMS} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}}} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta I}{2 \cdot I_{LOAD}}\right)^2}$$

For low ESR an e.g. Al-electrolytic capacitance in parallel to an ceramic capacitance could be used.

7.10.6 Freewheeling diode / catch diode (D1)

For lowest power loss in the freewheeling path Schottky diodes are recommended. With those types the reverse recovery charge is negligible and a fast hand over from freewheeling to forward conduction mode is possible. Depending on the application (12V battery systems) 40V types could be also used instead of the 60V diodes. Also for high temperature operation select a Schottky-diode with low reverse leakage.

A fast recovery diode with recovery times in the range of 30ns can be also used if smaller junction capacitance values (smaller spikes) are desired.

7.10.7 Buck driver supply capacitor (C_{BDS})

The voltage at the ceramic capacitor is clamped internally to 7V, a ceramic type with a minimum of 220nF and voltage class 16V would be sufficient.

7.10.8 Input pi-filter components for reduced EME

At the input of Buck converters a square wave current is observed causing electromagnetical interference on the battery line. The emission to the battery line consists on one hand of components of the switching frequency (fundamental wave) and its harmonics and on the other hand of the high frequency components derived from the current slope. For proper attenuation of those interferers a π-type input filter structure is recommended which is built up with inductive and capacitive components in addition to the Input caps C_{IN1} and C_{IN2}. The inductance can be chosen up to the value of the Buck converter inductance, higher values might not be necessary, the additional capacitance should be a ceramic type in the range up to 100nF.

Inexpensive input filters show due to their parasitrics a notch filter characteristic, which means basically that the low pass filter acts from a certain frequency as a high pass filter and means further that the high frequency components are not attenuated properly. To slower down the slopes at the gate of the PMOS switch and get down the emission in the high frequency range a small gate resistor can be put between GDRV and the PMOS gate.

7.10.9 Frequency compensation

The external frequency compensation pin should be connected via a 2.2nF ($\geq$10V) ceramic capacitor and a 680 Ω (1/8W) resistor to GND. This node should be kept free from switching noise.

7.11 Components recommendation - Overview

Device	Type	Supplier	Remark
C_{IN1}	Electrolytic /Foil type	various	100µF, 60V
C_{IN2}	Ceramic	various	220nF, 60V
L1	B82464-A4473	EPCOS	47µH, 1.6A, 145mΩ
	B82479-A1473-M	EPCOS	47µH, 3.5A, 47mΩ
	DO3340P-473	Coilcraft	47µH, 3.8A, 110mΩ
	DO5022P-683	Coilcraft	68µH, 3.5A, 130mΩ
	DS5022P-473	Coilcraft	47µH, 4.0A, 97mΩ
M1	BSO 613SPV	Infineon	60V, 3.44A, 130mΩ, NL
	BSP 613P	Infineon	60V, 2.9A, 130mΩ, NL
	SPD09P06PL	Infineon	60V, 9A, 250mΩ, LL
C_{BDS}	Ceramic	various	220nF, 16V
D1	MBRD360	Motorola	Schottky, 60V, 3A
	MBRD340	Motorola	Schottky, 40V, 3A
	SS34	various	Schottky, 40V, 3A
C_{OUT}	B45197-A2107	EPCOS	Low ESR Tantalum, 100µF, 10V
C_{COMP}	Ceramic	various	see 7.10.9.

7.12 Layout recommendation

The most sensitive points for Buck converters - when considering the layout - are the nodes at the input, output and the gate of the PMOS transistor and the feedback path.

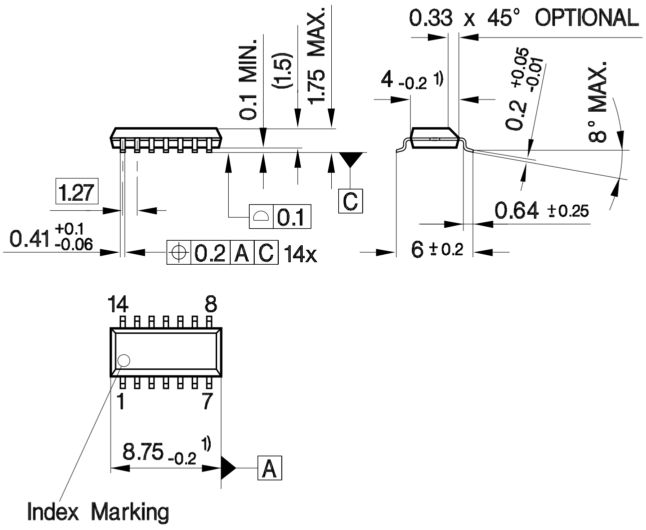
For proper operation and to avoid stray inductance paths the external catch diode, the Buck inductance and the input capacitor C_{IN1} have to be connected as close as possible to the PMOS device. Also the GDRV path from the controller to the MOSFET has to be as short as possible. Best suitable for the connection of the cathode of the catch diode and one terminal of the inductance would be a small plain located next to the drain of the PMOS.

The GND connection of the catch diode must be also as short as possible. In general the GND level should be implemented as surface area over the whole PCB as second layer, if necessary as third layer. The feedback path has to be well grounded also, a ceramic capacitance might help in addition to the output cap to avoid spikes.

To obtain the optimum filter capability of the input pi-filter it has to be located also as close as possible to the input. To filter the supply input of the device (VS) the ceramic cap should be connected directly to the pin.

As a guideline an EMC optimized application board / layout is available.

8 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 7 Outline PG-DSO-14 (Plastic Green Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision History

Version	Date	Changes
Rev.2.2	2018-06-20	Update package outline, page 4 changed pinconfig drawing to PG-DSO-14 Page 1: Marking corrected, chapter 7.10.3: deleted paragraph “For more details...” Update Layout style
Rev. 2.1	2007-08-13	Initial version of RoHS-compliant derivate of TLE6389-2/-3 Page 1: AEC certified statement added Page 1 and **Page 30**: RoHS compliance statement and green product feature added Page 1 and **Page 30**: Package changed to RoHS compliant version Legal Disclaimer updated
Rev. 2.0	2006-08-24	Final Datasheet TLE6389-2/-3

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